**DS0141**

**Datasheet**

**PolarFire**

![Microsemi — a Microchip company logo]

# Contents

# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 1.5

Revision 1.5 was published in November 2018. The following is a summary of changes.

- All tables have been reviewed and updated to reflect production silicon characteristics for the 200T, 200TL, 200TS, 200TLS, 100T, 100TL, 100TS, and 100TLS devices in all packages, speed grades, and temperature grades.
- The maximum transceiver reference clock input rate was changed from 800 MHz to 400 MHz due to a typo in version 1.4. For more information, see table PolarFire Transceiver Reference Clock AC Requirements (see page 43).

## 1.2 Revision 1.4

Revision 1.4 was published September 2018. The following is a summary of changes.

- All tables have been reviewed and updated to reflect production silicon characteristics for the 300T, 300TL, 300TS, and 300TLS devices in all packages, speed grades, and temperature grades.

## 1.3 Revision 1.3

Revision 1.3 was published in June 2018. The following is a summary of changes.

- The System Services section was updated. For more information, see System Services (see page 66).
- The Non-Volatile Characteristics section was updated. For more information, see Non-Volatile Characteristics (see page 57).
- The Fabric Macros section was updated. For more information, see Fabric Macros (see page 67).
- The Transceiver Switching Characteristics section was updated. For more information, see Transceiver Switching Characteristics (see page 41).

## 1.4 Revision 1.2

Revision 1.2 was published in June 2018. The following is a summary of changes.

- The datasheet has moved to preliminary status. Every table has been updated.

## 1.5 Revision 1.1

Revision 1.1 was published in August 2017. The following is a summary of changes.

- LVDS specifications changed to 1.25G. For more information, see HSIO Maximum Input Buffer Speed and HSIO Maximum Output Buffer Speed.
- LVDS18, LVDS25/LVDS33, and LVDS25 specifications changed to 800 Mbps. For more information, see I/O Standards Specifications.
- A note was added indicting a zeroization cycle counts as a programming cycle. For more information, see Non-Volatile Characteristics.
- A note was added defining power down conditions for programming recovery conditions. For more information, see Power-Supply Ramp Times.

## 1.6 Revision 1.0

Revision 1.0 was the first publication of this document.

# 2 Overview

This datasheet describes PolarFire® FPGA device characteristics with industrial temperature range (−40 °C to 100 °C $T_J$) and extended commercial temperature range (0 °C to 100 °C $T_J$). The devices are provided with a standard speed grade (STD) and a −1 speed grade with higher performance. The FPGA core supply $V_{DD}$ can operate at 1.0 V for lower-power or 1.05 V for higher performance. Similarly, the transceiver core supply $V_{DDA}$ can also operate at 1.0 V or 1.05 V. Users select the core operating voltage while creating the Libero project.

# 3    References

The following documents are recommended references. For more information about PolarFire static and dynamic power data, see the PolarFire Power Estimator Spreadsheet.

- PO0137: PolarFire FPGA Product Overview
- ER0217: PolarFire FPGA Pre-Production Device Errata
- UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide
- UG0726: PolarFire FPGA Board Design User Guide
- UG0686: PolarFire FPGA User I/O User Guide
- UG0680: PolarFire FPGA Fabric User Guide
- UG0714: PolarFire FPGA Programming User Guide
- UG0684: PolarFire FPGA Clocking Resources User Guide
- UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide
- UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide
- UG0748: PolarFire FPGA Low Power User Guide
- UG0676: PolarFire FPGA DDR Memory Controller User Guide
- UG0743: PolarFire FPGA Debugging User Guide
- UG0725: PolarFire FPGA Device Power-Up and Resets User Guide
- UG0677: PolarFire FPGA Transceiver User Guide
- UG0685: PolarFire FPGA PCI Express User Guide
- UG0753: PolarFire FPGA Security User Guide
- UG0752: PolarFire FPGA Power Estimator User Guide

# 4 Device Offering

The following table lists the PolarFire FPGA device options using the MPF300T as an example. The MPF100T, MPF200T, and MPF500T device densities have identical offerings.

Table 1 • PolarFire FPGA Device Options

| Device Options | Extended Commercial 0 °C–100 °C | Industrial –40 °C–100 °C | STD | –1 | Transceivers T | Lower Static Power L | Data Security S |
|---|---|---|---|---|---|---|---|
| MPF300T | Yes | Yes | Yes | Yes | Yes | | |
| MPF300TL | Yes | Yes | Yes | | Yes | Yes | |
| MPF300TS | | Yes | Yes | Yes | Yes | | Yes |
| MPF300TLS | | Yes | Yes | | Yes | Yes | Yes |

# 5 Silicon and Libero Tool Status

There are three status levels:

- **Advanced**—initial estimated information based on simulations
- **Preliminary**—information based on simulation and/or initial characterization
- **Production**—final production data

The following tables shows the status of the PolarFire FPGA silicon devices and Libero Timing and Power tool status.

**Table 2 • PolarFire FPGA Silicon Status**

| Product | Silicon |
|---------|---------|
| MPF100T, TS, TL, TLS | Production |
| MPF200T, TS, TL, TLS | Production |
| MPF300T, TS, TL, TLS | Production |
| MPF500T, TS, TL, TLS | Preliminary |

**Table 3 • PolarFire FPGA Tool Status**

| Product | Status | Libero PolarFire SoC Version | | | | | | | |
|---------|--------|------|------|------|------|------|------|------|------|
| | | Timing | | | | Power | | | |
| | | Extended Commercial | | Industrial | | Extended Commercial | | Industrial | |
| | | STD | −1 | STD | −1 | STD | −1 | STD | −1 |
| MPF100T, TS, TL, TLS | Preliminary | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 |
| | Production | | | | | | | | |
| MPF200T, TS, TL, TLS | Preliminary | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 |
| | Production | | | | | | | | |
| MPF300T, TS, TL, TLS | Preliminary | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 |
| | Production | | | | | | | | |
| MPF500T, TS, TL, TLS | Preliminary | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 | v2.2 |
| | Production | | | | | | | | |

# 6 DC Characteristics

This section lists the DC characteristics of the PolarFire FPGA device.

## 6.1 Absolute Maximum Rating

The following table lists the absolute maximum ratings for PolarFire devices.

Table 4 • Absolute Maximum Rating

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| FPGA core power supply | $V_{DD}$ | −0.5 | 1.13 | V |
| Transceiver Tx and Rx lanes supply | $V_{DDA}$ | −0.5 | 1.13 | V |
| Programming and HSIO receiver supply | $V_{DD18}$ | −0.5 | 2.0 | V |
| FPGA core and FPGA PLL high-voltage supply | $V_{DD25}$ | −0.5 | 2.7 | V |
| Transceiver PLL high-voltage supply | $V_{DDA25}$ | −0.5 | 2.7 | V |
| Transceiver reference clock supply | $V_{DD\_XCVR\_CLK}$ | −0.5 | 3.6 | V |
| Global $V_{REF}$ for transceiver reference clocks | $XCVR_{VREF}$ | −0.5 | 3.6 | V |
| HSIO DC I/O supply[2] | $V_{DDIx}$ | −0.5 | 2.0 | V |
| GPIO DC I/O supply[2] | $V_{DDIx}$ | −0.5 | 3.6 | V |
| Dedicated I/O DC supply for JTAG and SPI | $V_{DDI3}$ | −0.5 | 3.6 | V |
| GPIO auxiliary power supply for I/O bank x[2] | $V_{DDAUXx}$ | −0.5 | 3.6 | V |
| Maximum DC input voltage on GPIO | $V_{IN}$ | −0.5 | 3.8 | V |
| Maximum DC input voltage on HSIO | $V_{IN}$ | −0.5 | 2.2 | V |
| Transceiver Receiver absolute input voltage | Transceiver $V_{IN}$ | −0.5 | 1.26 | V |
| Transceiver Reference clock absolute input voltage | Transceiver REFCLK $V_{IN}$ | −0.5 | 3.6 | V |
| Storage temperature (ambient)[1] | $T_{STG}$ | −65 | 150 | °C |
| Junction temperature[1] | $T_J$ | −55 | 135 | °C |
| Maximum soldering temperature RoHS | $T_{SOLROHS}$ | | 260 | °C |

1. See FPGA Programming Cycles vs Retention Characteristics for retention time vs. temperature. The total time used in calculating the device retention includes the device operating temperature time and temperature during storage time.
2. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

## 6.2 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 5 • Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| FPGA core supply at 1.0 V mode[1] | $V_{DD}$ | 0.97 | 1.00 | 1.03 | V | |
| FPGA core supply at 1.05 V mode[1] | $V_{DD}$ | 1.02 | 1.05 | 1.08 | V | |
| Transceiver TX and RX lanes supply (1.0 V mode) | $V_{DDA}$ | 0.97 | 1.00 | 1.03 | V | When all lane rates are 10.3125 Gbps or less.[1] |

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Transceiver TX and RX lanes supply (1.05 V mode) | $V_{DDA}$ | 1.02 | 1.05 | 1.08 | V | Must when any lane rate is greater than 10.3125 Gbps. Lane rates 10.3125 Gbps or less may also be powered in 1.05 V mode.[1] |
| Programming and HSIO receiver supply | $V_{DD18}$ | 1.71 | 1.80 | 1.89 | V | |
| FPGA core and FPGA PLL high-voltage supply | $V_{DD25}$ | 2.425 | 2.50 | 2.575 | V | |
| Transceiver PLL high-voltage supply | $V_{DDA25}$ | 2.425 | 2.50 | 2.575 | V | |
| Transceiver reference clock supply | $V_{DD\_XCVR\_CLK}$ | 3.135 | 3.3 | 3.465 | V | 3.3 V nominal |
| | | 2.375 | 2.5 | 2.625 | V | 2.5 V nominal |
| Global $V_{REF}$ for transceiver reference clocks[3] | $XCVR_{VREF}$ | Ground | | $V_{DD\_XCVR\_CLK}$ | V | |
| HSIO DC I/O supply | $V_{DDIx}$ | 1.14 | Various | 1.89 | V | Allowed nominal options: 1.2 V, 1.35 V, 1.5 V, and 1.8 V[4,5] |
| GPIO DC I/O supply | $V_{DDIx}$ | 1.14 | Various | 3.465 | V | Allowed nominal options: 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V[2,4,5] |
| Dedicated I/O DC supply for JTAG and SPI (GPIO Bank 3) | $V_{DDI3}$ | 1.71 | Various | 3.465 | V | Allowed nominal options: 1.8 V, 2.5 V, and 3.3 V |
| GPIO auxiliary supply | $V_{DDAUXx}$ | 3.135 | 3.3 | 3.465 | V | For I/O bank x with $V_{DDIx}$ = 3.3 V nominal[2,4,5] |
| | | 2.375 | 2.5 | 2.625 | V | For I/O bank x with $V_{DDIx}$ = 2.5 V nominal or lower[2,4,5] |
| Extended commercial temperature range | $T_J$ | 0 | | 100 | °C | |
| Industrial temperature range | $T_J$ | −40 | | 100 | °C | |
| Extended commercial programming temperature range | $T_{PRG}$ | 0 | | 100 | °C | |
| Industrial programming temperature range | $T_{PRG}$ | −40 | | 100 | °C | |

1. $V_{DD}$ and $V_{DDA}$ can independently operate at 1.0 V or 1.05 V nominal. These supplies are not dynamically adjustable.
2. For GPIO buffers where I/O bank is designated as bank number, if $V_{DDIx}$ is 2.5 V nominal or 3.3 V nominal, $V_{DDAUXx}$ must be connected to the $V_{DDIx}$ supply for that bank. If $V_{DDIx}$ for a given GPIO bank is <2.5 V nominal, $V_{DDAUXx}$ per I/O bank must be powered at 2.5 V nominal.
3. $XCVR_{VREF}$ globally sets the reference voltage of the transceiver's single-ended reference clock input buffers. It is typically near $V_{DD\_XCVR\_CLK}$/2 V but is allowed in the specified range.
4. The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.
5. At power up and power down the VDDIx and VDDAUXx supply sequencing can cause signal glitches. Refer to UG0686: PolarFire FPGA I/O User Guide and UG0726: PolarFire FPGA Board Design User Guide for detailed explanation and recommended steps.

### 6.2.1 DC Characteristics over Recommended Operating Conditions

The following table lists the DC characteristics over recommended operating conditions.

Table 6 • DC Characteristics over Recommended Operating Conditions

| Parameter | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| Input pin capacitance[1] | $C_{IN}$ (dedicated GPIO) | | 5.6 | pf | |
| | $C_{IN}$ (GPIO) | | 5.6 | pf | |
| | $C_{IN}$ (HSIO) | | 2.8 | pf | |
| Input or output leakage current per pin | $I_L$ (GPIO) | | 10 | µA | I/O disabled, high – Z |
| | $I_L$ (HSIO) | | 10 | µA | I/O disabled, high – Z |
| Input rise time (10%–90% of $V_{DDIx}$)[2] | $T_{RISE}$ | | | ns | |
| Input fall time (90%–10% of $V_{DDIx}$)[2] | $T_{FALL}$ | | | ns | |
| Pad pull-up when $V_{IN}$ = 0[5] | $I_{PU}$ | 137 | 220 | µA | $V_{DDIx}$ = 3.3 V |
| Pad pull-up when $V_{IN}$ = 0[5] | | 102 | 166 | µA | $V_{DDIx}$ = 2.5 V |
| Pad pull-up when $V_{IN}$ = 0 | | 68 | 115 | µA | $V_{DDIx}$ = 1.8 V |
| Pad pull-up when $V_{IN}$ = 0 | | 51 | 88 | µA | $V_{DDIx}$ = 1.5 V |
| Pad pull-up when $V_{IN}$ = 0[6] | | 29 | 73 | µA | $V_{DDIx}$ = 1.35 V |
| Pad pull-up when $V_{IN}$ = 0 | | 16 | 46 | µA | $V_{DDIx}$ = 1.2 V |
| Pad pull-down when $V_{IN}$ = 3.3 V[3] | $I_{PD}$ | 65 | 187 | µA | $V_{DDIx}$ = 3.3 V |
| Pad pull-down when $V_{IN}$ = 2.5 V[3] | | 63 | 160 | µA | $V_{DDIx}$ = 2.5 V |
| Pad pull-down when $V_{IN}$ = 1.8 V | | 60 | 117 | µA | $V_{DDIx}$ = 1.8 V |
| Pad pull-down when $V_{IN}$ = 1.5 V | | 57 | 95 | µA | $V_{DDIx}$ = 1.5 V |
| Pad pull-down when $V_{IN}$ = 1.35 V | | 52 | 86 | µA | $V_{DDIx}$ = 1.35 V |
| Pad pull-down when $V_{IN}$ = 1.2 V | | 47 | 79 | µA | $V_{DDIx}$ = 1.2 V |

1. Represents the die input capacitance at the pad not the package.
2. Voltage ramp must be monotonic.
3. GPIO only.

### 6.2.2 Maximum Allowed Overshoot and Undershoot

During transitions, input signals may overshoot and undershoot the voltage shown in the following table. Input currents must be limited to less than 100 mA per latch-up specifications.

The maximum overshoot duration is specified as a high-time percentage over the lifetime of the device. A DC signal is equivalent to 100% of the duty-cycle.

The following table shows the maximum AC input voltage ($V_{IN}$) overshoot duration for HSIO.

Table 7 • Maximum Overshoot During Transitions for HSIO

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | 1.8 |
| 100 | 1.85 |
| 100 | 1.9 |
| 100 | 1.95 |
| 100 | 2 |

| AC (V$_{IN}$) Overshoot Duration as % at T$_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | 2.05 |
| 100 | 2.1 |
| 100 | 2.15 |
| 100 | 2.2 |
| 90 | 2.25 |
| 30 | 2.3 |
| 7.5 | 2.35 |
| 1.9 | 2.4 |

**Note:** Overshoot level is for VDDI at 1.8 V.

The following table shows the maximum AC input voltage (V$_{IN}$) undershoot duration for HSIO.

**Table 8 • Maximum Undershoot During Transitions for HSIO**

| AC (V$_{IN}$) Undershoot Duration as % at T$_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | −0.05 |
| 100 | −0.1 |
| 100 | −0.15 |
| 100 | −0.2 |
| 100 | −0.25 |
| 100 | −0.3 |
| 100 | −0.35 |
| 100 | −0.4 |
| 44 | −0.45 |
| 14 | −0.5 |
| 4.8 | −0.55 |
| 1.6 | −0.6 |

The following table shows the maximum AC input voltage (V$_{IN}$) overshoot duration for GPIO.

**Table 9 • Maximum Overshoot During Transitions for GPIO**

| AC (V$_{IN}$) Overshoot Duration as % at T$_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | 3.8 |
| 100 | 3.85 |
| 100 | 3.9 |
| 100 | 3.95 |
| 70 | 4 |
| 50 | 4.05 |
| 33 | 4.1 |
| 22 | 4.15 |
| 14 | 4.2 |
| 9.8 | 4.25 |
| 6.5 | 4.3 |

| AC ($V_{IN}$) Overshoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 4.4 | 4.35 |
| 3 | 4.4 |
| 2 | 4.45 |
| 1.4 | 4.5 |
| 0.9 | 4.55 |
| 0.6 | 4.6 |

**Note:** Overshoot level is for $V_{DDI}$ at 3.3 V.

The following table shows the maximum AC input voltage ($V_{IN}$) undershoot duration for GPIO.

**Table 10 • Maximum Undershoot During Transitions for GPIO**

| AC ($V_{IN}$) Undershoot Duration as % at $T_J$ = 100 °C | Condition (V) |
|---|---|
| 100 | −0.5 |
| 100 | −0.55 |
| 100 | −0.6 |
| 100 | −0.65 |
| 100 | −0.7 |
| 100 | −0.75 |
| 100 | −0.8 |
| 100 | −0.85 |
| 100 | −0.9 |
| 100 | −0.95 |
| 100 | −1 |
| 100 | −1.05 |
| 100 | −1.1 |
| 100 | −1.15 |
| 100 | −1.2 |
| 69 | −1.25 |
| 45 | −1.3 |

## 6.2.2.1 Power Supply Ramp Times

The following table shows the allowable power-up ramp times. Times shown correspond to the ramp of the supply from 0 V to the minimum recommended voltage as specified in the section Recommended Operating Conditions (see page 6). All supplies must rise and fall monotonically.

**Table 11 • Power Supply Ramp Times**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| FPGA core supply | $V_{DD}$ | 0.2 | 50 | ms |
| Transceiver core supply | $V_{DDA}$ | 0.2 | 50 | ms |
| Must connect to 1.8 V supply | $V_{DD18}$ | 0.2 | 50 | ms |
| Must connect to 2.5 V supply | $V_{DD25}$ | 0.2 | 50 | ms |
| Must connect to 2.5 V supply | $V_{DDA25}$ | 0.2 | 50 | ms |
| HSIO bank I/O power supplies | $V_{DDI[0,1,6,7]}$ | 0.2 | 50 | ms |

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| GPIO bank I/O power supplies | $V_{DDI[2,4,5]}$ | 0.2 | 50 | ms |
| Bank 3 dedicated I/O buffers (GPIO) | $V_{DDI3}$ | 0.2 | 50 | ms |
| GPIO bank auxiliary power supplies | $V_{DDAUX[2,4,5]}$ | 0.2 | 50 | ms |
| Transceiver reference clock supply | $V_{DD\_XCVR\_CLK}$ | 0.2 | 50 | ms |
| Global $V_{REF}$ for transceiver reference clocks | $XCVR_{VREF}$ | 0.2 | 50 | ms |

**Note:** For proper operation of programming recovery mode, if a VDD supply brownout occurs during programming, a minimum supply ramp down time for only the VDD supply is recommended to be 10 ms or longer by using a programmable regulator or on-board capacitors.

### 6.2.2.2 Hot Socketing

The following table lists the hot socketing DC characteristics over recommended operating conditions.

**Table 12 • Hot Socketing DC Characteristics over Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Current per transceiver Rx input pin (P or N single-ended)[1, 2] | $XCVRRX\_HS$ | | | ±4 | mA | $V_{DDA}$ = 0 V |
| Current per transceiver Tx output pin (P or N single-ended)[3] | $XCVRTX\_HS$ | | | ±10 | mA | $V_{DDA}$ = 0 V |
| Current per transceiver reference clock input pin (P or N single-ended)[4] | $XCVRREF\_HS$ | | | ±1 | mA | $V_{DD\_XCVR\_CLK}$ = 0 V |
| Current per GPIO pin (P or N single-ended)[5] | $I_{GPIO\_HS}$ | | | ±1 | mA | $V_{DDIx}$ = 0 V |
| Current per HSIO pin (P or N single-ended) | | | | | | Hot socketing is not supported in HSIO. |

1. Assumes device is powered-down, all supplies are grounded, AC-coupled interface, and input pin pairs are driven by a CML driver at the maximum amplitude (1 V pk–pk) that is toggling at any rate with PRBS7 data.
2. Each P and N transceiver input has less than the specified maximum input current.
3. Each P and N transceiver output is connected to a 40 Ω resistor (50 Ω CML termination – 20% tolerance) to the maximum allowed output voltage ($V_{DDAmax}$ + 0.3 V = 1.4 V) through an AC-coupling capacitor with all PolarFire device supplies grounded. This shows the current for a worst-case DC coupled interface. As an AC-coupled interface, the output signal will settle at ground and no hot socket current will be seen.
4. $V_{DD\_XCVR\_CLK}$ is powered down and the device is driven to –0.3 V < $V_{IN}$ < $V_{DD\_XCVR\_CLK}$.
5. $V_{DDIx}$ is powered down and the device is driven to –0.3 V < $V_{IN}$ < GPIO $V_{DDImax}$.

**Note**: The following dedicated pins do not support hot socketing: TMS, TDI, TRSTB, and DEVRST_N. Weak pull-up (as specified in GPIO) is always enabled.

## 6.3 Input and Output

The following section describes:

- DC I/O levels
- Differential and complementary differential DC I/O levels
- HSIO and GPIO on-die termination specifications
- LVDS specifications

### 6.3.1 DC Input and Output Levels

The following tables list the DC I/O levels.

**Table 13 • DC Input Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{IL}$ Min (V) | $V_{IL}$ Max (V) | $V_{IH}$ Min (V) | $V_{IH}$[1] Max (V) |
|---|---|---|---|---|---|---|---|
| PCI | 3.15 | 3.3 | 3.45 | −0.3 | $0.3 \times V_{DDI}$ | $0.5 \times V_{DDI}$ | 3.45 |
| LVTTL | 3.15 | 3.3 | 3.45 | −0.3 | 0.8 | 2 | 3.45 |
| LVCMOS33 | 3.15 | 3.3 | 3.45 | −0.3 | 0.8 | 2 | 3.45 |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | −0.3 | 0.7 | 1.7 | 2.625 |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | −0.3 | $0.35 \times V_{DDI}$ | $0.65 \times V_{DDI}$ | 1.89 |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | −0.3 | $0.35 \times V_{DDI}$ | $0.65 \times V_{DDI}$ | 1.575 |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | −0.3 | $0.35 \times V_{DDI}$ | $0.65 \times V_{DDI}$ | 1.26 |
| SSTL25I[2] | 2.375 | 2.5 | 2.625 | −0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | 2.625 |
| SSTL25II[2] | 2.375 | 2.5 | 2.625 | −0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | 2.625 |
| SSTL18I[2] | 1.71 | 1.8 | 1.89 | −0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | 1.89 |
| SSTL18II[2] | 1.71 | 1.8 | 1.89 | −0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | 1.89 |
| SSTL15I | 1.425 | 1.5 | 1.575 | −0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 1.575 |
| SSTL15II | 1.425 | 1.5 | 1.575 | −0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 1.575 |
| SSTL135I | 1.283 | 1.35 | 1.418 | −0.3 | $V_{REF} - 0.09$ | $V_{REF} + 0.09$ | 1.418 |
| SSTL135II | 1.283 | 1.35 | 1.418 | −0.3 | $V_{REF} - 0.09$ | $V_{REF} + 0.09$ | 1.418 |
| HSTL15I | 1.425 | 1.5 | 1.575 | −0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 1.575 |
| HSTL15II | 1.425 | 1.5 | 1.575 | −0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 1.575 |
| HSTL135I | 1.283 | 1.35 | 1.418 | −0.3 | $V_{REF} - 0.09$ | $V_{REF} + 0.09$ | 1.418 |
| HSTL135II | 1.283 | 1.35 | 1.418 | −0.3 | $V_{REF} - 0.09$ | $V_{REF} + 0.09$ | 1.418 |
| HSTL12I | 1.14 | 1.2 | 1.26 | −0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 1.26 |
| HSTL12II | 1.14 | 1.2 | 1.26 | −0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 1.26 |
| HSUL18I | 1.71 | 1.8 | 1.89 | −0.3 | $0.3 \times V_{DDI}$ | $0.7 \times V_{DDI}$ | 1.89 |
| HSUL18II | 1.71 | 1.8 | 1.89 | −0.3 | $0.3 \times V_{DDI}$ | $0.7 \times V_{DDI}$ | 1.89 |
| HSUL12I | 1.14 | 1.2 | 1.26 | −0.3 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 1.26 |
| POD12I | 1.14 | 1.2 | 1.26 | −0.3 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | 1.26 |
| POD12II | 1.14 | 1.2 | 1.26 | −0.3 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | 1.26 |

1. GPIO $V_{IH}$ max is 3.45 V with PCI clamp diode turned off regardless of mode, that is, over-voltage tolerant.
2. For external stub-series resistance. This resistance is on-die for GPIO.

Note: 3.3 V and 2.5 V are only supported in GPIO banks.

**Table 14 • DC Output Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Max (V) | $V_{OH}$ Min (V) | $I_{OL}^{2,6}$ mA | $I_{OH}^{2,6}$ mA |
|---|---|---|---|---|---|---|---|
| PCI[1] | 3.15 | 3.3 | 3.45 | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | 1.5 | 0.5 |
| LVTTL | 3.15 | 3.3 | 3.45 | 0.4 | 2.4 | | |
| LVCMOS33 | 3.15 | 3.3 | 3.45 | 0.4 | $V_{DDI} - 0.4$ | Refer to note 2 | |
| LVCMOS25 | 2.375 | 2.5 | 2.625 | 0.4 | $V_{DDI} - 0.4$ | | |
| LVCMOS18 | 1.71 | 1.8 | 1.89 | 0.45 | $V_{DDI} - 0.45$ | | |
| LVCMOS15 | 1.425 | 1.5 | 1.575 | $0.25 \times V_{DDI}$ | $0.75 \times V_{DDI}$ | | |
| LVCMOS12 | 1.14 | 1.2 | 1.26 | $0.25 \times V_{DDI}$ | $0.75 \times V_{DDI}$ | | |
| SSTL25I[3] | 2.375 | 2.5 | 2.625 | $V_{TT} - 0.608$ | $V_{TT} + 0.608$ | 8.1 | 8.1 |
| SSTL25II[3] | 2.375 | 2.5 | 2.625 | $V_{TT} - 0.810$ | $V_{TT} + 0.810$ | 16.2 | 16.2 |
| SSTL18I[3] | 1.71 | 1.8 | 1.89 | $V_{TT} - 0.603$ | $V_{TT} + 0.603$ | 6.7 | 6.7 |
| SSTL18II[3] | 1.71 | 1.8 | 1.89 | $V_{TT} - 0.603$ | $V_{TT} + 0.603$ | 13.4 | 13.4 |
| SSTL15I[4] | 1.425 | 1.5 | 1.575 | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} - V_{OH})/40$ |
| SSTL15II[4] | 1.425 | 1.5 | 1.575 | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/34$ | $(V_{DDI} - V_{OH})/34$ |
| SSTL135I[4] | 1.283 | 1.35 | 1.418 | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} - V_{OH})/40$ |
| SSTL135II[4] | 1.283 | 1.35 | 1.418 | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/34$ | $(V_{DDI} - V_{OH})/34$ |
| HSTL15I | 1.425 | 1.5 | 1.575 | 0.4 | $V_{DDI} - 0.4$ | 8 | 8 |
| HSTL15II | 1.425 | 1.5 | 1.575 | 0.4 | $V_{DDI} - 0.4$ | 16 | 16 |
| HSTL135I[4] | 1.283 | 1.35 | 1.418 | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/50$ | $(V_{DDI} - V_{OH})/50$ |
| HSTL135II[4] | 1.283 | 1.35 | 1.418 | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} - V_{OH})/25$ |
| HSTL12I[4] | 1.14 | 1.2 | 1.26 | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/50$ | $(V_{DDI} - V_{OH})/50$ |
| HSTL12II[4] | 1.14 | 1.2 | 1.26 | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} - V_{OH})/25$ |
| HSUL18I[4] | 1.71 | 1.8 | 1.89 | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/55$ | $(V_{DDI} - V_{OH})/55$ |
| HSUL18II[4] | 1.71 | 1.8 | 1.89 | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} - V_{OH})/25$ |
| HSUL12I[4] | 1.14 | 1.2 | 1.26 | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} - V_{OH})/40$ |
| POD12I[4,5] | 1.14 | 1.2 | 1.26 | $0.5 \times V_{DDI}$ | | $V_{OL}/48$ | $(V_{DDI} - V_{OH})/48$ |
| POD12II[4,5] | 1.14 | 1.2 | 1.26 | $0.5 \times V_{DDI}$ | | $V_{OL}/34$ | $(V_{DDI} - V_{OH})/34$ |

1. Drive strengths per PCI specification V/I curves.
2. Refer to UG0686: PolarFire FPGA User I/O User Guide for details on supported drive strengths.
3. For external stub-series resistance. This resistance is on-die for GPIO.
4. $I_{OL}/I_{OH}$ units for impedance standards in amps (not mA).
5. VOH_MAX based on external pull-up termination (pseudo-open drain).
6. The total DC sink/source current of all IOs within a lane is limited as follows:
   a. HSIO lane: 120 mA per 12 IO buffers.
   b. GPIO lane: 160 mA per 12 IO buffers.

**Note:** 3.3 V and 2.5 V are only supported in GPIO banks.

## 6.3.2 Differential DC Input and Output Levels

The follow tables list the differential DC I/O levels.

**Table 15 • Differential DC Input Levels**

| I/O Standard | Bank Type | VICM_RANGE Libero Setting | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| LVDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS18[4] | GPIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LVDS18 | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS18 | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| LCMDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.35 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.35 | 0.6 |
| RSDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| RSDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| MINILVDS33 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| MINILVDS18[5] | HSIO | Mid (default) | 0.6 | 1.25 | 1.65 | 0.1 | 0.3 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.3 | 0.6 |
| SUBLVDS33 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | Mid (default) | 0.6 | 0.9 | 2.35 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| SUBLVDS18[5] | HSIO | Mid (default) | 0.6 | 0.9 | 1.65 | 0.1 | 0.15 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| PPDS25 | GPIO | Mid (default) | 0.6 | 0.8 | 2.35 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |

| I/O Standard | Bank Type | VICM_RANGE Libero Setting | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$ Typ (V) | $V_{ID}$ Max (V) |
|---|---|---|---|---|---|---|---|---|
| PPDS18[5] | HSIO | Mid (default) | 0.6 | 0.8 | 1.65 | 0.1 | 0.2 | 0.6 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.6 |
| SLVS33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |
| SLVS25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.1 | 0.2 | 0.3 |
| SLVS18[5] | HSIO | Mid (default) | 0.6 | 1.00 | 1.65 | 0.1 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.2 | 0.3 |
| HCSL33[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |
| HCSL25[6] | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.35 | 0.8 | 0.1 | 0.55 | 1.1 |
| HCSL18[5] | HSIO | Mid (default) | 0.6 | 1.0 | 1.65 | 0.1 | 0.55 | 1.1 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.1 | 0.55 | 1.1 |
| BUSLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.1 | $V_{DDIn}$ |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.1 | $V_{DDIn}$ |
| MLVDSE25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.35 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.35 | 2.4 |
| LVPECL33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| LVPECLE33 | GPIO | Mid (default) | 0.6 | 1.65 | 2.35 | 0.05 | 0.8 | 2.4 |
| | | Low | 0.05 | 0.4 | 0.8 | 0.05 | 0.8 | 2.4 |
| MIPI25 | GPIO | Mid (default) | 0.6 | 1.25 | 2.35 | 0.05 | 0.2 | 0.3 |
| | | Low | 0.05 | 0.2 | 0.8 | 0.05 | 0.2 | 0.3 |

1. $V_{ICM}$ is the input common mode.
2. $V_{ID}$ is the input differential voltage.
3. $V_{ICM}$ rules are as follows:
    a. $V_{ICM}$ must be less than $V_{DDI} - 0.4$ V;
    b. $V_{ICM} + V_{ID}/2$ must be $< V_{DDI} + 0.4$ V;
    c. $V_{ICM} - V_{ID}/2$ must be $> VSS - 0.3$ V;
    d. Any differential input with $V_{ICM} \leq 0.6$ V requires the low common mode setting in Libero (VICM_RANGE=LOW).
4. VDDI = 1.8 V, VDDAUX = 2.5 V.
5. HSIO receiver only.
6. GPIO receiver only.

**Table 16 • Differential DC Output Levels**

| I/O Standard | Bank Type | $V_{OCM}$[1] Min (V) | $V_{OCM}$ Typ (V) | $V_{OCM}$ Max (V) | $V_{OD}$[2] Min (V) | $V_{OD}$[2] Typ (V) | $V_{OD}$[2] Max (V) |
|---|---|---|---|---|---|---|---|
| LVDS33 | GPIO | 1.125 | 1.2 | 1.375 | 0.25 | 0.35 | 0.45 |
| LVDS25 | GPIO | 1.125 | 1.2 | 1.375 | 0.25 | 0.35 | 0.45 |
| LCMDS33 | GPIO | 0.45 | 0.6 | 0.7 | 0.25 | 0.35 | 0.45 |
| LCMDS25 | GPIO | 0.45 | 0.6 | 0.7 | 0.25 | 0.35 | 0.45 |
| RSDS33 | GPIO | 1.125 | 1.2 | 1.375 | 0.17 | 0.2 | 0.23 |
| RSDS25 | GPIO | 1.125 | 1.2 | 1.375 | 0.17 | 0.2 | 0.23 |
| MINILVDS33 | GPIO | 1.125 | 1.2 | 2.375 | 0.3 | 0.4 | 0.6 |
| MINILVDS25 | GPIO | 1.125 | 1.2 | 2.375 | 0.3 | 0.4 | 0.6 |
| SUBLVDS33 | GPIO | 0.8 | 0.9 | 1.0 | 0.1 | 0.15 | 0.3 |
| SUBLVDS25 | GPIO | 0.8 | 0.9 | 1.0 | 0.1 | 0.15 | 0.3 |
| PPDS33 | GPIO | 0.05 | 0.8 | 1.4 | 0.17 | 0.2 | 0.23 |
| PPDS25 | GPIO | 0.05 | 0.8 | 1.4 | 0.17 | 0.2 | 0.23 |
| SLVSE15[3] | GPIO, HSIO | 0.1 | 0.2 | 0.3 | 0.12 | 0.135 | 0.15 |
| BUSLVDSE25[3] | GPIO | 1.15 | 1.25 | 1.31 | 0.24 | 0.262 | 0.272 |
| MLVDSE25[3] | GPIO | 1.15 | 1.25 | 1.31 | 0.396 | 0.442 | 0.453 |
| LVPECLE33[3] | GPIO | 1.51 | 1.65 | 1.74 | 0.664 | 0.722 | 0.755 |
| MIPIE25 [3] | GPIO | 0.15 | 0.25 | 0.35 | 0.1 | 0.22 | 0.3 |

1. $V_{OCM}$ is the output common mode voltage.
2. $V_{OD}$ is the output differential voltage.
3. Emulated output o nly, using external resistors.

### 6.3.3 Complementary Differential DC Input and Output Levels

The following tables list the complementary differential DC I/O levels.

**Table 17 • Complementary Differential DC Input Levels**

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{ICM}$[1,3] Min (V) | $V_{ICM}$[1,3] Typ (V) | $V_{ICM}$[1,3] Max (V) | $V_{ID}$[2] Min (V) | $V_{ID}$[2] Max (V) |
|---|---|---|---|---|---|---|---|---|
| SSTL25I | 2.375 | 2.5 | 2.625 | 1.164 | 1.250 | 1.339 | 0.1 | $V_{DDAUX}$ (GPIO) |
| SSTL25II | 2.375 | 2.5 | 2.625 | 1.164 | 1.250 | 1.339 | 0.1 | $V_{DDAUX}$ (GPIO) |
| SSTL18I | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL18II | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL15I | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL15II | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| SSTL135I | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |
| SSTL135II | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |
| HSTL15I | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| HSTL15II | 1.425 | 1.5 | 1.575 | 0.698 | 0.750 | 0.803 | 0.1 | $V_{DDAUX}$ (GPIO) $V_{DDI}$ (HSIO) |
| HSTL135I | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |
| HSTL135II | 1.283 | 1.35 | 1.418 | 0.629 | 0.675 | 0.723 | 0.1 | $V_{DDI}$ (HSIO) |
| HSTL12I | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 | $V_{DDI}$ (HSIO) |
| HSTL12II | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 | $V_{DDI}$ (HSIO) |
| HSUL18I | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDI}$ (HSIO) |
| HSUL18II | 1.71 | 1.8 | 1.89 | 0.838 | 0.900 | 0.964 | 0.1 | $V_{DDI}$ (HSIO) |
| HSUL12I | 1.14 | 1.2 | 1.26 | 0.559 | 0.600 | 0.643 | 0.1 | $V_{DDI}$ (HSIO) |
| POD12I | 1.14 | 1.2 | 1.26 | 0.787 | 0.840 | 0.895 | 0.1 | $V_{DDI}$ (HSIO) |
| POD12II | 1.14 | 1.2 | 1.26 | 0.787 | 0.840 | 0.895 | 0.1 | $V_{DDI}$ (HSIO) |

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage.
3. $V_{ICM}$ rules are as follows:
   a. $V_{ICM}$ must be less than $V_{DDI} - 0.4$ V;
   b. $V_{ICM} + V_{ID}/2$ must be $<V_{DDI} + 0.4$ V;
   c. $V_{ICM} - V_{ID}/2$ must be $>VSS - 0.3$ V.

### Table 18 • Complementary Differential DC Output Levels

| I/O Standard | $V_{DDI}$ Min (V) | $V_{DDI}$ Typ (V) | $V_{DDI}$ Max (V) | $V_{OL}$ Min (V) | $V_{OL}$ Max (V) | $V_{OH}$[1,3] Min (V) | $I_{OL}$[2] Min (mA) | $I_{OH}$[2] Min (mA) |
|---|---|---|---|---|---|---|---|---|
| SSTL25I | 2.375 | 2.5 | 2.625 | | $V_{TT} - 0.608$ | $V_{TT} + 0.608$ | 8.1 | 8.1 |
| SSTL25II | 2.375 | 2.5 | 2.625 | | $V_{TT} - 0.810$ | $V_{TT} + 0.810$ | 16.2 | 16.2 |
| SSTL18I | 1.71 | 1.8 | 1.89 | | $V_{TT} - 0.603$ | $V_{TT} + 0.603$ | 6.7 | 6.7 |
| SSTL18II | 1.71 | 1.8 | 1.89 | | $V_{TT} - 0.603$ | $V_{TT} + 0.603$ | 13.4 | 13.4 |
| SSTL15I[4] | 1.425 | 1.5 | 1.575 | | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} - V_{OH})/40$ |
| SSTL15II[4] | 1.425 | 1.5 | 1.575 | | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/34$ | $(V_{DDI} - V_{OH})/34$ |
| SSTL135I[4] | 1.283 | 1.35 | 1.418 | | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} - V_{OH})/40$ |
| SSTL135II[4] | 1.283 | 1.35 | 1.418 | | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/34$ | $(V_{DDI} - V_{OH})/34$ |
| HSTL15I | 1.425 | 1.5 | 1.575 | | 0.4 | $V_{DDI} - 0.4$ | 8 | 8 |
| HSTL15II | 1.425 | 1.5 | 1.575 | | 0.4 | $V_{DDI} - 0.4$ | 16 | 16 |
| HSTL135I[4] | 1.283 | 1.35 | 1.418 | | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/50$ | $(V_{DDI} - V_{OH})/50$ |
| HSTL135II[4] | 1.283 | 1.35 | 1.418 | | $0.2 \times V_{DDI}$ | $0.8 \times V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} - V_{OH})/25$ |
| HSTL12I[4] | 1.14 | 1.2 | 1.26 | | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/50$ | $(V_{DDI} - V_{OH})/50$ |
| HSTL12II[4] | 1.14 | 1.2 | 1.26 | | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} - V_{OH})/25$ |
| HSUL18I[4] | 1.71 | 1.8 | 1.89 | | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/55$ | $(V_{DDI} - V_{OH})/55$ |
| HSUL18II[4] | 1.71 | 1.8 | 1.89 | | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/25$ | $(V_{DDI} - V_{OH})/25$ |
| HSUL12I[4] | 1.14 | 1.2 | 1.26 | | $0.1 \times V_{DDI}$ | $0.9 \times V_{DDI}$ | $V_{OL}/40$ | $(V_{DDI} - V_{OH})/40$ |
| POD12I[3,4] | 1.14 | 1.2 | 1.26 | | $0.5 \times V_{DDI}$ | | $V_{OL}/48$ | $(V_{DDI} - V_{OH})/48$ |
| POD12II[3,4] | 1.14 | 1.2 | 1.26 | | $0.5 \times V_{DDI}$ | | $V_{OL}/34$ | $(V_{DDI} - V_{OH})/34$ |

1. $V_{OH}$ is the single-ended high-output voltage.
2. The total DC sink/source current of all IOs within a lane is limited as follows:
    a. HSIO lane: 120 mA per 12 IO buffers.
    b. GPIO lane: 160 mA per 12 IO buffers
3. $V_{OH\_MAX}$ based on external pull-up termination (pseudo-open drain).
4. $I_{OL}/I_{OH}$ units for impedance standards in amps (not mA).

## 6.3.4 HSIO On-Die Termination

The following tables lists the on-die termination calibration accuracy specifications for HSIO bank.

### Table 19 • Single-Ended Thevenin Termination (Internal Parallel Thevenin Termination)

| Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|
| −40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V/1.35 V/1.2 V |
| −40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| −40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| −20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| −20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| −20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| −20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| −20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5 V/1.35 V |
| −20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2 V |

| Min (%) | Typ | Max (%) | Unit | Condition |
|---------|-----|---------|------|-----------|
| −20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Thevenin impedance is calculated based on independent P and N as measured at 50% of $V_{DDI}$. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.

**Table 20 • Single-Ended Termination to VDDI (Internal Parallel Termination to VDDI)**

| Min (%) | Typ | Max (%) | Unit | Condition |
|---------|-----|---------|------|-----------|
| −20 | 34 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| −20 | 40 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| −20 | 48 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| −20 | 60 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| −20 | 80 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| −20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| −20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Measured at 80% of $V_{DDI}$.

**Table 21 • Single-Ended Termination to VSS (Internal Parallel Termination to VSS)**

| Min (%) | Typ | Max (%) | Unit | Condition |
|---------|-----|---------|------|-----------|
| −20 | 120 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| −20 | 240 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| −20 | 120 | 20 | Ω | $V_{DDI}$ = 1.2 V |
| −20 | 240 | 20 | Ω | $V_{DDI}$ = 1.2 V |

**Note:** Measured at 50% of $V_{DDI}$.

## 6.3.5 GPIO On-Die Termination

The following table lists the on-die termination calibration accuracy specifications for GPIO bank.

**Table 22 • On-Die Termination Calibration Accuracy Specifications for GPIO Bank**

| Parameter | Description | Min (%) | Typ | Max (%) | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential termination[1] | Internal differential termination | −20 | 100 | 20 | Ω | $V_{ICM}$ < 0.8 V [6] |
| | | −20 | 100 | 40 | Ω | 0.6 V < $V_{ICM}$ < 1.65 V [6] |
| | | −20 | 100 | 80 | Ω | 1.4 V < $V_{ICM}$ [6] |
| Single-ended thevenin termination[2, 3] | Internal parallel thevenin termination | −40 | 50 | 20 | Ω | $V_{DDI}$ = 1.8 V/1.5 V |
| | | −40 | 75 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| | | −40 | 150 | 20 | Ω | $V_{DDI}$ = 1.8 V |
| | | −20 | 20 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | −20 | 30 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | −20 | 40 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | −20 | 60 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| | | −20 | 120 | 20 | Ω | $V_{DDI}$ = 1.5 V |
| Single-ended termination to $V_{SS}$[4, 5] | Internal parallel termination to $V_{SS}$ | −20 | 120 | 20 | Ω | $V_{DDI}$ = 2.5 V/1.8 V/1.5 V/1.2 V |
| | | −20 | 240 | 20 | Ω | $V_{DDI}$ = 2.5 V/1.8 V/1.5 V/1.2 V |

1. Measured across P to N with 400 mV bias.
2. Thevenin impedance is calculated based on independent P and N as measured at 50% of $V_{DDI}$.
3. For 50 Ω/75 Ω/150 Ω cases, nearest supported values of 40 Ω/60 Ω/120 Ω are used.
4. Measured at 50% of $V_{DDI}$.
5. Supported terminations vary with the IO type regardless of $V_{DDI}$ nominal voltage. Refer to Libero for available combinations.
6. When $V_{ICM}$ complies with more than one range, use the maximum percentage tolerance of the two ranges.

# 7 AC Switching Characteristics

This section contains the AC switching characteristics of the PolarFire FPGA device.

## 7.1 I/O Standards Specifications

This section describes I/O delay measurement methodology, buffer speed, switching characteristics, digital latency, gearing training calibration, and maximum physical interface (PHY) rate for memory interface IP.

### 7.1.1 Input Delay Measurement Methodology Maximum PHY Rate for Memory Interface IP

The following table provides information about the methodology for input delay measurement.

Table 23 • Input Delay Measurement Methodology

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3,4] | $V_{REF}$[1,5] | Unit |
|---|---|---|---|---|---|---|---|---|
| PCI | PCIE 3.3 V | 0 | VDDI | | | VDDI/2 | | V |
| LVTTL | LVTTL 3.3 V | 0 | VDDI | | | VDDI/2 | | V |
| LVCMOS33 | LVCMOS 3.3 V | 0 | VDDI | | | VDDI/2 | | V |
| LVCMOS25 | LVCMOS 2.5 V | 0 | VDDI | | | VDDI/2 | | V |
| LVCMOS18 | LVCMOS 1.8 V | 0 | VDDI | | | VDDI/2 | | V |
| LVCMOS15 | LVCMOS 1.5 V | 0 | VDDI | | | VDDI/2 | | V |
| LVCMOS12 | LVCMOS 1.2 V | 0 | VDDI | | | VDDI/2 | | V |
| SSTL25I | SSTL 2.5 V Class I | $V_{REF}-0.5$ | $V_{REF}+0.5$ | | | $V_{REF}$ | 1.25 | V |
| SSTL25II | SSTL 2.5 V Class II | $V_{REF}-0.5$ | $V_{REF}+0.5$ | | | $V_{REF}$ | 1.25 | V |
| SSTL18I | SSTL 1.8 V Class I | $V_{REF}-0.5$ | $V_{REF}+0.5$ | | | $V_{REF}$ | 0.90 | V |
| SSTL18II | SSTL 1.8 V Class II | $V_{REF}-0.5$ | $V_{REF}+0.5$ | | | $V_{REF}$ | 0.90 | V |
| SSTL15I | SSTL 1.5 V Class I | $V_{REF}-.175$ | $V_{REF}+.175$ | | | $V_{REF}$ | 0.75 | V |
| SSTL15II | SSTL 1.5 V Class II | $V_{REF}-.175$ | $V_{REF}+.175$ | | | $V_{REF}$ | 0.75 | V |
| SSTL135I | SSTL 1.35 V Class I | $V_{REF}-.16$ | $V_{REF}+.16$ | | | $V_{REF}$ | 0.675 | V |
| SSTL135II | SSTL 1.35 V Class II | $V_{REF}-.16$ | $V_{REF}+.16$ | | | $V_{REF}$ | 0.675 | V |
| HSTL15I | HSTL 1.5 V Class I | $V_{REF}-.5$ | $V_{REF}+.5$ | | | $V_{REF}$ | 0.75 | V |
| HSTL15II | HSTL 1.5 V Class II | $V_{REF}-.5$ | $V_{REF}+.5$ | | | $V_{REF}$ | 0.75 | V |
| HSTL135I | HSTL 1.35 V Class I | $V_{REF}-.45$ | $V_{REF}+.45$ | | | $V_{REF}$ | 0.675 | V |
| HSTL135II | HSTL 1.35 V Class II | $V_{REF}-.45$ | $V_{REF}+.45$ | | | $V_{REF}$ | 0.675 | V |
| HSTL12I | HSTL 1.2 V Class I | $V_{REF}-.4$ | $V_{REF}+.4$ | | | $V_{REF}$ | 0.60 | V |

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3, 4] | $V_{REF}$[1, 5] | Unit |
|---|---|---|---|---|---|---|---|---|
| HSTL12II | HSTL 1.2 V Class II | $V_{REF}$ − .4 | $V_{REF}$ + .4 | | | $V_{REF}$ | 0.60 | V |
| HSUL18I | HSUL 1.8 V Class I | $V_{REF}$ − .54 | $V_{REF}$ + .54 | | | $V_{REF}$ | 0.90 | V |
| HSUL18II | HSUL 1.8 V Class II | $V_{REF}$ − .54 | $V_{REF}$ + 0.54 | | | $V_{REF}$ | 0.90 | V |
| HSUL12I | HSUL 1.2 V | $V_{REF}$ − .22 | $V_{REF}$ + .22 | | | $V_{REF}$ | 0.60 | V |
| POD12I | Pseudo open drain (POD) logic 1.2 V Class I | $V_{REF}$ − .15 | $V_{REF}$ + .15 | | | $V_{REF}$ | 0.84 | V |
| POD12II | POD 1.2 V Class II | $V_{REF}$ − .15 | $V_{REF}$ + .15 | | | $V_{REF}$ | 0.84 | V |
| LVDS33 | Low-voltage differential signaling (LVDS) 3.3 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LVDS25 | LVDS 2.5 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LVDS18 | LVDS 1.8 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LCMDS33 | Low-common mode differential signaling (LCMDS) 3.3 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LCMDS25 | LCMDS 2.5 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| LCMDS18 | LCMDS 1.8 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| RSDS33 | RSDS 3.3 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| RSDS25 | RSDS 2.5 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| RSDS18 | RSDS 1.8 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS33 | Mini-LVDS 3.3 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS25 | Mini-LVDS 2.5 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| MINILVDS18 | Mini-LVDS 1.8 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 1.250 | 0 | | V |
| SUBLVDS33 | Sub-LVDS 3.3 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| SUBLVDS25 | Sub-LVDS 2.5 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| SUBLVDS18 | Sub-LVDS 1.8 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 0.900 | 0 | | V |
| PPDS33 | Point-to-point differential signaling 3.3 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| PPDS25 | PPDS 2.5 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |
| PPDS18 | PPDS 1.8 V | $V_{ICM}$ − .125 | $V_{ICM}$ + .125 | 0.250 | 0.800 | 0 | | V |

| Standard | Description | $V_L{}^1$ | $V_H{}^1$ | $V_{ID}{}^2$ | $V_{ICM}{}^2$ | $V_{MEAS}{}^{3, 4}$ | $V_{REF}{}^{1, 5}$ | Unit |
|---|---|---|---|---|---|---|---|---|
| SLVS33 | Scalable low-voltage signaling 3.3 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.200 | 0 | | V |
| SLVS25 | SLVS 2.5 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.200 | 0 | | V |
| SLVS18 | SLVS 1.8 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.200 | 0 | | V |
| HCSL33 | High-speed current steering logic (HCSL) 3.3 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.350 | 0 | | V |
| HCSL25 | HCSL 2.5 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.350 | 0 | | V |
| HCSL18 | HCSL 1.8 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.350 | 0 | | V |
| BLVDSE25[6] | Bus LVDS 2.5 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 1.250 | 0 | | V |
| MLVDSE25[6] | Multipoint LVDS 2.5 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 1.250 | 0 | | V |
| LVPECL33 | Low-voltage positive emitter coupled logic | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 1.650 | 0 | | V |
| LVPECLE33[6] | Low-voltage positive emitter coupled logic | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 1.650 | 0 | | V |
| SSTL25I | Differential SSTL 2.5 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 1.250 | 0 | | V |
| SSTL25II | Differential SSTL 2.5 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 1.250 | 0 | | V |
| SSTL18I | Differential SSTL 1.8 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.900 | 0 | | V |
| SSTL18II | Differential SSTL 1.8 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.900 | 0 | | V |
| SSTL15 I | Differential SSTL 1.5 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.750 | 0 | | V |
| SSTL15II | Differential SSTL 1.5 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.750 | 0 | | V |
| SSTL135I | Differential SSTL 1.35 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.675 | 0 | | V |
| SSTL135II | Differential SSTL 1.35 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.675 | 0 | | V |
| HSTL15I | Differential HSTL 1.5 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.750 | 0 | | V |
| HSTL15II | Differential HSTL 1.5 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.750 | 0 | | V |
| HSTL135I | Differential HSTL 1.35 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.675 | 0 | | V |
| HSTL135II | Differential HSTL 1.35 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.675 | 0 | | V |

| Standard | Description | $V_L$[1] | $V_H$[1] | $V_{ID}$[2] | $V_{ICM}$[2] | $V_{MEAS}$[3,4] | $V_{REF}$[1,5] | Unit |
|---|---|---|---|---|---|---|---|---|
| HSTL12I | Differential HSTL 1.2 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.600 | 0 | | V |
| HSTL12II | Differential HSTL 1.2 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.600 | 0 | | V |
| HSUL18I | Differential HSUL 1.8 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.900 | 0 | | V |
| HSUL18II | Differential HSUL 1.8 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.900 | 0 | | V |
| HSUL12I | Differential HSUL 1.2 V | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.600 | 0 | | V |
| POD12I | Differential POD 1.2 V Class I | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.840 | 0 | | V |
| POD12II | Differential POD 1.2 V Class II | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.840 | 0 | | V |
| MIPI25 | Mobile Industry Processor Interface | $V_{ICM} - .125$ | $V_{ICM} + .125$ | 0.250 | 0.200 | 0 | | V |

1. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst-case of these measurements. $V_{REF}$ values listed are typical. Input waveform switches between $V_L$ and $V_H$. All rise and fall times must be 1 V/ns.
2. Differential receiver standards all use 250 mV $V_{ID}$ for timing. $V_{CM}$ is different between different standards.
3. Input voltage level from which measurement starts.
4. The value given is the differential input voltage.
5. This is an input voltage reference that bears no relation to the $V_{REF}$/$V_{MEAS}$ parameters found in IBIS models or shown in Output Delay Measurement—Single-Ended Test Setup (see page 26).
6. Emulated bidirectional interface.

## 7.1.2 Output Delay Measurement Methodology
The following section provides information about the methodology for output delay measurement.

Table 24 • Output Delay Measurement Methodology

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| PCI | PCIE 3.3 V | 25 | 10 | 1.65 | |
| LVTTL | LVTTL 3.3 V | 1M | 0 | 1.65 | |
| LVCMOS33 | LVCMOS 3.3 V | 1M | 0 | 1.65 | |
| LVCMOS25 | LVCMOS 2.5 V | 1M | 0 | 1.25 | |
| LVCMOS18 | LVCMOS 1.8 V | 1M | 0 | 0.90 | |
| LVCMOS15 | LVCMOS 1.5 V | 1M | 0 | 0.75 | |
| LVCMOS12 | LVCMOS 1.2 V | 1M | 0 | 0.60 | |
| SSTL25I | Stub-series terminated logic 2.5 V Class I | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL25II | SSTL 2.5 V Class II | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL18I | SSTL 1.8 V Class I | 50 | 0 | $V_{REF}$ | 0.9 |

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| SSTL18II | SSTL 1.8 V Class II | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL15I | SSTL 1.5 V Class I | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL15II | SSTL 1.5 V Class II | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL135I | SSTL 1.35 V Class I | 50 | 0 | $V_{REF}$ | 0.675 |
| SSTL135II | SSTL 1.35 V Class II | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL15I | High-speed transceiver logic (HSTL) 1.5 V Class I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL15II | HSTL 1.5 V Class II | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL135I | HSTL 1.35 V Class I | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL135II | HSTL 1.35 V Class II | 50 | 0 | $V_{REF}$ | 0.675 |
| HSTL12I | HSTL 1.2 V Class I | 50 | 0 | $V_{REF}$ | 0.6 |
| HSTL12II | HSTL 1.2 V Class II | 50 | 0 | $V_{REF}$ | 0.6 |
| HSUL18I | High-speed unterminated logic 1.8 V Class I | 50 | 0 | $V_{REF}$ | 0.9 |
| HSUL18II | HSUL 1.8 V Class II | 50 | 0 | $V_{REF}$ | 0.9 |
| HSUL12I | HSUL 1.2 V Class I | 50 | 0 | $V_{REF}$ | 0.6 |
| POD12I | Pseudo open drain (POD) logic 1.2 V Class I | 50 | 0 | $V_{REF}$ | 0.84 |
| POD12II | POD 1.2 V Class II | 50 | 0 | $V_{REF}$ | 0.84 |
| LVDS33 | LVDS 3.3 V | 100 | 0 | $0^1$ | 0 |
| LVDS25 | LVDS 2.5 V | 100 | 0 | $0^1$ | 0 |
| LCMDS33 | Low-common mode differential signaling (LCMDS) 3.3 V | 100 | 0 | $0^1$ | 0 |
| LCMDS25 | LCMDS 2.5 V | 100 | 0 | 0 | 0 |
| RSDS33 | Reduced swing differential signaling 3.3 V | 100 | 0 | $0^1$ | 0 |
| RSDS25 | RSDS 2.5 V | 100 | 0 | $0^1$ | 0 |
| MINILVDS33 | Mini-LVDS 3.3 V | 100 | 0 | $0^1$ | 0 |
| MINILVDS25 | Mini-LVDS 2.5 V | 100 | 0 | $0^1$ | 0 |
| SUBLVDS33 | Sub-LVDS 3.3 V | 100 | 0 | $0^1$ | 0 |
| SUBLVDS25 | Sub-LVDS 2.5 V | 100 | 0 | $0^1$ | 0 |
| PPDS33 | Point-to-point differential signaling 3.3 V | 100 | 0 | $0^1$ | 0 |
| PPDS25 | PPDS 2.5 V | 100 | 0 | $0^1$ | 0 |
| SLVS33 | Scalable low-voltage signaling 3.3 V | 100 | 0 | $0^1$ | 0 |
| SLVS25 | SLVS 2.5 V | 100 | 0 | $0^1$ | 0 |
| SLVSE15 | SLVS 1.5 V | 100 | 0 | $0^1$ | 0 |
| HCSL33 | High-speed current steering logic 3.3 V | 100 | 0 | $0^1$ | 0 |
| HCSL25 | HCSL 2.5 V | 100 | 0 | $0^1$ | 0 |
| BUSLVDSE25 | Bus LVDS | 100 | 0 | $0^1$ | 0 |
| MLVDSE25 | Multipoint LVDS 2.5 V | 100 | 0 | $0^1$ | 0 |
| LVPECLE33 | Low-voltage positive emitter-coupled logic | 100 | 0 | $0^1$ | 0 |
| MIPIE25 | Mobile industry processor interface 2.5 V | 100 | 0 | $0^1$ | 0 |
| SSTL25I | Differential SSTL 2.5 V Class I | 50 | 0 | $0^1$ | 0 |
| SSTL25II | Differential SSTL 2.5 V Class II | 50 | 0 | $0^1$ | 0 |

| Standard | Description | $R_{REF}$ (Ω) | $C_{REF}$ (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| SSTL18I | Differential SSTL 1.8 V Class I | 50 | 0 | $0^1$ | 0 |
| SSTL18II | Differential SSTL 1.8 V Class II | 50 | 0 | $0^1$ | 0 |
| SSTL15I | Differential SSTL 1.5 V Class I | 50 | 0 | $0^1$ | 0 |
| SSTL15II | Differential SSTL 1.5 V Class II | 50 | 0 | $0^1$ | 0 |
| SSTL135I | Differential SSTL 1.35 V Class I | 50 | 0 | $0^1$ | 0 |
| SSTL135II | Differential SSTL 1.35 V Class II | 50 | 0 | $0^1$ | 0 |
| HSTL15I | Differential HSTL 1.5 V Class I | 50 | 0 | $0^1$ | 0 |
| HSTL15II | Differential HSTL 1.5 V Class II | 50 | 0 | $0^1$ | 0 |
| HSTL135I | Differential HSTL 1.35 V Class I | 50 | 0 | $0^1$ | 0 |
| HSTL135II | Differential HSTL 1.35 V Class II | 50 | 0 | $0^1$ | 0 |
| HSTL12I | Differential HSTL 1.2 V Class I | 50 | 0 | $0^1$ | 0 |
| HSTL12II | Differential HSTL 1.2 V Class II | 50 | 0 | $0^1$ | 0 |
| HSUL18I | Differential HSUL 1.8 V Class I | 50 | 0 | $0^1$ | 0 |
| HSUL18II | Differential HSUL 1.8 V Class II | 50 | 0 | $0^1$ | 0 |
| HSUL12I | Differential HSUL 1.2 V Class I | 50 | 0 | $0^1$ | 0 |
| POD12I | Differential POD 1.2 V Class II | 50 | 0 | $0^1$ | 0 |
| POD12II | Differential POD 1.2 V Class II | 50 | 0 | $0^1$ | 0 |

1. The value given is the differential output voltage.

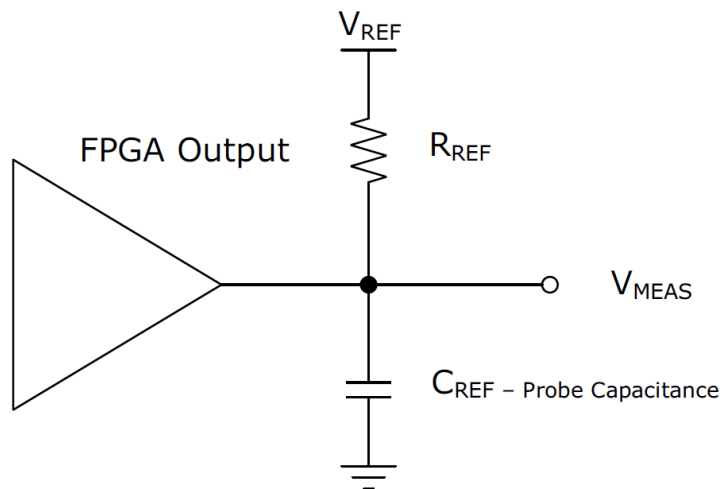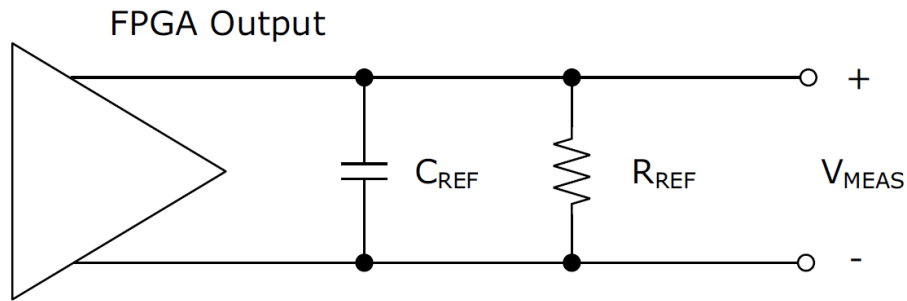**Figure 1 • Output Delay Measurement—Single-Ended Test Setup**

**Figure 2 • Output Delay Measurement—Differential Test Setup**



## 7.1.3 Input Buffer Speed
The following tables provide information about input buffer speed.

**Table 25 • HSIO Maximum Input Buffer Speed**

| Standard | STD | −1 | Unit |
|---|---|---|---|
| LVDS18 | 1250 | 1250 | Mbps |
| LCMDS18 | 1250 | 1250 | Mbps |
| HCSL18 | 800 | 800 | Mbps |
| RSDS18 | 800 | 800 | Mbps |
| MINILVDS18 | 800 | 800 | Mbps |
| SUBLVDS18 | 800 | 800 | Mbps |
| PPDS18 | 800 | 800 | Mbps |
| SLVS18 | 800 | 800 | Mbps |
| SSTL18I | 800 | 1066 | Mbps |
| SSTL18II | 800 | 1066 | Mbps |
| SSTL15I | 1066 | 1333 | Mbps |
| SSTL15II | 1066 | 1333 | Mbps |
| SSTL135I | 1066 | 1333 | Mbps |
| SSTL135II | 1066 | 1333 | Mbps |
| HSTL15I | 900 | 1100 | Mbps |
| HSTL15II | 900 | 1100 | Mbps |
| HSTL135I | 1066 | 1066 | Mbps |
| HSTL135II | 1066 | 1066 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL12I | 1066 | 1333 | Mbps |
| HSTL12I | 1066 | 1266 | Mbps |
| HSTL12II | 1066 | 1266 | Mbps |
| POD12I | 1333 | 1600 | Mbps |
| POD12II | 1333 | 1600 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |

| Standard | STD | −1 | Unit |
|---|---|---|---|
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |
| LVCMOS12 (8 mA) | 300 | 300 | Mbps |

1. Performance is achieved with $V_{ID}$ ≥200 mV.

**Table 26 • GPIO Maximum Input Buffer Speed**

| Standard | STD | −1 | Unit |
|---|---|---|---|
| LVDS25/LVDS33/LCMDS25/LCMDS33 | 1250 | 1600 | Mbps |
| RSDS25/RSDS33 | 800 | 800 | Mbps |
| MINILVDS25/MINILVDS33 | 800 | 800 | Mbps |
| SUBLVDS25/SUBLVDS33 | 800 | 800 | Mbps |
| PPDS25/PPDS33 | 800 | 800 | Mbps |
| SLVS25/SLVS33 | 800 | 800 | Mbps |
| SLVSE15 | 800 | 800 | Mbps |
| HCSL25/HCSL33 | 800 | 800 | Mbps |
| BUSLVDSE25 | 800 | 800 | Mbps |
| MLVDSE25 | 800 | 800 | Mbps |
| LVPECL33 | 800 | 800 | Mbps |
| SSTL25I | 800 | 800 | Mbps |
| SSTL25II | 800 | 800 | Mbps |
| SSTL18I | 800 | 800 | Mbps |
| SSTL18II | 800 | 800 | Mbps |
| SSTL15I | 800 | 1066 | Mbps |
| SSTL15II | 800 | 1066 | Mbps |
| HSTL15I | 800 | 900 | Mbps |
| HSTL15II | 800 | 900 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| PCI | 500 | 500 | Mbps |
| LVTTL | 500 | 500 | Mbps |
| LVCMOS33 | 500 | 500 | Mbps |
| LVCMOS25 | 500 | 500 | Mbps |
| LVCMOS18 | 500 | 500 | Mbps |
| LVCMOS15 | 500 | 500 | Mbps |
| LVCMOS12 | 300 | 300 | Mbps |
| MIPI25 | | | Mbps |

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with $V_{ID}$ ≥200 mV.

## 7.1.4        Output Buffer Speed

**Table 27 • HSIO Maximum Output Buffer Speed**

| Standard | STD | –1 | Unit |
|---|---|---|---|
| SSTL18I | 800 | 1066 | Mbps |
| SSTL18II | 800 | 1066 | Mbps |
| SSTL18I (differential) | 800 | 1066 | Mbps |
| SSTL18II (differential) | 800 | 1066 | Mbps |
| SSTL15I | 1066 | 1333 | Mbps |
| SSTL15II | 1066 | 1333 | Mbps |
| SSTL15I (differential) | 1066 | 1333 | Mbps |
| SSTL15II (differential) | 1066 | 1333 | Mbps |
| SSTL135I | 1066 | 1333 | Mbps |
| SSTL135II | 1066 | 1333 | Mbps |
| SSTL135I (differential) | 1066 | 1333 | Mbps |
| SSTL135II (differential) | 1066 | 1333 | Mbps |
| HSTL15I | 900 | 1100 | Mbps |
| HSTL15II | 900 | 1100 | Mbps |
| HSTL15I (differential) | 900 | 1100 | Mbps |
| HSTL15II (differential) | 900 | 1100 | Mbps |
| HSTL135I | 1066 | 1066 | Mbps |
| HSTL135II | 1066 | 1066 | Mbps |
| HSTL135I (differential) | 1066 | 1066 | Mbps |
| HSTL135II (differential) | 1066 | 1066 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL18I (differential) | 400 | 400 | Mbps |
| HSUL18II (differential) | 400 | 400 | Mbps |
| HSUL12I | 1066 | 1333 | Mbps |
| HSUL12I (differential) | 1066 | 1333 | Mbps |
| HSTL12I | 1066 | 1266 | Mbps |
| HSTL12II | 1066 | 1266 | Mbps |
| HSTL12I (differential) | 1066 | 1266 | Mbps |
| HSTL12II (differential) | 1066 | 1266 | Mbps |
| POD12I | 1333 | 1600 | Mbps |
| POD12II | 1333 | 1600 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |
| LVCMOS12 (8 mA) | 250 | 300 | Mbps |

**Table 28 • GPIO Maximum Output Buffer Speed**

| Standard | STD | –1 | Unit |
|---|---|---|---|
| LVDS25/LCMDS25 | 1250 | 1250 | Mbps |
| LVDS33/LCMDS33 | 1250 | 1600 | Mbps |
| RSDS25 | 800 | 800 | Mbps |
| MINILVDS25 | 800 | 800 | Mbps |
| SUBLVDS25 | 800 | 800 | Mbps |
| PPDS25 | 800 | 800 | Mbps |
| SLVSE15 | 500 | 500 | Mbps |
| BUSLVDSE25 | 500 | 500 | Mbps |
| MLVDSE25 | 500 | 500 | Mbps |
| LVPECLE33 | 500 | 500 | Mbps |
| SSTL25I | 800 | 800 | Mbps |
| SSTL25II | 800 | 800 | Mbps |
| SSTL25I (differential) | 800 | 800 | Mbps |
| SSTL25II (differential) | 800 | 800 | Mbps |
| SSTL18I | 800 | 800 | Mbps |
| SSTL18II | 800 | 800 | Mbps |
| SSTL18I (differential) | 800 | 800 | Mbps |
| SSTL18II (differential) | 800 | 800 | Mbps |
| SSTL15I | 800 | 1066 | Mbps |
| SSTL15II | 800 | 1066 | Mbps |
| SSTL15I (differential) | 800 | 1066 | Mbps |
| SSTL15II (differential) | 800 | 1066 | Mbps |
| HSTL15I | 900 | 900 | Mbps |
| HSTL15II | 900 | 900 | Mbps |
| HSTL15I (differential) | 900 | 900 | Mbps |
| HSTL15II (differential) | 900 | 900 | Mbps |
| HSUL18I | 400 | 400 | Mbps |
| HSUL18II | 400 | 400 | Mbps |
| HSUL18I (differential) | 400 | 400 | Mbps |
| HSUL18II (differential) | 400 | 400 | Mbps |
| PCI | 500 | 500 | Mbps |
| LVTTL (20 mA) | 500 | 500 | Mbps |
| LVCMOS33 (20 mA) | 500 | 500 | Mbps |
| LVCMOS25 (16 mA) | 500 | 500 | Mbps |
| LVCMOS18 (12 mA) | 500 | 500 | Mbps |
| LVCMOS15 (10 mA) | 500 | 500 | Mbps |
| LVCMOS12 (8 mA) | 250 | 300 | Mbps |
| MIPIE25 | | | Mbps |

### 7.1.5 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

**Table 29 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks**

| Memory Standard | Gearing Ratio | V$_{DDAUX}$ | V$_{DDI}$ | STD (Mbps) | −1 (Mbps) | Fabric STD (MHz) | Fabric −1 (MHz) |
|---|---|---|---|---|---|---|---|
| DDR4 | 8:1 | 1.8 V | 1.2 V | 1333 | 1600 | 167 | 200 |
| DDR3 | 8:1 | 1.8 V | 1.5 V | 1067 | 1333 | 133 | 167 |
| DDR3L | 8:1 | 1.8 V | 1.35 V | 1067 | 1333 | 133 | 167 |
| LPDDR3 | 8:1 | 1.8 V | 1.2 V | 800 | 1333 | 133 | 167 |
| QDRII+ | 8:1 | 1.8 V | 1.5 V | 900 | 1100 | 112.5 | 137.5 |
| RLDRAM3[1] | 8:1 | 1.8 V | 1.35 V | 1067 | 1067 | 133 | 133 |
| RLDRAM3[1] | 4:1 | 1.8 V | 1.35 V | 667 | 800 | 167 | 200 |
| RLDRAM3[1] | 2:1 | 1.8 V | 1.35 V | 333 | 400 | 167 | 200 |
| RLDRAMII [1] | 8:1 | 1.8 V | 1.8 V | 800 | 1067 | 100 | 133 |
| RLDRAMII [1] | 4:1 | 1.8 V | 1.8 V | 667 | 800 | 167 | 200 |
| RLDRAMII [1] | 2:1 | 1.8 V | 1.8 V | 333 | 400 | 167 | 200 |

1. Simulation data only. RLDRAMII and RLDRAM3 are not supported with a soft IP controller currently.

**Table 30 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks**

| Memory Standard | Gearing Ratio | V$_{DDAUX}$ | V$_{DDI}$ | STD (Mbps) | −1 (Mbps) | Fabric STD (MHz) | Fabric −1 (MHz) |
|---|---|---|---|---|---|---|---|
| DDR3 | 8:1 | 2.5 V | 1.5 V | 800 | 1067 | 100 | 133 |
| QDRII+ | 8:1 | 2.5 V | 1.5 V | 900 | 900 | 113 | 113 |
| RLDRAMII [1] | 4:1 | 2.5 V | 1.8 V | 800 | 800 | 200 | 200 |
| RLDRAMII [1] | 2:1 | 2.5 V | 1.8 V | 400 | 400 | 200 | 200 |

1. Simulation data only. RLDRAMII is currently not supported with a soft IP controller.

## 7.1.6 User I/O Switching Characteristics

The following section describes characteristics for user I/O switching. For more information about user I/O timing, see the *PolarFire I/O Timing Spreadsheet* (to be released).

### 7.1.6.1 I/O Digital

The following tables provide information about I/O digital.

#### Table 31 • I/O Digital Receive Single-Data Rate Switching Characteristics

| Parameter | Interface Name | Topology | IO Type | STD (MHz) | −1 (MHz) | STD (Mbps) | −1 (Mbps) | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|
| Input F$_{MAX}$ | RX_SDR_G_A | Rx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, aligned |
| Input F$_{MAX}$ | RX_SDR_R_A | Rx SDR | HSIO, GPIO | 250 | 250 | 250 | 250 | From a regional clock source, aligned |
| Input F$_{MAX}$ | RX_SDR_G_C | Rx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, centered |
| Input F$_{MAX}$ | RX_SDR_R_C | Rx SDR | HSIO, GPIO | 250 | 250 | 250 | 250 | From a regional clock source, centered |

#### Table 32 • I/O Digital Receive Double-Data Rate Switching Characteristics

| Parameter | Interface Name | Topology | IO Type | STD (MHz) | −1 (MHz) | STD (Mbps) | −1 (Mbps) | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|
| Input F$_{MAX}$ | RX_DDR_G_A | Rx DDR | HSIO | 335 | 345 | 670 | 690 | From a global clock source, aligned |
| | | | GPIO | 310 | 325 | 620 | 650 | |
| Input F$_{MAX}$ | RX_DDR_R_A | Rx DDR | HSIO | 250 | 250 | 500 | 500 | From a regional clock source, aligned |
| | | | GPIO | 250 | 250 | 500 | 500 | |
| Input F$_{MAX}$ | RX_DDR_G_C | Rx DDR | HSIO | 335 | 345 | 670 | 690 | From a global clock source, centered |
| | | | GPIO | 310 | 325 | 620 | 650 | |
| Input F$_{MAX}$ | RX_DDR_R_C | Rx DDR | HSIO | 250 | 250 | 500 | 500 | From a regional clock source, centered |
| | | | GPIO | 250 | 250 | 500 | 500 | |
| Input F$_{MAX}$ 2:1 | RX_DDRX_B_G_A | Rx DDR digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, aligned, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |
| Input F$_{MAX}$ 4:1 | RX_DDRX_B_G_A | Rx DDR digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, aligned, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |
| Input F$_{MAX}$ 2:1 | RX_DDRX_B_G_C | Rx DDR digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, centered, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |
| Input F$_{MAX}$ 4:1 | RX_DDRX_B_G_C | Rx DDR digital mode | HSIO | 350 | 350 | 700 | 700 | From a HS_IO_CLK clock source, centered, global fabric clock |
| | | | GPIO | 300 | 310 | 600 | 620 | |

| Parameter | Interface Name | Topology | IO Type | STD (MHz) | −1 (MHz) | STD (Mbps) | −1 (Mbps) | Clock-to-Data Condition |
|---|---|---|---|---|---|---|---|---|
| Input F$_{MAX}$ 4:1 | RX_DDRX_B_G_C_MIPI | Rx DDR digital mode for MIPI | GPIO | | | | | From a HS_IO_CLK clock source, centered, global fabric clock |
| Input F$_{MAX}$ 2:1 | RX_DDRX_B_R_A | Rx DDR digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, aligned, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |
| Input F$_{MAX}$ 4:1 | RX_DDRX_B_R_A | Rx DDR digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, aligned, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |
| Input F$_{MAX}$ 2:1 | RX_DDRX_B_R_C | Rx DDR digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, centered, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |
| Input F$_{MAX}$ 4:1 | RX_DDRX_B_R_C | Rx DDR digital mode | HSIO | 220 | 270 | 440 | 540 | From a HS_IO_CLK clock source, centered, regional fabric clock |
| | | | GPIO | 205 | 250 | 410 | 500 | |

**Table 33 • I/O Digital Transmit Single-Data Rate Switching Characteristics**

| Parameter | Interface Name | Topology | IO Type | STD (MHz) | −1 (MHz) | STD (Mbps) | −1 (Mbps) | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|
| Output F$_{MAX}$ | TX_SDR_G_A | Tx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, aligned[1] |
| | TX_SDR_G_C | Tx SDR | HSIO, GPIO | 500 | 500 | 500 | 500 | From a global clock source, centered[1] |

1. A centered clock-to-data interface can be created with a negedge launch of the data.

**Table 34 • I/O Digital Transmit Double-Data Rate Switching Characteristics**

| Parameter | Interface Name | Topology | IO Type | STD (MHz) | −1 (MHz) | STD (Mbps) | −1 (Mbps) | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|
| Output F$_{MAX}$ | TX_DDR_G_A | Tx DDR | HSIO, GPIO | 500 | 500 | 1000 | 1000 | From a global clock source, aligned |
| | TX_DDR_G_C | Tx DDR | HSIO, GPIO | 500 | 500 | 1000 | 1000 | From a global clock source, centered |
| Output F$_{MAX}$ 2:1 | TX_DDRX _B_A | Tx DDR digital mode | HSIO | 667 | 800 | 1333 | 1600 | From a HS_IO_CLK clock source, aligned |
| Output F$_{MAX}$ 4:1 | TX_DDRX_B_A | Tx DDR digital mode | HSIO | 667 | 800 | 1333 | 1600 | From a HS_IO_CLK clock source, aligned |
| Output F$_{MAX}$ 2:1 | TX_DDRX_B_C | Tx DDR digital mode | HSIO | 667 | 800 | 1333 | 1600 | From a HS_IO_CLK clock source, centered with PLL |

| Parameter | Interface Name | Topology | IO Type | STD (MHz) | −1 (MHz) | STD (Mbps) | −1 (Mbps) | Forwarded Clock-to-Data Skew |
|---|---|---|---|---|---|---|---|---|
| Output F$_{MAX}$ 4:1 | TX_DDRX_B_C | Tx DDR digital mode | HSIO | 667 | 800 | 1333 | 1600 | From a HS_IO_CLK clock source, centered with PLL |
| Output F$_{MAX}$ 2:1 | TX_DDRX_B_A | Tx DDR digital mode | GPIO | 625 | 800 | 1250 | 1600 | From a HS_IO_CLK clock source, aligned |
| Output F$_{MAX}$ 4:1 | TX_DDRX_B_A | Tx DDR digital mode | GPIO | 625 | 800 | 1250 | 1600 | From a HS_IO_CLK clock source, aligned |
| Output F$_{MAX}$ 2:1 | TX_DDRX_B_C | Tx DDR digital mode | GPIO | 625 | 800 | 1250 | 1600 | From a HS_IO_CLK clock source, centered with PLL |
| Output F$_{MAX}$ 4:1 | TX_DDRX_B_C | Tx DDR digital mode | GPIO | 625 | 800 | 1250 | 1600 | From a HS_IO_CLK clock source, centered with PLL |
| Output F$_{MAX}$ 4:1 | TX_DDRX_B_C_ MIPI | Tx DDR digital mode for MIPI | GPIO | | | | | From a HS_IO_CLK clock source, centered with PLL |

**Table 35 • Programmable Delay**

| Parameter | STD Min | STD Typ | STD Max | −1 Min | −1 Typ | −1 Max | Unit |
|---|---|---|---|---|---|---|---|
| In delay, out delay, DLL delay step sizes | 12.7 | 30 | 35 | 12.7 | 25 | 29.5 | ps |

**Table 36 • I/O CDR Switching Characteristics**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Data rate | 266 | 1250 | Mbps |
| Receiver sinusoidal jitter tolerance | | | UI |

**Note:** See the LVDS output buffer specifications for transmit characteristics.

## 7.2    Clocking Specifications

This section describes the PLL and DLL clocking and oscillator specifications.

### 7.2.1    Clocking

The following table provides clocking specifications.

**Table 37 • Global and Regional Clock Characteristics (–40 °C to 100 °C)**

| Parameter | Symbol | $V_{DD}$ = 1.0 V STD | $V_{DD}$ = 1.0 V –1 | $V_{DD}$ = 1.05 V STD | $V_{DD}$ = 1.05 V –1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Global clock $F_{MAX}$ | $F_{MAXG}$ | 500 | 500 | 500 | 500 | MHz | |
| Regional clock $F_{MAX}$ | $F_{MAXR}$ | 375 | 375 | 375 | 375 | MHz | Transceiver interfaces only |
| | $F_{MAXR}$ | 250 | 250 | 250 | 250 | MHz | All other interfaces |
| Global clock duty cycle distortion | $T_{DCDG}$ | 190 | 190 | 190 | 190 | ps | At 500 MHz |
| Regional clock duty cycle distortion | $T_{DCDR}$ | 120 | 120 | 120 | 120 | ps | At 250 MHz |

The following table provides clocking specifications from –40 °C to 100 °C.

**Table 38 • High-Speed I/O Clock Characteristics (–40 °C to 100 °C)**

| Parameter | Symbol | $V_{DD}$ = 1.0 V STD | $V_{DD}$ = 1.0 V –1 | $V_{DD}$ = 1.05 V STD | $V_{DD}$ = 1.05 V –1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| High-speed I/O clock $F_{MAX}$ | $F_{MAXB}$ | 1000 | 1250 | 1000 | 1250 | MHz | HSIO and GPIO |
| High-speed I/O clock skew[1] | $F_{SKEWB}$ | 30 | 20 | 30 | 20 | ps | HSIO without bridging |
| | $F_{SKEWB}$ | 600 | 500 | 600 | 500 | ps | HSIO with bridging |
| | $F_{SKEWB}$ | 45 | 35 | 45 | 35 | ps | GPIO without bridging |
| | $F_{SKEWB}$ | 75 | 60 | 75 | 60 | ps | GPIO with bridging |
| High-speed I/O clock duty cycle distortion[2] | $T_{DCB}$ | 90 | 90 | 90 | 90 | ps | HSIO without bridging |
| | $T_{DCB}$ | 115 | 115 | 115 | 115 | ps | HSIO with bridging |
| | $T_{DCB}$ | 90 | 90 | 90 | 90 | ps | GPIO without bridging |
| | $T_{DCB}$ | 115 | 115 | 115 | 115 | ps | GPIO with bridging |

1. $F_{SKEWB}$ is the worst-case clock-tree skew observable between sequential I/O elements. Clock-tree skew is significantly smaller at I/O registers close to each other and fed by the same or adjacent clock-tree branches. Use the Microsemi Timing Analyzer tool to evaluate clock skew specific to the design.
2. Parameters listed in this table correspond to the worst-case duty cycle distortion observable at the I/O flip flops. IBIS should be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times for any I/O standard.

## 7.2.2 PLL

The following table provides information about PLL.

#### Table 39 • PLL Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Input clock frequency (integer mode) | $F_{INI}$ | 1 | | 1250 | MHz | |
| Input clock frequency (fractional mode) | $F_{INF}$ | 10 | | 1250 | MHz | |
| Minimum reference or feedback pulse width[1] | $F_{INPULSE}$ | 200 | | | ps | |
| Frequency at the Frequency Phase Detector (PFD) (integer mode) | $F_{PHDETI}$ | 1 | | 312 | MHz | |
| Frequency at the PFD (fractional mode) | $F_{PHDETF}$ | 10 | | 225 | MHz | |
| Allowable input duty cycle | $F_{INDUTY}$ | 25 | | 75 | % | |
| Maximum input period clock jitter (reference and feedback clocks)[2] | $F_{MAXINJ}$ | | 120 | 1000 | ps | |
| PLL VCO frequency | $F_{VCO}$ | 800 | | 5000 | MHz | |
| Loop bandwidth (Int)[3] | $F_{BW}$ | $F_{PHDET}/55$ | $F_{PHDET}/44$ | $F_{PHDET}/30$ | MHz | |
| Loop bandwidth (FRAC)[3] | $F_{BW}$ | $F_{PHDET}/91$ | $F_{PHDET}/77$ | $F_{PHDET}/56$ | MHz | |
| Static phase offset of the PLL outputs[4] | $T_{SPO}$ | | | Max (±60 ps, ±0.5 degrees) | ps | |
| PLL output period jitter[10] | $T_{OUTJITTER}$ | | | 0.025*output_period | ps | 1.5 MHz ≤ Fout < 15 MHz |
| | | | | 135 | ps | Fout ≥ 15 MHz |
| PLL output duty cycle precision | $T_{OUTDUTY}$ | 48 | | 54 | % | |
| PLL lock time[5] | $T_{LOCK}$ | | | Max (6.0 µs, 625 PFD cycles) | µs | |
| PLL unlock time[6] | $T_{UNLOCK}$ | 2 | | 8 | PFD cycles | |
| PLL output frequency | $F_{OUT}$ | 0.050 | | 1250 | MHz | |
| Minimum power-down pulse width | $T_{MPDPW}$ | 1 | | | µs | |
| Maximum delay in the feedback path[7] | $F_{MAXDFB}$ | | | 1.5 | PFD cycles | |
| Spread spectrum modulation spread[8] | Mod_Spread | 0.1 | | 3.1 | % | |
| Spread spectrum modulation frequency[9] | Mod_Freq | $F_{PHDETF}/(128\times63)$ | 32 | $F_{PHDETF}/(128)$ | KHz | |

1. Minimum time for high or low pulse width.
2. Maximum jitter the PLL can tolerate without losing lock.
3. Default bandwidth setting of BW_PROP_CTRL = "01" for Integer and Fraction modes leads to the typical estimated bandwidth. This bandwidth can be lowered by setting BW_PROP_CTRL = "00" and can be increased if BW_PROP_CTRL = "10" and will be at the highest value if BW_PROP_CTRL = "11".

4. Maximum (±3-Sigma) phase error between any two outputs with nominally aligned phases.
5. Input clock cycle is REFDIV/F$_{REF}$. For example, F$_{REF}$ = 25 MHz, REFDIV = 1, lock time = 10.0 (assumes LOCKCOUNTSEL setting = 4'd8 (256 cycles)).
6. Unlock occurs if two cycle slip within LOCKCOUNT/4 PFD cycles.
7. Maximum propagation delay of external feedback path in deskew mode.
8. Programmable capability for depth of down spread or center spread mod ulation.
9. Programmable modulation rate based on the modulation divider setting (1 to 63).
10. Period jitter is measured at the output of the device using HSUL12 output buffers and includes the jitter effects of the reference clock source, PLL, clock routing ne tworks, and output buffer. PLL is configured with internal feedback enabled and in integer mode. FPGA fabric is active during testing (75% utilization).

**Note**: In order to meet all data sheet specifications, the PLL must be programmed such that the PLL Loop Bandwidth < (0.0017 * VCO Frequency) – 0.4863 MHz. The Libero PLL configuration tool will enforce this rule when creating PLL configurations.

### 7.2.3 DLL

The following table provides information about DLL.

**Table 40 • DLL Electrical Characteristics**

| Parameter[1] | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input reference clock frequency | F$_{INF}$ | 133 | | 800 | MHz |
| Input feedback clock frequency | F$_{INFDBF}$ | 133 | | 800 | MHz |
| Primary output clock frequency | F$_{OUTPF}$ | 133 | | 800 | MHz |
| Secondary output clock frequency[2] | F$_{OUTSF}$ | 33.3 | | 800 | MHz |
| Input clock cycle-to-cycle jitter | F$_{INJ}$ | | | 200 | ps |
| Output clock cycle-to-cycle jitter (with clean input clock) | T$_{OUTJITTERCC}$ | | | Max (250 ps, 15% of clock period) | ps |
| Output clock period jitter (with clean input clock) | T$_{OUTJITTERP}$ | | | Max (300 ps, 20% of clock period) | ps |
| Output clock-to-clock skew between two outputs with the same phase settings | T$_{SKEW}$ | | | ±150 | ps |
| DLL lock time | T$_{LOCK}$ | 16 | | 16K | Reference clock cycles |
| Minimum reset pulse width | T$_{MRPW}$ | 3 | | | ns |
| Minimum input pulse width[3] | T$_{MIPW}$ | 20 | | | ns |
| Minimum input clock pulse width high | T$_{MPWH}$ | 400 | | | ps |
| Minimum input clock pulse width low | T$_{MPWL}$ | 400 | | | ps |
| Delay step size | T$_{DEL}$ | 12.7 | 30 | 35 | ps |
| Maximum delay block delay[4] | T$_{DELMAX}$ | 1.8 | | 4.8 | ns |
| Output clock duty cycle (with 50% duty cycle input)[5] | T$_{DUTY}$ | 40 | | 60 | % |
| Output clock duty cycle (with 50% duty cycle input)[6] | T$_{DUTY50}$ | 45 | | 55 | % |

1. For all DLL modes.
2. Secondary output clock divided by four option.
3. On load, direction, move, hold, and update input signals.
4. 128 delay taps in one delay block.
5. Without duty cycle correction enabled.
6. With dut y cycle correction enabled.

## 7.2.4 RC Oscillators

The following tables provide internal RC clock resources for user designs and additional information about designing systems with RF front end information about emitters generated on-chip to support programming operations.

**Table 41 • 2 MHz RC Oscillator Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating frequency | $RC_{2FREQ}$ | | 2 | | MHz |
| Accuracy | $RC_{2FACC}$ | −4 | | 4 | % |
| Duty cycle | $RC_{2DC}$ | 46 | | 54 | % |
| Peak-to-peak output period jitter | $RC_{2PJIT}$ | | 5 | 10 | ns |
| Peak-to-peak output cycle-to-cycle jitter | $RC_{2CJIT}$ | | 5 | 10 | ns |
| Operating current ($V_{DD25}$) | $RC_{2IVPPA}$ | | | 60 | µA |
| Operating current ($V_{DD}$) | $RC_{2IVDD}$ | | | 2.6 | µA |

**Table 42 • 160 MHz RC Oscillator Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating frequency | $RC_{SCFREQ}$ | | 160 | | MHz |
| Accuracy | $RC_{SCFACC}$ | −4 | | 4 | % |
| Duty cycle | $RC_{SCDC}$ | 47 | | 52 | % |
| Peak-to-peak output period jitter | $RC_{SCPJIT}$ | | | 600 | ps |
| Peak-to-peak output cycle-to-cycle jitter | $RC_{SCCJIT}$ | | | 172 | ps |
| Operating current ($V_{DD25}$) | $RC_{SCVPPA}$ | | | 599 | µA |
| Operating current ($V_{DD18}$) | $RC_{SCVPP}$ | | | 0.1 | µA |
| Operating current ($V_{DD}$) | $RC_{SCVDD}$ | | | 60.7 | µA |

## 7.3 Fabric Specifications

The following section describes specifications for the fabric.

### 7.3.1 Math Blocks

The following table lists the maximum operating frequency ($F_{MAX}$) of the math block in the extended commercial temperature range (0 °C to 100 °C).

**Table 43 • Math Block Performance Extended Commercial Range (0 °C to 100 °C)**

| Modes | $V_{DD}$ = 1.0 V – STD | $V_{DD}$ = 1.0 V – 1 | $V_{DD}$ = 1.05 V – STD | $V_{DD}$ = 1.05 V – 1 | Unit |
|---|---|---|---|---|---|
| 18 × 18 multiplication | 370 | 470 | 440 | 500 | MHz |
| 18 × 18 multiplication summed with 48-bit input | 370 | 470 | 440 | 500 | MHz |
| 18 × 19 multiplier pre-adder ROM mode | 365 | 465 | 435 | 500 | MHz |
| Two 9 × 9 multiplication | 370 | 470 | 440 | 500 | MHz |
| 9 × 9 dot product (DOTP) | 370 | 470 | 440 | 500 | MHz |
| Complex 18 × 19 multiplication | 360 | 455 | 430 | 500 | MHz |

The following table lists the maximum operating frequency ($F_{MAX}$) of the math block in the industrial temperature range (–40 °C to 100 °C).

**Table 44 • Math Block Performance Industrial Range (–40 °C to 100 °C)**

| Modes | $V_{DD}$ = 1.0 V – STD | $V_{DD}$ = 1.0 V – 1 | $V_{DD}$ = 1.05 V – STD | $V_{DD}$ = 1.05 V – 1 | Unit |
|---|---|---|---|---|---|
| 18 × 18 multiplication | 365 | 465 | 435 | 500 | MHz |
| 18 × 18 multiplication summed with 48-bit input | 365 | 465 | 435 | 500 | MHz |
| 18 × 19 multiplier pre-adder ROM mode | 355 | 460 | 430 | 500 | MHz |
| Two 9 × 9 multiplication | 365 | 465 | 435 | 500 | MHz |
| 9 × 9 DOTP | 365 | 465 | 435 | 500 | MHz |

| Modes | V_DD =<br>1.0 V – STD | V_DD =<br>1.0 V – 1 | V_DD =<br>1.05 V – STD | V_DD =<br>1.05 V – 1 | Unit |
|---|---|---|---|---|---|
| Complex<br>18 × 19<br>multiplication | 350 | 450 | 425 | 500 | MHz |

## 7.3.2 SRAM Blocks

The following table lists the maximum operating frequency (F_MAX) of the LSRAM block in the industrial temperature range (–40 °C to 100 °C).

**Table 45 • LSRAM Performance Industrial Temperature Range (–40 °C to 100 °C)**

| V_DD =<br>1.0 V – STD | V_DD =<br>1.0 V – 1 | V_DD =<br>1.05 V – STD | V_DD =<br>1.05 V – 1 | Unit | Condition |
|---|---|---|---|---|---|
| 343 | 428 | 343 | 428 | MHz | Two-port, all supported widths, pipelined, simple-write, and write-feed-through |
| 309 | 428 | 309 | 428 | MHz | Two-port, all supported widths, non-pipelined, simple-write, and write-feed-through |
| 343 | 428 | 343 | 428 | MHz | Dual-port, all supported widths, pipelined, simple-write, and write-feed-through |
| 309 | 428 | 309 | 428 | MHz | Dual-port, all supported widths, non-pipelined, simple-write, and write-feed-through |
| 343 | 428 | 343 | 428 | MHz | Two-port pipelined ECC mode, pipelined, simple-write, and write-feed-through |
| 279 | 295 | 279 | 295 | MHz | Two-port non-pipelined ECC mode, pipelined, simple-write, and write-feed-through |
| 343 | 428 | 343 | 428 | MHz | Two-port pipelined ECC mode, non-pipelined, simple-write, and write-feed-through |
| 196 | 285 | 196 | 285 | MHz | Two-port non-pipelined ECC mode, non-pipelined, simple-write, and write-feed-through |
| 274 | 285 | 274 | 285 | MHz | Two-port, all supported widths, pipelined, and read-before-write |
| 274 | 285 | 274 | 285 | MHz | Two-port, all supported widths, non-pipelined, and read-before-write |
| 274 | 285 | 274 | 285 | MHz | Dual-port, all supported widths, pipelined, and read-before-write |
| 274 | 285 | 274 | 285 | MHz | Dual-port, all supported widths, non-pipelined, and read-before-write |
| 274 | 285 | 274 | 285 | MHz | Two-port pipelined ECC mode, pipelined, and read-before-write |
| 274 | 285 | 274 | 285 | MHz | Two-port non-pipelined ECC mode, pipelined, and read-before-write |

| V DD =
1.0 V – STD | V DD =
1.0 V – 1 | V DD =
1.05 V – STD | V DD =
1.05 V – 1 | Unit | Condition |
|---|---|---|---|---|---|
| 274 | 285 | 274 | 285 | MHz | Two-port pipelined ECC mode, non-pipelined, and read-before-write |
| 193 | 285 | 193 | 285 | MHz | Two-port non-pipelined ECC mode, non-pipelined, and read-before-write |

The following table lists the maximum operating frequency ($F_{MAX}$) of the µSRAM block in the industrial temperature range (–40 °C to 100 °C).

**Table 46 • µSRAM Performance**

| Parameter | Symbol | V DD =
1.0 V – STD | V DD =
1.0 V – 1 | V DD =
1.05 V – STD | V DD =
1.05 V – 1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| Operating frequency | $F_{MAX}$ | 400 | 415 | 450 | 480 | MHz | Write-port |
| Read access time | Tac | | 2 | | 2 | ns | Read-port |

The following table lists the maximum operating frequency ($F_{MAX}$) of the µPROM block in the industrial temperature range (–40 °C to 100 °C).

**Table 47 • µPROM Performance**

| Parameter | Symbol | V DD =
1.0 V – STD | V DD =
1.0 V – 1 | V DD =
1.05 V – STD | V DD =
1.05 V – 1 | Unit |
|---|---|---|---|---|---|---|
| Read access time | Tac | 10 | 10 | 10 | 10 | ns |

## 7.4 Transceiver Switching Characteristics

This section describes transceiver switching characteristics.

### 7.4.1 Transceiver Performance

The following table describes transceiver performance.

**Table 48 • PolarFire Transceiver and TXPLL Performance**

| Parameter | Symbol | STD Min | STD Typ | STD Max | –1 Min | –1 Typ | –1 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Tx data rate[1,2] | $F_{TXRate}$ | 0.25 | | 10.3125 | 0.25 | | 12.7 | Gbps |
| Tx OOB (serializer bypass) data rate | $F_{TXRateOOB}$ | DC | | 1.5 | DC | | 1.5 | Gbps |
| Rx data rate when AC coupled[2] | $F_{RxRateAC}$ | 0.25 | | 10.3125 | 0.25 | | 12.7 | Gbps |
| Rx data rate when DC coupled | $F_{RxRateDC}$ | 0.25 | | 3.2 | 0.25 | | 3.2 | Gbps |
| Rx OOB (deserializer bypass) data rate | $F_{TXRateOOB}$ | DC | | 1.25 | DC | | 1.25 | Gbps |
| TXPLL output frequency[3] | $F_{TXPLL}$ | 1.6 | | 5.1563 | 1.6 | | 6.35 | GHz |
| Rx CDR mode | $F_{RXCDR}$ | 0.25 | | 10.3125 | 0.25 | | 10.3125 | Gbps |
| Rx DFE mode[2] | $F_{RXDFE}$ | 3.0 | | 10.3125 | 3.0 | | 12.7 | Gbps |
| Rx Eye Monitor mode[2] | $F_{RXEyeMon}$ | 3.0 | | 10.3125 | 3.0 | | 12.7 | Gbps |

1. The reference clock is required to be a minimum of 75 MHz for data rates of 10 Gbps and above.

2. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).
3. The Tx PLL rate is between 0.5x to 5.5x the Tx data rate. The Tx data rate depends on per XCVR lane Tx post-divider settings.

## 7.4.2 Transceiver Reference Clock Performance

The following table describes performance of the transceiver reference clock.

**Table 49 • PolarFire Transceiver Reference Clock AC Requirements**

| Parameter | Symbol | STD Min | STD Typ | STD Max | −1 Min | −1 Typ | −1 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Reference clock input rate[1, 2] | $F_{TXREFCLK}$ | 20 | | 400 | 20 | | 400 | MHz |
| Reference clock input rate[1, 2, 3] | $F_{XCVRREFCLKMAXCASCADE}$ | 20 | | 156 | 20 | | 156 | MHz |
| Reference clock rate at the Tx PLL PFD[4] | $F_{TXREFCLKPFD}$ | 20 | | 156 | 20 | | 175 | MHz |
| Reference clock rate recommended at the PFD for Tx rates 10 Gbps and above[4] | $F_{TXREFCLKPFD10G}$ | 75 | | 156 | 75 | | 175 | MHz |
| Tx reference clock phase noise requirements to meet jitter specifications (156 MHz clock at reference clock input)[5] | $F_{TXREFPN}$ | | | −110 | | | −110 | dBc /Hz |
| Phase noise at 10 KHz | $F_{TXREFPN}$ | | | −110 | | | −110 | dBc /Hz |
| Phase noise at 100 KHz | $F_{TXREFPN}$ | | | −115 | | | −115 | dBc /Hz |
| Phase noise at 1 MHz | $F_{TXREFPN}$ | | | −135 | | | −135 | dBc /Hz |
| Reference clock input rise time (10%–90%) | $T_{REFRISE}$ | | 200 | 500 | | 200 | 500 | ps |
| Reference clock input fall time (90%–10%) | $T_{REFFALL}$ | | 200 | 500 | | 200 | 500 | ps |
| Reference clock rate at RX CDR | $F_{RXREFCLKCDR}$ | 20 | | 156 | 20 | | 156 | MHz |
| Reference clock duty cycle | $T_{REFDUTY}$ | 40 | | 60 | 40 | | 60 | % |
| Spread spectrum modulation spread[6] | Mod_Spread | 0.1 | | 3.1 | 0.1 | | 3.1 | % |
| Spread spectrum modulation frequency[7] | Mod_Freq | TxREF CLKPFD/ (128) | 32 | TxREF CLKPFD/ (128*63) | TxREF CLKPFD/ (128) | 32 | TxREF CLKPFD/ (128*63) | KHz |

1. See the maximum reference clock rate allowed per input buffer standard.
2. The minimum value applies to this clock when used as an XCVR reference clock. It does not apply when used as a non-XCVR input buffer (DC input allowed).
3. Cascaded reference clock.
4. After reference clock input divider.
5. Required maximum phase noise is scaled based on actual $F_{TxRefClkPFD}$ value by 20 × log10 (TxRefClkPFD /156 MHz). It is assumed that the reference clock divider of 4 is used for these calculations to always meet the maximum PFD frequency specification.
6. Programmable capability for depth of down-spread or center-spread modulation.
7. Programmable modulation rate based on the modulation divider setting (1 to 63).

### 7.4.3 Transceiver Reference Clock I/O Standards

The following differential I/O standards are supported as transceiver reference clocks.

- LVDS25/33
- HCLS25 (for PCIe)
- RSDS25/33
- MINILVDS25/33
- SUBLVDS25/33
- PPDS25/33
- SLVS25/33
- BUSLVDS25
- MLVDS25
- LVPECL33
- MIPI25

For DC input levels, see table Differential DC Input and Output Levels.

**Note:** The transceiver reference clock differential receiver supports $V_{ICM}$ common mode.

**Note**: The amount of jitter from the input receiver increases at common modes of less 0.2 V or greater than VDDSREF–0.4 V. Therefore, for improved SerDes operation, it is recommended that the $V_{CM}$ of the signal into the SerDes reference clock input be at a minimum of 0.2 V and below VDDSREF–0.4 V.

The following single-ended I/O standard s are supported as transceiver reference clocks.

- LVTTL
- LVCMOS33
- LVCMOS25
- LVCMOS18
- SSTL25I/II
- SSTL18I/II
- HSUL18I/II

For DC input levels, see table DC Input and Output Levels.

**Note**: Generally, Hysteresis = Off is recommended. In extremely high noise systems with degraded reference clock input, Hysteresis = On may improve results.

### 7.4.4 Transmitter Performance

The following tables describe performance of the transmitter.

**Table 50 • Transceiver Reference Clock Input Termination**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Single-ended termination | RefTerm | | 50 | | Ω |
| Single-ended termination | RefTerm | | 75 | | Ω |
| Single-ended termination | RefTerm | | 150 | | Ω |
| Differential termination | RefDiffTerm | | 115[1] | | Ω |
| Power-up termination | | | >50K | | Ω |

1. Measured at VCM= 1.2 V and VID= 350 mV.

**Note**: All pull-ups are disabled at power-up to allow hot plug capability.

**Table 51 • PolarFire Transceiver User Interface Clocks**

| Parameter | Modes [1] | STD Min | STD Max | −1 Min | −1 Max | Unit |
|---|---|---|---|---|---|---|
| Transceiver TX_CLK range (non-deterministic PCS mode with global or regional fabric clocks) | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |
| | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |
| | 16-bit, max data rate = 4.8 Gbps | | 300 | | 300 | MHz |
| | 20-bit, max data rate = 6.0 Gbps | | 300 | | 300 | MHz |
| | 32-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 325 | | 325 | MHz |
| | 40-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 260 | | 320 | MHz |
| | 64-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 165 | | 200 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 130 | | 160 | MHz |
| | Fabric pipe mode 32-bit, max data rate = 6.0 Gbps | | 150 | | 150 | MHz |
| Transceiver RX_CLK range (non-deterministic PCS mode with global or regional fabric clocks) | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |
| | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |
| | 16-bit, max data rate = 4.8 Gbps | | 300 | | 300 | MHz |
| | 20-bit, max data rate = 6.0 Gbps | | 300 | | 300 | MHz |
| | 32-bit, max data rate = 10.3125 Gbps | | 325 | | 325 | MHz |
| | 40-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 260 | | 320 | MHz |
| | 64-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 165 | | 200 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 130 | | 160 | MHz |
| | Fabric pipe mode 32-bit, max data rate = 6.0 Gbps | | 150 | | 150 | MHz |
| Transceiver TX_CLK range (deterministic PCS mode with regional fabric clocks) | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |
| | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |
| | 16-bit, max data rate = 3.6 Gbps (−STD) / 4.25 Gbps (−1) | | 225 | | 266 | MHz |
| | 20-bit, max data rate = 4.5 Gbps (−STD) / 5.32 Gbps (−1) | | 225 | | 266 | MHz |
| | 32-bit, max data rate = 7.2 Gbps (−STD) / 8.5 Gbps (−1) | | 225 | | 266 | MHz |
| | 40-bit, max data rate = 9.0 Gbps (−STD) / 10.6 Gbps (−1)[1] | | 225 | | 266 | Mhz |
| | 64-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 165 | | 200 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps (−STD) / 12.7 Gbps (−1)[1] | | 130 | | 160 | MHz |
| Transceiver RX_CLK range (deterministic PCS mode with regional fabric clocks) | 8-bit, max data rate = 1.6 Gbps | | 200 | | 200 | MHz |
| | 10-bit, max data rate = 1.6 Gbps | | 160 | | 160 | MHz |

| Parameter | Modes [1] | STD Min | STD Max | −1 Min | −1 Max | Unit |
|---|---|---|---|---|---|---|
| | 16-bit, max data rate = 3.6 Gbps (–STD) / 4.25 Gbps (–1) | | 225 | | 266 | MHz |
| | 20-bit, max data rate = 4.5 Gbps (–STD) / 5.32 Gbps (–1) | | 225 | | 266 | MHz |
| | 32-bit, max data rate = 7.2 Gbps (–STD) / 8.5 Gbps (–1) | | 225 | | 266 | MHz |
| | 40-bit, max data rate = 9.0 Gbps (–STD) / 10.6 Gbps (–1)[1] | | 225 | | 266 | MHz |
| | 64-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 165 | | 200 | MHz |
| | 80-bit, max data rate = 10.3125 Gbps (–STD) / 12.7 Gbps (–1)[1] | | 130 | | 160 | MHz |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6) .

**Note**: Until specified, all modes are non-deterministic. For more information, see UG0677: PolarFire FPGA Transceiver User Guide.

### Table 52 • PolarFire Transceiver Transmitter Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Differential termination | $V_{OTERM}$ | | 85 | | Ω | |
| | $V_{OTERM}$ | | 100 | | Ω | |
| | $V_{OTERM}$ | | 150 | | Ω | |
| Common mode voltage[1] | $V_{OCM}$ | $0.44 \times V_{DDA}$ | $0.525 \times V_{DDA}$ | $0.59 \times V_{DDA}$ | V | DC coupled 50% setting |
| | $V_{OCM}$ | $0.52 \times V_{DDA}$ | $0.6 \times V_{DDA}$ | $0.66 \times V_{DDA}$ | V | DC coupled 60% setting |
| | $V_{OCM}$ | $0.61 \times V_{DDA}$ | $0.7 \times V_{DDA}$ | $0.75 \times V_{DDA}$ | V | DC coupled 70% setting |
| | $V_{OCM}$ | $0.63 \times V_{DDA}$ | $0.8 \times V_{DDA}$ | $0.83 \times V_{DDA}$ | V | DC coupled 80% setting |
| Rise time[2] Fall time[2] | $T_{TxRF}$ | 40 | | 61 | ps | 20% to 80% |
| | | 39 | | 58 | ps | 80% to 20% |
| Differential peak-to-peak amplitude | $V_{ODPP}$ | 1080 | 1140 | 1320 | mV | 1000 mV setting |
| | $V_{ODPP}$ | 1010 | 1060 | 1220 | mV | 800 mV setting |
| | $V_{ODPP}$ | 550 | 580 | 670 | mV | 500 mV setting |
| | $V_{ODPP}$ | 465 | 490 | 560 | mV | 400 mV setting |
| | $V_{ODPP}$ | 350 | 370 | 425 | mV | 300 mV setting |
| | $V_{ODPP}$ | 250 | 260 | 300 | mV | 200 mV setting |
| | $V_{ODPP}$ | 150 | 160 | 185 | mV | 100 mV setting |
| Transmit lane P to N skew[3] | $T_{OSKEW}$ | | 8 | 15 | ps | |
| Lane to lane transmit skew[4] | $T_{LLSKEW}$ | | | 75 | ps | Single PLL, 2–4 bonded lanes, 8–40-bit fabric width[10] |
| | | | | 8 | UI | Single PLL, 2–4 bonded lanes, 64–80-bit fabric width[11] |
| | | | | 8 + Refclk skew | UI | Multiple PLL, 2–4 bonded lanes, 8–40-bit fabric width[11, 12] |
| | | | | 32 + Refclk skew | UI | Multiple PLL, 2–4 bonded lanes, 64–80-bit fabric width[11, 12] |
| Electrical idle transition entry time[7] | TTxEITrEntry | | | 20 | ns | |
| Electrical idle transition exit time[7] | TTxEITrExit | | | 19 | ns | |
| Electrical idle amplitude | VTxEIpp | | | 7 | mV | |
| TXPLL lock time | $T_{TXLock}$ | | | 1600 | PFD cycles | |
| Digital PLL lock time[8] | $T_{DPLLLock}$ | | | 75,000 | REFCLK UIs | Frequency lock |
| | | | | 150,000 | REFCLK UIs | Phase lock |

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.22 0.1 | UI UI | Data rate ≥10.3125 Gbps to 12.7 Gbps[9] (Tx Vco rate 5.16 GHz to 6.35 GHz)<br><br>TXPLL in integer mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.28 0.1 | UI UI | Data rate ≥10.3125 to 12.7 Gbps[9] (Tx Vco rate 5.16 GHz to 6.35 GHz)<br><br>TXPLL in fractional mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.22 0.09 | UI UI | Data rate ≥8.5 Gbps to 10.3125 Gbps (Tx Vco rate 4.25 GHz to 5.16 GHz)<br><br>TXPLL in integer mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.28 0.09 | UI UI | Data rate ≥8.5 Gbps to 10.3125 Gbps (Tx Vco rate 4.25 GHz to 5.16 GHz) TXPLL in fractional mode |
| Total jitter[5, 6, 13] Deterministic jitter[5,6] | $T_J$ $T_{DJ}$ | | | 0.21 0.09 | UI UI | Data rate ≥5.0 Gbps to 8.5 Gbps (Tx Vco rate 2.5 GHz to 4.25 GHz)<br><br>TXPLL in integer mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.25 0.09 | UI UI | Data rate ≥5.0 Gbps to 8.5 Gbps (Tx Vco rate 2.5 GHz to 4.25 GHz)<br><br>TXPLL in fractional mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.17 0.03 | UI UI | Data rate ≥1.6 Gbps to 5.0 Gbps (Tx Vco rate 1.6 GHz to 2.5 GHz)<br><br>TXPLL in integer mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.2 0.03 | UI UI | Data rate ≥1.6 Gbps to 5.0 Gbps (Tx Vco rate 1.6 GHz to 2.5 GHz)<br><br>TXPLL in fractional mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.08 0.02 | UI UI | Data rate ≥ 800 Mbps to 1.6 Gbps (Tx Vco rate 1.6 GHz)<br><br>TXPLL in integer mode |
| Total jitter[5, 6, 13] Deterministic jitter[5, 6] | $T_J$ $T_{DJ}$ | | | 0.11 0.02 | UI UI | Data rate ≥ 800 Mbps to 1.6 Gbps (Tx Vco rate 1.6 GHz)<br><br>TXPLL in fractional mode |

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Total jitter[5, 6, 13] | $T_J$ | | | 0.05 | UI | Data rate = 250 Mbps to |
| Deterministic jitter[5, 6] | $T_{DJ}$ | | | 0.01 | UI | 800 Mbps (Tx $V_{CO}$ rate 1.48 GHz to 1.6 GHz) TXPLL in integer mode |
| Total jitter[5, 6, 13] | $T_J$ | | | 0.06 | UI | Data rate = 250 Mbps to |
| Deterministic jitter[5, 6] | $T_{DJ}$ | | | 0.01 | UI | 800 Mbps (Tx $V_{CO}$ rate 1.48 GHz to 1.6 GHz) TXPLL in fractional mode |

1. Increased DC common mode settings above 50% reduce allowed $V_{OD}$ output swing capabilities.
2. Adjustable through transmit emphasis.
3. With estimated package differences.
4. Single PLL applies to all four lanes in the same quad location with the same T xPLL. Multiple PLL applies to N lanes using multiple TxPLLs from different quad locations.
5. Improved jitter characteristics for a specific industry standard are possible in many cases due to improved reference clock or higher $V_{CO}$ rate used.
6. Tx jitter is specified with all transmitters on the device enabled, a 10–12-bit error rate (BER) and Tx data pattern of PRBS7.
7. From the PMA mode, the TX_ELEC_IDLE port to the XVCR TXP/N pins.
8. FTxRefClk = 75 MHz with typical settings.
9. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).
10. Transmit alignment in this case will automatically align upon the TX PLL obtaining lock. For details on transmit alignment, see UG0677: PolarFire FPGA Transceiver User Guide.
11. In order to obtain the required alignment for these configurations, an FPGA fabric TX alignment circuit must be implemented. For details on transmit alignment, see UG0677: PolarFire FPGA Transceiver User Guide.
12. Re fclk skew is the amount of skew between the reference clocks of the two PLL.
13. Jitter decomposition can be found in the protocol characterization reports.

## 7.4.5 Receiver Performance

The following table describes performance of the receiver.

### Table 53 • PolarFire Transceiver Receiver Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Input voltage range | $V_{IN}$ | 0 | | $V_{DDA}$ + 0.3 | V | |
| Differential peak-to-peak amplitude | $V_{IDPP}$ | 140 | | 1250 | mV | |
| Differential termination | $V_{ITERM}$ | | 85 | | Ω | |
| | | | 100 | | Ω | |
| | | | 150 | | Ω | |
| Common mode voltage | $V_{ICMDC}$ [1] | $0.7 \times V_{DDA}$ | | $0.9 \times V_{DDA}$ | V | DC coupled |
| Exit electrical idle detection time | $T_{EIDET}$ | | 50 | 100 | ns | |
| Run length of consecutive identical digits (CID) | $C_{ID}$ | | | 200 | UI | |
| CDR PPM tolerance[2] | $C_{DRPPM}$ | | | | % UI | |

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| CDR lock-to-data time | $T_{LTD}$ | | | | CDR$_{REFCLK}$ UI | |
| CDR lock-to-ref time | $T_{LTF}$ | | | | CDR$_{REFCLK}$ UI | |
| Loss-of-signal detect (Peak Detect Range setting = high)[9, 10] | $V_{DETLHIGH}$ | 145 | | 295 | mV | Setting = 3 |
| | | 155 | | 340 | mV | Setting = 4 |
| | | 180 | | 365 | mV | Setting = 5 |
| | | 195 | | 375 | mV | Setting = 6 |
| | | 210 | | 385 | mV | Setting = 7 |
| Loss-of-signal detect (Peak Detect Range setting = low)[9, 10] | $V_{DETLOW}$ | 65 | | 175 | mV | Setting = PCIe[3, 7] |
| | | 95 | | 190 | mV | Setting = SATA[4, 8] |
| | | 75 | | 170 | mV | Setting = 1 |
| | | 95 | | 185 | mV | Setting = 2 |
| | | 100 | | 190 | mV | Setting = 3 |
| | | 140 | | 210 | mV | Setting = 4 |
| | | 155 | | 240 | mV | Setting = 5 |
| | | 165 | | 245 | mV | Setting = 6 |
| | | 170 | | 250 | mV | Setting = 7 |
| Sinusoidal jitter tolerance | $T_{SJTOL}$ | 0.34 | | | UI | >8.5 Gbps −12.7 Gbps[5, 11] |
| | | 0.43 | | | UI | >8.0–8.5 Gbps[5] |
| | | 0.45 | | | UI | >3.2–8.0 Gbps[5] |
| | | 0.45 | | | UI | >1.6 to 3.2 Gbps[5] |
| | | 0.42 | | | UI | >0.8 to 1.6 Gbps[5] |
| | | 0.41 | | | UI | 250 to 800 Mpbs[5] |
| Total jitter tolerance with stressed eye | $T_{TJTOLSE}$ | 0.65 | | | UI | 3.125 Gbps[5] |
| | | 0.65 | | | UI | 6.25 Gbps[6] |
| | | 0.7 | | | UI | 10.3125 Gbps[6] |
| | | 0.7 | | | UI | 12.7 Gbps[6, 11] |
| Sinusoidal jitter tolerance with stressed eye | $T_{SJTOLSE}$ | 0.1 | | | UI | 3.125 Gbps[5] |
| | | 0.05 | | | UI | 6.25 Gbps[6] |
| | | 0.05 | | | UI | 10.3125 Gbps[6] |
| | | 0.05 | | | UI | 12.7 Gbps[6, 11] |
| CTLE DC gain (all stages, max settings) | | 0.1 | | 10 | dB | |
| CTLE AC gain (all stages, max settings) | | 0.05 | | 16 | dB | |
| DFE AC gain (per 5 stages, max settings) | | 0.05 | | 7.5 | dB | |
| Auto adaptive calibration time (CTLE or CTLE+DFE) | | 0.05 | | | ms | |

1. Valid at 3.2 Gbps and below.
2. Data vs. Rx reference clock frequency.
3. Achieves compliance with PCIe electrical idle detection.
4. Achieves compliance with SATA OOB specification.
5. Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV $V_{ID}$, all stages of Rx CTLE enabled, DFE disabled, 80 MHz sinusoidal jitter injected to Rx data.

6. Rx jitter values based on bit error ratio (BER) of 10–12, AC coupled input with 400 mV $V_{ID}$, all stages of Rx CTLE enabled, DFE enabled, 80 MHz sinusoidal jitter injected to Rx data.
7. For PCIe: Low Threshold Setting = 0, High Threshold Setting = 2.
8. For SATA: Low Threshold Setting = 2, High Threshold Setting = 3.
9. Loss of signal is valid for data rates of 1 Gbps to 5 Gbps for PRBS7 (8B/10B) or PRBS31 (64b/6xb) data formats. It is also valid for detection of SATA out-of-band signals at data rates up to 6 Gbps. If the default settings for the low threshold (0x0) and high threshold (0x2) using the low range option for the peak detector are used, then the Rx $V_{Amplitude}$ pk-pk (outside of data eye) at the receiver input package pins must be a minimum of 300 mV for short reach (6.5 dB insertion loss at 5 GHz) applications, 350 mV for medium reach (17.0 dB insertion loss at 5 GHz) applications, and 450 mV for long reach (25.0 dB insertion loss at 5 GHz) applications—generally the settings are less limiting than what is required for good BER operation of the SerDes. Note that if the option to force CDR Lock2Ref upon Rx Idle is set (default at data rates of 5 Gbps and below), this minimum $V_{Amplitude}$ pk-pk must be enforced for proper CDR operation.
10. Detect values measured at 1.5 Gbps with PRBS7 data pattern.
11. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

## 7.5 Transceiver Protocol Characteristics

The following section describes transceiver protocol characteristics.

### 7.5.1 PCI Express

The following tables describe the PCI express.

**Table 54 • PCI Express Gen1**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 2.5 Gbps | | 0.25 | UI |
| Receiver jitter tolerance | 2.5 Gbps | 0.4 | | UI |

**Note**: With add-in card, as specified in PCI Express CEM Rev 2.0.

**Table 55 • PCI Express Gen2**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 5.0 Gbps | | 0.35 | UI |
| Receiver jitter tolerance | 5.0 Gbps | 0.4 | | UI |

**Note**: With add-in card as specified in PCI Express CEM Rev 2.0.

### 7.5.2 Interlaken

The following table describes Interlaken.

**Table 56 • Interlaken**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 6.375 Gbps | | 0.3 | UI |
| | 10.3125 Gbps | | 0.3 | UI |
| | 12.7 Gbps[1] | | 0.3 | UI |
| Receiver jitter tolerance | 6.375 Gbps | 0.6 | | UI |
| | 10.3125 Gbps | 0.65 | | UI |
| | 12.7 Gbps[1] | 0.65 | | UI |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

### 7.5.3 10GbE (10GBASE-R, and 10GBASE-KR)

The following table describes 10GbE (10GBASE-R).

**Table 57 • 10GbE (10GBASE-R)**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 10.3125 Gbps | | 0.28 | UI |
| Receiver jitter tolerance | 10.3125 Gbps | 0.7 | | UI |

The following table describes 10GbE (10GBASE-KR).

**Table 58 • 10GbE (10GBASE-KR)**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 10.3125 Gbps | | 0.28 | UI |
| Receiver jitter tolerance (SJ) | 10.3125 Gbps | 0.115 | | UI |
| Receiver jitter tolerance (RJ) | 10.3125 Gbps | 0.13 | | UI |
| Receiver jitter tolerance (DCD) | 10.3125 Gbps | 0.035 | | UI |

The following table describes 10GbE (XAUI).

**Table 59 • 10GbE (XAUI)**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter (near end) | 3.125 Gbps | | 0.35 | UI |
| Total transmit jitter (far end) | | | 0.55 | UI |
| Receiver jitter tolerance | 3.125 Gbps | 0.65 | | UI |

The following table describes 10GbE (RXAUI).

**Table 60 • 10GbE (RXAUI)**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter (near-end) | 6.25 Gbps | | 0.35 | UI |
| Total transmit jitter (far-end) | 6.25 Gbps | | 0.55 | UI |
| Receiver jitter tolerance | 6.25 Gbps | 0.65 | | UI |

## 7.5.4 1GbE (1000BASE-X)
The following table describes 1GbE (1000BASE-X).

**Table 61 • 1GbE (1000BASE-X)**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 1.25 Gbps | | 0.24 | UI |
| Receiver jitter tolerance | 1.25 Gbps | 0.749 | | UI |

## 7.5.5 SGMII and QSGMII
The following table describes SGMII.

**Table 62 • SGMII**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 1.25 Gbps | | 0.24 | UI |
| Receiver jitter tolerance | 1.25 Gbps | 0.749 | | UI |

The following table describes QSGMII.

**Table 63 • QSGMII**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 5.0 Gbps | | 0.3 | UI |
| Receiver jitter tolerance | 5.0 Gbps | 0.65 | | UI |

### 7.5.6 CPRI
The following table describes CPRI.

**Table 64 • CPRI**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 0.6144 Gbps | | 0.35 | UI |
| | 1.2288 Gbps | | 0.35 | UI |
| | 2.4576 Gbps | | 0.35 | UI |
| | 3.0720 Gbps | | 0.35 | UI |
| | 4.9152 Gbps | | 0.3 | UI |
| | 6.1440 Gbps | | 0.3 | UI |
| | 8.11008 Gbps | | 0.335 | UI |
| | 9.8304 Gbps | | 0.335 | UI |
| Receive jitter tolerance | 0.6144 Gbps | 0.75 | | UI |
| | 1.2288 Gbps | 0.75 | | UI |
| | 2.4576 Gbps | 0.75 | | UI |
| | 3.0720 Gbps | 0.75 | | UI |
| | 4.9152 Gbps | 0.7 | | UI |
| | 6.1440 Gbps | 0.7 | | UI |
| | 8.11008 Gbps | 0.7 | | UI |
| | 9.8304 Gbps | 0.7 | | UI |

### 7.5.7 JESD204B
The following table describes JESD204B.

**Table 65 • JESD204B**

| Parameter | Data Rate | Min | Max | Unit |
|---|---|---|---|---|
| Total transmit jitter | 3.125 Gbps | | 0.35 | UI |
| | 6.25 Gbps | | 0.3 | UI |
| | 12.5 Gbps[1] | | 0.3 | UI |
| Receive jitter tolerance | 3.125 Gbps | 0.56 | | UI |
| | 6.25 Gbps | 0.6 | | UI |
| | 12.5 Gbps[1] | 0.7 | | UI |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

## 7.5.8 Display Port

The following table describes Display Port.

**Table 66 • Display Port**

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 1.62 Gbps | Test point: TP2 | | 0.27 | UI |
| | 2.7 Gbps | Test point: TP2 | | 0.42 | UI |
| | 5.4 Gbps | Test point: TP3_EQ | | 0.62 | UI |
| Receive jitter tolerance | 1.62 Gbps | SJ at 20 MHz | 0.747 | | UI |
| | 2.7 Gbps | SJ at 100 MHz | 0.491 | | UI |
| | 5.4 Gbps | SJ at 10 MHz | 0.636 | | UI |

## 7.5.9 Serial RapidIO

The following table describes Serial RapidIO.

**Table 67 • Serial RapidIO**

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 1.25 Gbps | | | 0.35 | UI |
| | 2.5 Gbps | | | 0.35 | UI |
| | 3.125 Gbps | | | 0.35 | UI |
| | 5.0 Gbps | | | 0.3 | UI |
| | 6.25 Gbps | | | 0.3 | UI |
| | 10.3125 Gbps | | | 0.28 | UI |
| Receive jitter tolerance | 1.25 Gbps | | 0.65 | | UI |
| | 2.5 Gbps | | 0.65 | | UI |
| | 3.125 Gbps | | 0.65 | | UI |
| | 5.0 Gbps | Short reach | 0.6 | | UI |
| | | Long reach | 0.95 | | UI |
| | 6.25 Gbps | Short reach | 0.6 | | UI |
| | | Long reach | 0.95 | | UI |
| | 10.3125 Gbps | Short reach | 0.62 | | UI |

### 7.5.10 SDI

The following table describes SDI.

**Table 68 • SDI**

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 270 Mbps | Timing jitter (10 Hz–27 MHz) | | | UI |
| | | Alignment jitter (1 KHz–27 MHz) | | | UI |
| | 1.485 Gbps | Timing jitter (10 Hz–148.5 MHz) | | 1.0 | UI |
| | | Alignment jitter (100 KHz–148.5 MHz) | | 0.2 | UI |
| | 2.97 Gbps | Timing jitter (10 Hz–297 MHz) | | 2.0 | UI |
| | | Alignment jitter (100 KHz–297 MHz) | | 0.3 | UI |
| Receive jitter tolerance | 270 Mbps | Alignment jitter | | | UI |
| | 1.485 Gbps | Alignment jitter | 0.2 | | UI |
| | 2.97 Gbps | Alignment jitter | 0.3 | | UI |

### 7.5.11 OTN

The following table describes OTN.

**Table 69 • OTN**

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 2.66 Gbps | 3 dB BW: 5 KHz to 20 MHz | | 0.3 | UI |
| | | 3 dB BW: 1 MHz to 20 MHz | | 0.1 | UI |
| | 10.70 Gbps | 3 dB BW: 20 KHz to 80 MHz | | 0.3 | UI |
| | | 3 dB BW: 4 MHz to 80 MHz | | 0.1 | UI |
| | 11.09 Gbps[1] | 3 dB BW: 20 KHz to 80 MHz | | 0.3 | UI |
| | | 3 dB BW: 4 MHz to 80 MHz | | 0.1 | UI |
| Receive jitter tolerance | 2.66 Mbps | SJ at 5 KHz | 1.5 | | UI |
| | | SJ at 20 MHz | 0.15 | | UI |
| | 10.70 Gbps | SJ at 20 KHz | 1.5 | | UI |
| | | SJ at 80 MHz | 0.15 | | UI |
| | 11.09 Gbps[1] | SJ at 20 KHz | 1.5 | | UI |
| | | SJ at 80 MHz | 0.15 | | UI |

1. For data rates greater than 10.3125 Gbps, VDDA must be set to 1.05 V mode. See supply tolerance in the section Recommended Operating Conditions (see page 6).

### 7.5.12 Fiber Channel

The following table describes Fiber Channel.

**Table 70 • Fiber Channel**

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 1.0625 Gbps | | | | UI |
| | 2.125 Gbps | | | | UI |
| | 4.25 Gbps | | | | UI |
| | 8.5 Gbps | | | | UI |
| Receive jitter tolerance | 2.66 Mbps | | | | UI |
| | 10.70 Gbps | | | | UI |
| | 11.09 Gbps | | | | UI |

### 7.5.13 HiGig and HiGig+

The following table describes HiGig and HiGig+.

**Table 71 • HiGig, HiGig+**

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 3.75 Gbps | Near-end | | | UI |
| | 3.75 Gbps | Far-end | | | UI |
| Receive jitter tolerance | 3.75 Gbps | | | | UI |

### 7.5.14 HiGig II

The following table describes HiGig II.

**Table 72 • HiGig II**

| Parameter | Data Rate | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Total transmit jitter | 4.065 Gbps | Near-end | | | UI |
| | 4.065 Gbps | Far-end | | | UI |
| Receive jitter tolerance | 4.065 Gbps | | | | UI |

## 7.6 Non-Volatile Characteristics

The following section describes non-volatile characteristics.

### 7.6.1 FPGA Programming Cycle and Retention

The following table describes FPGA programming cycle and retention.

**Table 73 • FPGA Programming Cycles vs Retention Characteristics**

| Programming $T_J$ | Programming Cycles, Max | Retention Years | Retention Years at $T_J$ |
|---|---|---|---|
| 0 °C to 85 °C | 1000 | 20 | 85 °C |
| 0 °C to 100 °C | 500 | 20 | 100 °C |

| Programming T$_J$ | Programming Cycles, Max | Retention Years | Retention Years at T$_J$ |
|---|---|---|---|
| −20 °C to 100 °C | 500 | 20 | 100 °C |
| −40 °C to 100 °C | 500 | 20 | 100 °C |
| −40 °C to 85 °C | 1000 | 16 | 100 °C |
| −40 °C to 55 °C | 2000 | 12 | 100 °C |

**Note:** Power supplied to the device must be valid during programming operations such as programming and verify . Programming recovery mode is available only for in-application programming mode and requires an external SPI flash.

## 7.6.2 FPGA Programming Time

The following tables describe FPGA programming time.

**Table 74 • Master SPI Programming Time (IAP)**

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | T$_{PROG}$ | MPF100T, TL, TS, TLS | 17 | 25 | s |
| | | MPF200T, TL, TS, TLS | 17 | 25 | s |
| | | MPF300T, TL, TS, TLS | 26 | 32 | s |
| | | MPF500T, TL, TS, TLS | 31 | 37 | s |

**Table 75 • Slave SPI Programming Time**

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | T$_{PROG}$ | MPF100T, TL, TS, TLS[1] | 27 | 33 | s |
| | | MPF200T, TL, TS, TLS[1] | 41 | 50 | s |
| | | MPF300T, TL, TS, TLS[1] | 50 | 60 | s |
| | | MPF500T, TL, TS, TLS[1] | 90 | 108 | s |

1. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port running at 6.67 MHz. Bitstream stored in DDR. DirectC version 4.1.

**Table 76 • JTAG Programming Time**

| Parameter | Symbol | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|
| Programming time | T$_{PROG}$ | MPF100T, TL, TS, TLS[1] | 35 | 42 | s |
| | | MPF200T, TL, TS, TLS[1] | 56 | 68 | s |
| | | MPF300T, TL, TS, TLS[1] | 95 | 114 | s |
| | | MPF500T, TL, TS, TLS[1] | 122 | 147 | s |

1. Programmer: FlashPro5 with TCK 10 MHz. PC Configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

### 7.6.3 FPGA Bitstream Sizes

The following table describes FPGA bitstream sizes.

**Table 77 • Initialization Client Sizes**

| Device | Plaintext | Ciphertext |
|---|---|---|
| MPF100T, TL, TS, TLS | 1580 KB | 1630 KB |
| MPF200T, TL, TS, TLS | 2916 KB | 3006 KB |
| MPF300T, TL, TS, TLS | 4265 KB | 4403 KB |
| MPF500T, TL, TS, TLS | 6835 KB | 7045 KB |

**Note:** Worst case initializing all fabric LSRAM, USRAM, and UPROM.

**Table 78 • Bitstream Sizes**

| File | Devices | FPGA | Security | SNVM (all pages) | FPGA+ SNVM | FPGA+ Sec | SNVM+ Sec | FPGA+ SNVM+ Sec |
|---|---|---|---|---|---|---|---|---|
| SPI | MPF100T, TL, TS, TLS | 3.4 MB | 3.5 KB | 59.7 KB | 3.5 MB | 3.5 MB | 62.2 KB | 3.5 MB |
| DAT | MPF100T, TL, TS, TLS | 3.4 MB | 7.6 KB | 61.2 KB | 3.5 MB | 3.4 MB | 66.3 KB | 3.5 MB |
| SPI | MPF200T, TL, TS, TLS | 5.9 MB | 3.5 KB | 59.7 KB | 5.9 MB | 5.9 MB | 62.2 KB | 6.0 MB |
| DAT | MPF200T, TL, TS, TLS | 5.9 MB | 7.6 KB | 61.2 KB | 6.0 MB | 5.9 MB | 66.3 KB | 6.0 MB |
| SPI | MPF300T, TL, TS, TLS | 9.3 MB | 3.5 KB | 59.7 KB | 9.6 MB | 9.5 MB | 62.2 KB | 9.6 MB |
| DAT | MPF300T, TL, TS, TLS | 9.3 MB | 7.6 KB | 61.2 KB | 9.6 MB | 9.5 MB | 66.3 KB | 9.6 MB |
| SPI | MPF500T, TL, TS, TLS | 14.3 MB | 3.5 KB | 59.7 KB | 14.4 MB | 14.3 MB | 62.2 KB | 14.4 MB |
| DAT | MPF500T, TL, TS, TLS | 14.3 MB | 7.6 KB | 61.2 KB | 14.4 MB | 14.3 MB | 66.3 KB | 14.4 MB |

### 7.6.4 Digest Cycles

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

**Table 79 • Maximum Number of Digest Cycles**

| Digest $T_J$ | Storage and Operating $T_J$ | Retention Since Programmed (N = Number Digests During that Time)[1] | | | | | | | Unit | Retention |
|---|---|---|---|---|---|---|---|---|---|---|
| | | N ≤300 | N = 500 | N = 1000 | N = 1500 | N = 2000 | N = 4000 | N = 6000 | | |
| −40 to 100 | −40 to 100 | 20 × LF | 17 × LF | 12 × LF | 10 × LF | 8 × LF | 4 × LF | 2 × LF | °C | Years |
| −40 to 100 | 0 to 100 | 20 × LF | 17 × LF | 12 × LF | 10 × LF | 8 × LF | 4 × LF | 2 × LF | °C | Years |
| −40 to 85 | −40 to 85 | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 16 × LF | 8 × LF | 4 × LF | °C | Years |
| −40 to 55 | −40 to 55 | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | 20 × LF | °C | Years |

1. LF = Lifetime factor as defined by the number of programming cycles the device has seen under the conditions listed in the following table.

### Table 80 • FPGA Programming Cycles Lifetime Factor

| Programming $T_J$ | Programming Cycles | LF |
|---|---|---|
| –40 °C to 100 °C | 500 | 1 |
| –40 °C to 85 °C | 1000 | 0.8 |
| –40 °C to 55 °C | 2000 | 0.6 |

**Notes:**

- The maximum number of device digest cycles is 100K.
- Digests are operational only over the –40 °C to 100 °C temperature range.
- After a program cycle, an additional N digests cycles are allowed with the resultant retention characteristics for the total operating and storage temperature shown.
- Retention is specified for total device storage and operating temperature.
- All temperatures are junction temperatures ($T_J$).
- Example 1—500 digests cycles are performed between programming cycles. N = 500. The operating conditions are –40 °C to 85 °C $T_J$. 501 programming cycles have occurred. The retention under these operating conditions is 20 × LF = 20 × .8 = 16 years.
- Example 2—one programming cycle has occurred, N = 1500 digest cycles have occurred. Temperature range is –40 °C to 100 °C. The resultant retention is 10 × LF or 10 years over the industrial temperature range.

## 7.6.5 Digest Time

The following table describes digest time.

### Table 81 • Digest Times

| Parameter | Devices | Typ | Max | Unit |
|---|---|---|---|---|
| Setup time | All | 2 | | µs |
| Fabric digest run time | MPF100T, TL, TS, TLS | 880 | 910 | ms |
| | MPF200T, TL, TS, TLS | 1005 | 1072 | ms |
| | MPF300T, TL, TS, TLS | 1503.9 | 1582 | ms |
| | MPF500T, TL, TS, TLS | 2085 | 2150 | ms |
| UFS CC digest run time | MPF100T, TL, TS, TLS | 33.5 | 35 | µs |
| | MPF200T, TL, TS, TLS | 33.5 | 35 | µs |
| | MPF300T, TL, TS, TLS | 33.5 | 35 | µs |
| | MPF500T, TL, TS, TLS | 33.5 | 35 | µs |
| sNVM digest run time[1] | MPF100T, TL, TS, TLS | 4.5 | 5 | ms |
| | MPF200T, TL, TS, TLS | 4.5 | 5 | ms |
| | MPF300T, TL, TS, TLS | 4.5 | 5 | ms |
| | MPF500T, TL, TS, TLS | 4.5 | 5 | ms |
| UFS UL digest run time | MPF100T, TL, TS, TLS | 47 | 49 | µs |
| | MPF200T, TL, TS, TLS | 47 | 49 | µs |
| | MPF300T, TL, TS, TLS | 47 | 49 | µs |
| | MPF500T, TL, TS, TLS | 47 | 49 | µs |
| User key digest run time[2] | MPF100T, TL, TS, TLS | 526 | 544 | µs |
| | MPF200T, TL, TS, TLS | 526 | 544 | µs |
| | MPF300T, TL, TS, TLS | 526 | 544 | µs |
| | MPF500T, TL, TS, TLS | 526 | 544 | µs |

| Parameter | Devices | Typ | Max | Unit |
|---|---|---|---|---|
| UFS UPERM digest run time | MPF100T, TL, TS, TLS | 33.2 | 35 | μs |
| | MPF200T, TL, TS, TLS | 33.2 | 35 | μs |
| | MPF300T, TL, TS, TLS | 33.2 | 35 | μs |
| | MPF500T, TL, TS, TLS | 33.2 | 35 | μs |
| Factory digest run time | MPF100T, TL, TS, TLS | 494 | 511 | μs |
| | MPF200T, TL, TS, TLS | 494 | 511 | μs |
| | MPF300T, TL, TS, TLS | 494 | 511 | μs |
| | MPF500T, TL, TS, TLS | 494 | 511 | μs |

1. The entire sNVM is used as ROM.
2. Valid for user key 0 through 6.

Note: These times do not include the power-up to functional timing overhead when using digest checks on power-up.

### 7.6.6 Zeroization Time

The following tables describe zeroization time. A zeroization operation is counted as one programming cycle.

Table 82 • Zeroization Times for MPF100T, TL, TS, and TLS Devices

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | 8 | 9 | ms | Zip flag set |
| Time to destroy the fabric data[1] | 248 | 253 | ms | Data erased |
| Time to destroy data in non-volatile memory (like new)[1, 2] | 507 | 522 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (recoverable)[1, 3] | 514 | 530 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | 520 | 536 | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | 0.8 | 0.9 | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | 1.5 | 1.6 | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | 1.6 | 1.7 | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1, 4] | 1.7 | 1.8 | s | Full scrubbing |
| Time to verify[5] | 1.1 | 1.2 | s | |
| Total time to zeroize (like new)[1, 2] | 2.8 | 2.9 | s | |
| Total time to zeroize (recoverable)[1, 3] | 2.9 | 3.0 | s | |
| Total time to zeroize (non-recoverable)[1, 4] | 3.1 | 3.2 | s | |

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

**Table 83 • Zeroization Times for MPF200T, TL, TS, and TLS Devices**

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | 8 | 9 | ms | Zip flag set |
| Time to destroy the fabric data[1] | 250 | 255 | ms | Data erased |
| Time to destroy data in non-volatile memory (like new)[1, 2] | 507 | 522 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (recoverable)[1, 3] | 514 | 530 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | 520 | 536 | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | 0.9 | 1.0 | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | 1.5 | 1.6 | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | 1.6 | 1.7 | s | Full scrubbing |
| Time to scrub the fabric data PNVM data (non-recoverable)[1, 4] | 1.7 | 1.8 | s | Full scrubbing |
| Time to verify[5] | 1.4 | 1.5 | s | |
| Total time to zeroize (like new)[1, 2] | 2.9 | 3.0 | s | |
| Total time to zeroize (recoverable)[1, 3] | 3.0 | 3.1 | s | |
| Total time to zeroize (non-recoverable)[1, 4] | 3.1 | 3.2 | s | |

1. Total completion time after interning zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

**Table 84 • Zeroization Times for MPF300T, TL, TS, and TLS Devices**

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | 8 | 9 | ms | Zip flag set |
| Time to destroy the fabric data[1] | 390 | 420 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (like new)[1, 2] | 507 | 522 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (recoverable)[1, 3] | 514 | 530 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (non- recoverable)[1, 4] | 520 | 536 | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | 1.3 | 1.4 | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | 1.5 | 1.6 | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | 1.6 | 1.7 | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1, 4] | 1.7 | 1.8 | s | Full scrubbing |
| Time to verify[5] | 1.8 | 1.9 | s | |
| Total time to zeroize (like new)[1, 2] | 3.7 | 3.8 | s | |
| Total time to zeroize (recoverable)[1, 3] | 3.8 | 3.9 | s | |
| Total time to zeroize (non-recoverable)[1, 4] | 3.9 | 4 | s | |

1. Total completion time after interning zeroization.

2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

**Table 85 • Zeroization Times for MPF500T, TL, TS, and TLS Devices**

| Parameter | Typ | Max | Unit | Conditions |
|---|---|---|---|---|
| Time to enter zeroization | 8 | 9 | ms | Zip flag set |
| Time to destroy the fabric data[1] | 392 | 422 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (like new)[1, 2] | 507 | 522 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (recoverable)[1, 3] | 514 | 530 | ms | One iteration of scrubbing |
| Time to destroy data in non-volatile memory (non-recoverable)[1, 4] | 520 | 536 | ms | One iteration of scrubbing |
| Time to scrub the fabric data[1] | 1.4 | 1.5 | s | Full scrubbing |
| Time to scrub the pNVM data (like new)[1, 2] | 1.5 | 1.6 | s | Full scrubbing |
| Time to scrub the pNVM data (recoverable)[1, 3] | 1.6 | 1.7 | s | Full scrubbing |
| Time to scrub the fabric data pNVM data (non-recoverable)[1] | 1.7 | 1.8 | s | Full scrubbing |
| Time to verify[5] | 1.9 | 2.0 | s | |
| Total time to zeroize (like new)[1, 2] | 3.8 | 3.9 | s | |
| Total time to zeroize (recoverable)[1, 3] | 3.9 | 4.0 | s | |
| Total time to zeroize (non-recoverable)[1, 4] | 4.0 | 4.1 | s | |

1. Total completion time after entering zeroization.
2. Like new mode—zeroizes user design security setting and sNVM content.
3. Recoverable mode—zeroizes user design security setting, sNVM and factory keys.
4. Non-recoverable mode—zeroizes user design security setting, sNVM and factory keys, and factory data required for programming.
5. Time to verify after scrubbing completes.

## 7.6.7 Verify Time

The following tables describe verify time.

**Table 86 • Standalone Fabric Verify Times**

| Parameter | Devices | Max | Unit |
|---|---|---|---|
| Standalone verification over JTAG | MPF100T, TL, TS, TLS[1] | 33 | s |
| | MPF200T, TL, TS, TLS[1] | 53 | s |
| | MPF300T, TL, TS, TLS[1] | 90 | s |
| | MPF500T, TL, TS, TLS[1] | 114 | s |
| Standalone verification over SPI | MPF100T, TL, TS, TLS[2] | 24 | s |
| | MPF200T, TL, TS, TLS[2] | 37 | s |
| | MPF300T, TL, TS, TLS[2] | 55 | s |
| | MPF500T, TL, TS, TLS[2] | 89 | s |

1. Programmer: FlashPro5, TCK 10 MHz; PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

2. SmartFusion2 with MSS running at 100 MHz, MSS_SPI_0 port r unning at 6.67 MHz. Bitstream stored in DDR. Dire ctC version 4.1.

**Notes:**

- Standalone verify is limited to 2,000 total device hours ove r the industrial –40 °C to 100 °C temperature.
- Use the digest system service, for verify device time more than 2,000 hours.
- Standalone verify checks the programming margin on both the P and N gates of the push-pull cell.
- Digest checks only the P side of the push-pull gate. However, the push-pull gates work in tandem. Digest check is recommended if users believe they will exceed the 2,000-hour verify time specification.

**Table 87 • Verify Time by Programming Hardware**

| Devices | IAP | FlashPro4 | FlashPro5 | BP | Silicon Sculptor | Units |
|---|---|---|---|---|---|---|
| MPF100T, TL, TS, TLS | 6 | 42 | 33 | | | s |
| MPF200T, TL, TS, TLS | 9 | 67 | 53 | | | s |
| MPF300T, TL, TS, TLS | 14 | 95 | 90 | | | s |
| MPF500T, TL, TS, TLS | 15 | 169 | 114 | | | s |

**Notes:**

- FlashPro4 4 MHz TCK.
- FlashPro5 10 MHz TCK.
- PC configuration: Intel i7 at 3.6 GHz, 32 GB RAM, Windows 10.

**Table 88 • Verify System Services**

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| In application verify by index | $T_{IAP\_Ver\_Index}$ | 44H | MPF100T, TL, TS, TLS | 5.9 | 6.2 | s |
| | | | MPF200T, TL, TS, TLS | 8.2 | 9 | s |
| | | | MPF300T, TL, TS, TLS | 12.4 | 13 | s |
| | | | MPF500T, TL, TS, TLS | 13.4 | 14 | s |
| In application verify by SPI address | $T_{IAP\_Ver\_Addr}$ | 45H | MPF100T, TL, TS, TLS | 5.9 | 6.2 | s |
| | | | MPF200T, TL, TS, TLS | 8.2 | 9 | s |
| | | | MPF300T, TL, TS, TLS | 12.4 | 13 | s |
| | | | MPF500T, TL, TS, TLS | 13.4 | 14 | s |

### 7.6.8 Authentication Time

The following tables describe authentication system service time.

**Table 89 • Authentication Services**

| Parameter | Symbol | ServiceID | Devices | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Bitstream Authentication | $T_{BIT\_AUTH}$ | 22H | MPF100T, TL, TS, TLS | 2.1 | 2.4 | s |
| | | | MPF200T, TL, TS, TLS | 3.3 | 3.7 | s |
| | | | MPF300T, TL, TS, TLS | 4.9 | 5.4 | s |
| | | | MPF500T, TL, TS, TLS | 7.6 | 7.8 | s |
| IAP Image Authentication | $T_{IAP\_AUTH}$ | 23H | MPF100T, TL, TS, TLS | 2.1 | 2.4 | s |
| | | | MPF200T, TL, TS, TLS | 3.3 | 3.7 | s |
| | | | MPF300T, TL, TS, TLS | 4.9 | 5.4 | s |
| | | | MPF500T, TL, TS, TLS | 7.6 | 7.8 | s |

### 7.6.9 Secure NVM Performance

The following table describes secure NVM performance.

**Table 90 • sNVM Read/Write Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Plain text programming | | 7.0 | 7.2 | 7.9 | ms | |
| Authenticated text programming | | 7.2 | 7.4 | 9.4 | ms | |
| Authenticated and encrypted text programming | | 7.2 | 7.4 | 9.4 | ms | |
| Authentication R/W 1st access from power-up overhead | $T_{PUF\_OVHD}$ | 10 | 13 | 111 | ms | From $T_{FAB\_READY}$ |
| Plain text read | | 8 | 8.5 | 9 | µs | |
| Authenticated text read | | 113 | 114.5 | 119 | µs | |
| Authenticated and decrypted text read | | 159 | 161 | 167 | µs | |

**Notes:**

- Page size= 252 bytes (non-authenticated), 236 bytes (authenticated).
- Only page reads and writes allowed.
- $T_{PUF\_OVHD}$ is an additional time that occurs on the first R/W, after cold or warm boot, to sNVM using authenticated or authenticated and encrypted text.

### 7.6.10 Secure NVM Programming Cycles

The following table describes secure NVM programming cycles.

**Table 91 • sNVM Programming Cycles vs. Retention Characteristics**

| Programming Temperature | Programming Cycles per Page, Max | Programming Cycles per Block, Max | Retention Years |
|---|---|---|---|
| –40 °C to 100 °C | 10,000 | 100,000 | 20 |
| –40 °C to 85 °C | 10,000 | 100,000 | 20 |
| –40 °C to 55 °C | 10,000 | 100,000 | 20 |

**Note:** Page size = 128 bytes. Block size = 56 KBytes.

4. See Authentication Services Time (see page 65).
5. See Verify Services Time (see page 64).
6. Throughputs described are measured from SS_REQ assertion to BUSY de-assertion.

## 7.8 Fabric Macros

This section describes switching characteristics of UJTAG, UJTAG_SEC, USPI, system controller, and temper detectors and dynamic reconfiguration details.
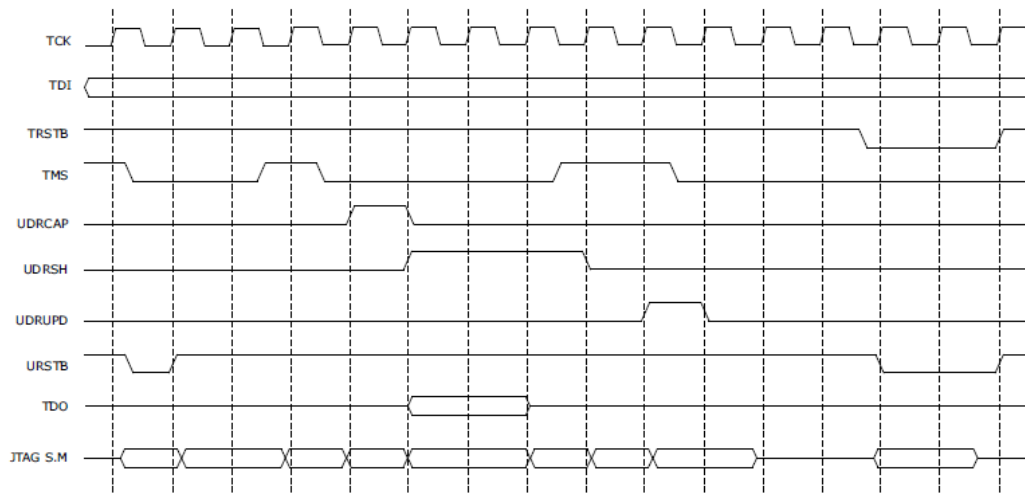
### 7.8.1 UJTAG Switching Characteristics

The following section describes characteristics of UJTAG switching.

**Table 93 • UJTAG Performance Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| TCK frequency | $F_{TCK}$ | | | 25 | MHz | |

**Figure 3 • UJTAG Timing Diagram**



### 7.8.2 UJTAG_SEC Switching Characteristics

The following table describes characteristics of UJTAG_SEC switching.

**Table 94 • UJTAG Security Performance Characteristics**

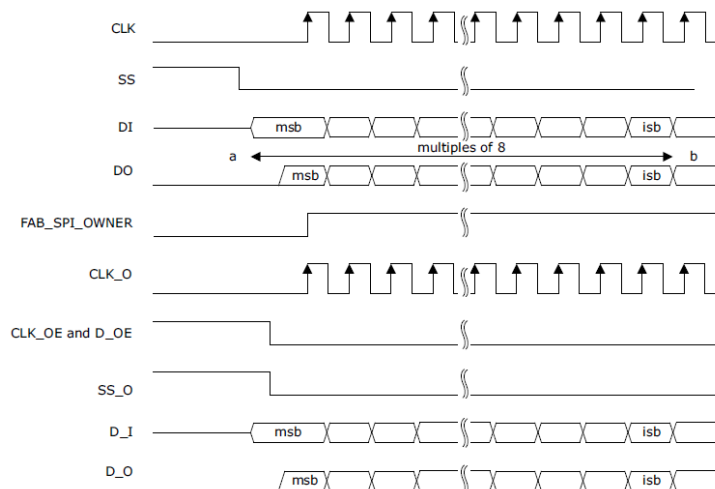| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| TCK frequency | $F_{TCK}$ | | | | MHz | |

### 7.8.3 USPI Switching Characteristics

The following section describes characteristics of USPI switching.

**Table 95 • SPI Macro Interface Timing Characteristics**

| Parameter | Symbol | $V_{DDI}$ = 3.3 V Max | $V_{DDI}$ = 2.5 V Max | $V_{DDI}$ = 1.8 V Max | $V_{DDI}$ = 1.5 V Max | $V_{DDI}$ = 1.2 V Max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay from the fabric to pins[1] | TPD_MOSI | 0.8 | 1 | 1.2 | 1.4 | 1.6 | ns |
| | TPD_MISO | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SS | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SCK | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_MOSI_OE | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SS_OE | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |
| | TPD_SCK_OE | 3.5 | 3.75 | 4 | 4.25 | 4.5 | ns |

1. Assumes CL of the relevant I/O standard as described in the input and output delay measurement tables.

**Figure 4 • USPI Switching Characteristics**



### 7.8.4 Tamper Detectors

The following section describes tamper detectors.

**Table 96 • ADC Conversion Rate**

| Parameter | Description | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| $T_{CONV1}$ | Time from enable changing from zero to non-zero value to first conversion completes. Minimum value applies when POWEROFF = 0. | 350 | | 470 | µs |
| $T_{CONVN}$ | Time between subsequent channel conversions. | | 480 | | µs |
| $T_{SETUP}$ | Data channel and output to valid asserted. Data is held until next conversion completes, that is >480 µs. | 0 | | | ns |
| $T_{VALID}$[2] | Width of the valid pulse. | 1.5 | | 2.5 | µs |

| Parameter | Description | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|
| $T_{RATE}$ | Time from start of first set of conversions to the start of the next set. Can be considered as the conversion rate. Is set by the conversion rate parameter. | | Rate × 32 | | µs |

1. Min, typ, and max refer to variation due to functional configuration and the raw TVS value. The actual internal correction time will vary based on the raw TVS value.
2. The pulse width varies depending on the time taken to complete the internal calibration multiplication, this can be up to 375 ns.

Note: Once the TVS block is active, the enable signal is sampled 25 ns before the falling edge of valid. The next enabled channel in the sequence 0-1-2-3 is started; that is, if channel 0 has just completed and only channels 0 and 3 are enabled, the next channel will be 3. When all the enabled channels in the sequence 0-1-2-3 are completed, the TVS waits for the conversion rate timer to expire. The enable signal may be changed at any time if it changes to 4'b0000 while valid is asserted (and 25 ns before valid is de-asserted), then no further conversions will be started.

**Table 97 • Temperature and Voltage Sensor Electrical Characteristics**

| Parameter | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|
| Temperature sensing range | −40 | | 125 | °C | |
| Temperature sensing accuracy | −10 | | 10 | °C | |
| Voltage sensing range | 0.9 | | 2.8 | V | |
| Voltage sensing accuracy | −3.0 | | 3.0 | % | |

**Table 98 • Tamper Macro Timing Characteristics—Flags and Clearing**

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| From event detection to flag generation | $T_{JTAG\_ACTIVE}$[1] | 28 | 35 | ns |
| | $T_{MESH\_ERR}$[1] | 1.8 | 2.5 | µs |
| | $T_{CLK\_GLITCH}$[1] | | 50 | ns |
| | $T_{CLK\_FREQ}$[1] | | 4 | µs |
| | $T_{LOW\_1P05}$[1, 3] | 70 | 1000 | µs |
| | $T_{HIGH\_1P8}$[1, 3] | 85 | 1000 | µs |
| | $T_{HIGH\_2P5}$[1, 3] | 130 | 1000 | µs |
| | $T_{GLITCH\_1P05}$[1] | | 20 | ns |
| | $T_{SECDEC}$[1] | | 5 | ns |
| | $T_{DRI\_ERR}$[1] | 14 | 18 | µs |
| | $T_{WDOG}$[1] | | 5 | ns |
| | $T_{LOCK\_ERR}$[1] | | 5 | ns |
| Time from system controller instruction execution to flag generation | $T_{INST\_BUF\_ACCESS}$[1, 2] | 4 | 5 | µs |
| | $T_{INST\_DEBUG}$[1, 2] | 3.3 | 4 | µs |
| | $T_{INST\_CHK\_DIGEST}$[1, 2] | 1.8 | 3 | µs |
| | $T_{INST\_EC\_SETUP}$[1, 2] | 1.8 | 2 | µs |
| | $T_{INST\_FACT\_PRIV}$[1, 2] | 3.8 | 5 | µs |
| | $T_{INST\_KEY\_VAL}$[1, 2] | 2.5 | 3.5 | µs |
| | $T_{INST\_MISC}$[1, 2] | 1.5 | 2 | µs |
| | $T_{INST\_PASSCODE\_MATCH}$[1, 2] | 2.5 | 3 | µs |
| | $T_{INST\_PASSCODE\_SETUP}$[1, 2] | 4.2 | 5 | µs |
| | $T_{INST\_PROG}$[1, 2] | 3.8 | 4.5 | µs |
| | $T_{INST\_PUB\_INFO}$[1, 2] | 4 | 4.5 | µs |
| | $T_{INST\_ZERO\_RECO}$[1, 2] | 2.5 | 3 | µs |
| | $T_{INST\_PASSCODE\_FAIL}$[1, 2] | 170 | 180 | µs |
| | $T_{INST\_KEY\_VAL\_FAIL}$[1, 2] | 92 | 110 | µs |
| | $T_{INST\_UNUSED}$[1, 2] | 4 | 5 | µs |
| Time from sending the CLEAR to deassertion on FLAG | $T_{CLEAR\_FLAG}$ | 17 | 23 | ns |

1. The timing does not impact the user design, but it is useful for security analysis.
2. System service requests from the fabric will interrupt the system controller delaying the generation of the flag.
3. Timing of these depends highly on supply ramp rate.

**Table 99 • Tamper Macro Response Timing Characteristics**

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Time from triggering the response to all I/Os disabled | $T_{IO\_DISABLE}$ | 45 | 63 | ns |
| Time from negation of RESPONSE to all I/Os re-enabled | $T_{CLR\_IO\_DISABLE}$ | 34 | 51 | ns |
| Time from triggering the response to security locked | $T_{LOCKDOWN}$ | | 20 | ns |
| Time from negation of RESPONSE to earlier security unlock condition | $T_{CLR\_LOCKDOWN}$ | | 20 | ns |
| Time from triggering the response to device enters RESET | $T_{tr\_RESET}$ | 11.7 | 14 | µs |

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Time from triggering the response to start of zeroization | $T_{tr\_ZEROLISE}$ | 7.4 | 8.2 | ms |

### 7.8.5 System Controller Suspend Switching Characteristics

The following table describes the characteristics of system controller suspend switching.

Table 100 • System Controller Suspend Entry and Exit Characteristics

| Parameter | Symbol | Definition | Typ | Max | Unit |
|---|---|---|---|---|---|
| Time from TRSTb falling edge to SUSPEND_EN signal assertion | $T_{suspend\_Tr}$[1, 2] | Suspend entry time from TRST_N assertion | 42 | 44 | ns |
| Time from TRSTb rising edge to ACTIVE signal assertion | $T_{suspend\_exit}$ | Suspend exit time from TRST_N negation | 361 | 372 | ns |

1. ACTIVE indicates that the system controller is inactive or active regardless of the state of SUSPEND_EN.
2. ACTIVE signal must never be asserted with SUSPEND_EN is asserted.

### 7.8.6 Dynamic Reconfiguration Interface

The following table provides interface timing information for the DRI, which is an embedded APB slave interface within the FPGA fabric that does not use FPGA resources.

Table 101 • Dynamic Reconfiguration Interface Timing Characteristics

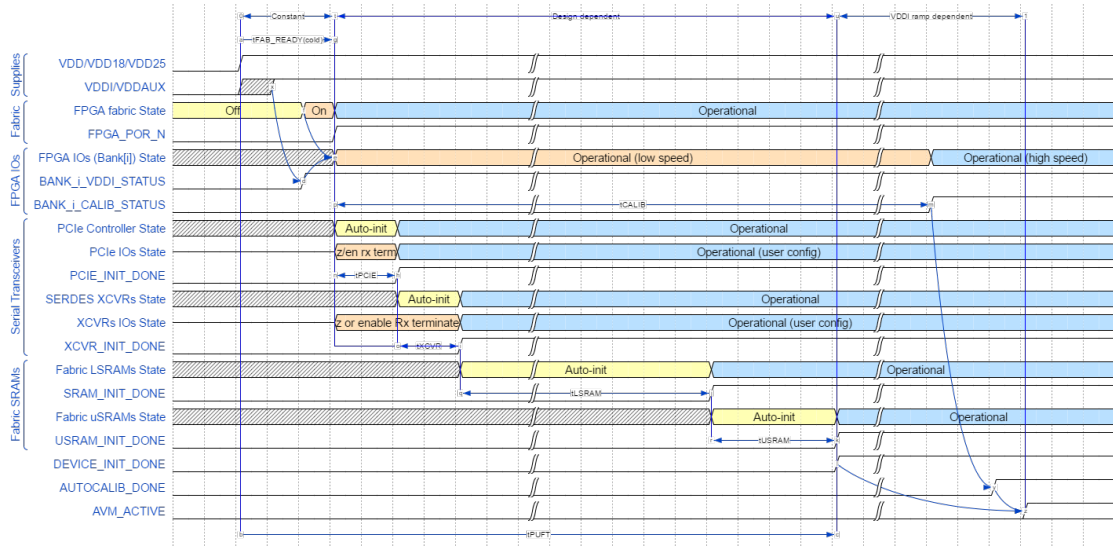| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| PCLK frequency | $F_{PD\_PCLK}$ | 200 | MHz |

## 7.9 Power-Up to Functional Timing

Microsemi non-volatile FPGA technology offers the fastest boot-time of any mid-range FPGA in the market. The following tables describes both cold-boot (from power-on) and warm-boot (assertion of DEVRST_N pin or assertion of reset from the tamper macro) timing. The power-up diagrams assume all power supplies to the device are stable.

### 7.9.1 Power-On (Cold) Reset Initialization Sequence

The following cold reset timing diagram shows the initialization sequencing of the device.

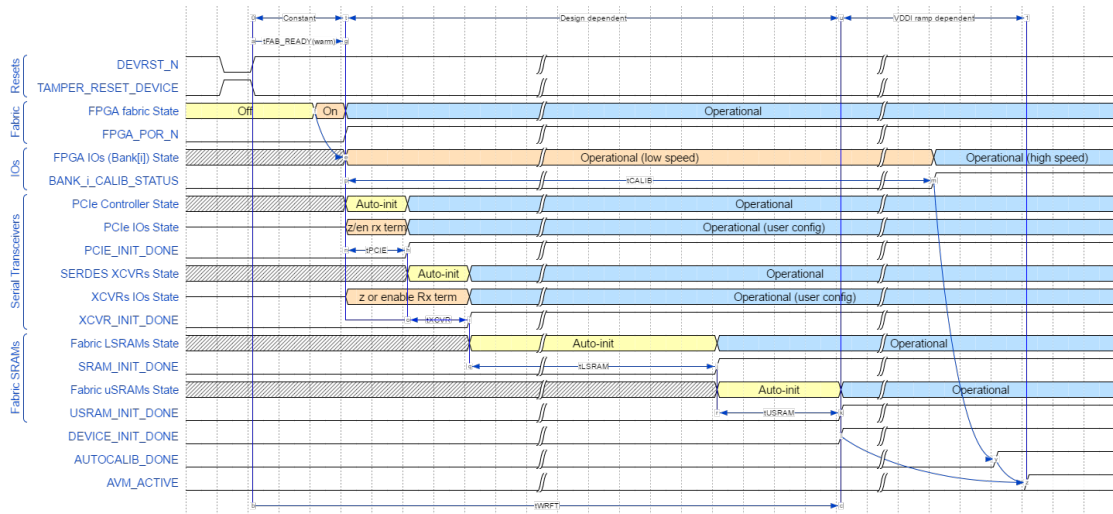**Figure 5 • Cold Reset Timing**



**Notes:**

- The previous diagram shows the case where VDDI/VDDAUX of I/O banks are powered either before or sufficiently soon after VDD/VDD18/VDD25 that the I/O bank enable time is measured from the assertion time of VDD/VDD18/VDD25 (that is, the PUFT specification). If VDDI/VDDAUX of I/O banks are powered sufficiently after VDD/VDD18/VDD25, then the I/O bank enable time is measured from the assertion of VDDI/VDDAUX and is not specified by the PUFT specification. In this case, I/O operation is indicated by the assertion of BANK_i_VDDI_STATUS, rather than being measured relative to FABRIC_POR_N negation.
- AUTOCALIB_DONE assertion indicates the completion of calibration for any I/O banks specified by the user for auto-calibration. AUTOCALIB_DONE asserts independently of DEVICE_INIT_DONE. It may assert before or after DEVICE_INIT_DONE and is determined by the following:
  - How long after VDD/VDD18/VDD25 that VDDI/VDDAUX are powered on. Note that if any of the user-specified I/O banks are not powered on within the auto-calibration timeout window, then AUTOCALIB_DONE doesn't assert until after this timeout.
  - The specified ramp times of VDDI of each I/O bank designated for auto-calibration.
  - How much auto-initialization is to be performed for the PCIe, SERDES transceivers, and fabric LSRAMs.
- If any of the I/O banks specified for auto-calibration do not have their VDDI/VDDAUX powered on within the auto-calibration timeout window, then it will be approximately auto-calibrated whenever VDDI/VDDAUX is subsequently powered on. To obtain an accurate calibration however, on such IO banks, it is necessary to initiate a re-calibration (using CALIB_START from fabric).
- AVM_ACTIVE only asserts if avionics mode is being used. It is asserted when the later of DEVICE_INIT_DONE or AUTOCALIB_DONE assert.

## 7.9.2 Warm Reset Initialization Sequence

The following warm reset timing diagram shows the initialization sequencing of the device when either DEVRST_N or TAMPER_RESET_DEVICE signals are asserted.

**Figure 6 • Warm Reset Timing**



## 7.9.3 Power-On Reset Voltages

The following sections describe the power-on reset voltages.

### 7.9.3.1 Main Supplies

The start of power-up to functional time ($T_{PUFT}$) is defined as the point at which the latest of the main supplies (VDD, VDD18, VDD25) reach the reference voltage levels specified in the following table. This starts the process of releasing the reset of the device and powering on the FPGA fabric and IOs.

**Table 102 • POR Ref Voltages**

| Supply | Power-On Reset Start Point (V) | Note |
|--------|-------------------------------|------|
| VDD    | 0.95                          | Applies to both 1.0 V and 1.05 V operation. |
| VDD18  | 1.71                          | |
| VDD25  | 2.25                          | |

### 7.9.3.2 I/O-Related Supplies

For the I/Os to become functional (for low speed, sub 400 MHz operation), the (per-bank) I/O supplies (VDDI, VDDAUX) must reach the trip point voltage levels specified in the following table and the main supplies above must also be powered on.

**Table 103 • I/O-Related Supplies**

| Supply | I/O Power-Up Start Point (V) |
|--------|------------------------------|
| VDDI   | 0.85                         |
| VDDAUX | 1.6                          |

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other IO supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the IO supplies of some IO banks remain powered off).

### 7.9.4    User Design Dependence of Power-Up Times

Some phases of the device initialization are user design-dependent, as the device automatically initializes certain resources to user-specified configurations if those resources are used in the design. It is necessary to compute the overall power-up to functional time by referencing the following tables and adding the relevant phases, according to the design configuration. The following equation refers to timing parameters specified in the above timing diagrams. Please note $T_{PCIE}$, $T_{XCVR}$, $T_{LSRAM,}$ and $T_{USRAM}$ can be found in the PolarFire FPGA device power-up and resets user guide UG0725.

$$T_{PUFT} = T_{FAB\_READY(cold)} + max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$$

$$T_{WRFT} = T_{FAB\_READY(warm)} + max((T_{PCIE} + T_{XCVR} + T_{LSRAM} + T_{USRAM}), T_{CALIB})$$

Note: $T_{PCIE}$, $T_{XCVR}$, $T_{LSRAM}$, $T_{USRAM}$, and $T_{CALIB}$ are common to both cold and warm reset scenarios.

Auto-initialization of FPGA (if required) occurs in parallel with I/O calibration. The device may be considered fully functional only when the later of these two activities has finished, which may be either one, depending on the configuration, as may be calculated from the following tables. Note that I/O calibration may extend beyond $T_{PUFT}$ (as I/O calibration process is independent of main device power-on and is instead dependent on I/O bank supply relative power-on time and ramp times). The previous timing diagram for power-on initialization shows the earliest that I/Os could be enabled, if the I/O power supplies are powered on before or at the same time as the main supplies.

### 7.9.5    Cold Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the power supplies reaching the above trip point levels until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

**Table 104 • Cold Boot**

| Power-On (Cold) Reset to Fabric and I/O Operational | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Time when input pins start working – $T_{IN\_ACTIVE(cold)}$ | 0.92 | 4.38 | 7.84 | ms |
| Time when weak pull-ups are enabled – $T_{PU\_PD\_ACTIVE(cold)}$ | 0.92 | 4.38 | 7.84 | ms |
| Time when fabric is operational – $T_{FAB\_READY(cold)}$ | 0.95 | 4.41 | 7.87 | ms |
| Time when output pins start driving – $T_{OUT\_ACTIVE(cold)}$ | 0.97 | 4.43 | 7.89 | ms |

### 7.9.6    Warm Reset to Fabric and I/Os (Low Speed) Functional

The following table specifies the minimum, typical, and maximum times from the negation of the warm reset event until the FPGA fabric is operational and the FPGA IOs are functional for low-speed (sub 400 MHz) operation.

**Table 105 • Warm Boot**

| Warm Reset to Fabric and I/O Operational | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Time when input pins start working – $T_{IN\_ACTIVE(warm)}$ | 0.65 | 1.63 | 2.62 | ms |
| Time when weak pull-ups/pull-downs are enabled – $T_{PU\_PD\_ACTIVE(warm)}$ | 0.65 | 1.63 | 2.62 | ms |
| Time when fabric is operational – $T_{FAB\_READY(warm)}$ | 0.68 | 1.66 | 2.65 | ms |
| Time when output pins start driving – $T_{OUT\_ACTIVE(warm)}$ | 0.70 | 1.68 | 2.67 | ms |

### 7.9.7    Miscellaneous Initialization Parameters

In the following table, $T_{FAB\_READY}$ refers to either $T_{FAB\_READY(cold)}$ or $T_{FAB\_READY(warm)}$ as specified in the previous tables, depending on whether the initialization is occurring as a result of a cold or warm reset, respectively.

### Table 106 • Cold and Warm Boot

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| The time from T$_{FAB\_READY}$ to ready to program through JTAG/SPI-Slave | | 0 | 0 | 0 | ms | |
| The time from T$_{FAB\_READY}$ to auto-update start | | | T$_{PUF\_OVHD}$[1] | T$_{PUF\_OVHD}$[1] | ms | |
| The time from T$_{FAB\_READY}$ to programming recovery start | | | T$_{PUF\_OVHD}$[1] | T$_{PUF\_OVHD}$[1] | ms | |
| The time from T$_{FAB\_READY}$ to the tamper flags being available | T$_{TAMPER\_READY}$ | 0 | 0 | 0 | ms | |
| The time from T$_{FAB\_READY}$ to the Athena Crypto co-processor being available (for S devices only) | T$_{CRYPTO\_READY}$ | 0 | 0 | 0 | ms | |

1. Programming depends on the PUF to power up. Refer to T$_{PUF\_OVHD}$ at section Secure NVM Performance (see page 65).

## 7.9.8 I/O Calibration

The following tables specify the initial I/O calibration time for the fastest and slowest supported VDDI ramp times of 0.2 ms to 50 ms, respectively. This only applies to I/O banks specified by the user to be auto-calibrated.

### Table 107 • I/O Initial Calibration Time (TCALIB)

| Ramp Time | Min (ms) | Max (ms) | Condition |
|---|---|---|---|
| 0.2 ms | 0.98 | 2.63 | Applies to HSIO and GPIO banks |
| 50 ms | 41.62 | 62.19 | Applies to HSIO and GPIO banks |

**Notes:**

- The user may specify any VDDI ramp time in the range specified above. The nominal initial calibration time is given by the specified VDDI ramp time plus 2 ms.
- In order for IO calibration to start, VDDI and VDDAUX of the I/O bank must be higher than the trip point levels specified in I/O-Related Supplies (see page 73).

### Table 108 • I/O Fast Recalibration Time (TRECALIB)

| I/O Type | Min (ms) | Typ (ms) | Max (ms) | Condition |
|---|---|---|---|---|
| GPIO bank | 0.04 | 0.14 | 0.24 | GPIO configured for 3.3 V operation |
| HSIO bank | 0.11 | 0.20 | 0.30 | HSIO configured for 1.8 V operation |

**Note:** In order to obtain fast re-calibration, the user must assert the relevant clock request signal from the FPGA fabric to the I/O bank controller.

## 7.10 Dedicated Pins

The following section describes the dedicated pins.

### 7.10.1 JTAG Switching Characteristics

The following table describes characteristics of JTAG switching.

**Table 109 • JTAG Electrical Characteristics**

| Symbol | Description | Min | Typ | Max | Unit | Condition |
|--------|-------------|-----|-----|-----|------|-----------|
| $T_{DISU}$ | TDI input setup time | 0.0 | | | ns | |
| $T_{DIHD}$ | TDI input hold time | 2.0 | | | ns | |
| $T_{TMSSU}$ | TMS input setup time | 1.5 | | | ns | |
| $T_{TMSHD}$ | TMS input hold time | 1.5 | | | ns | |
| $F_{TCK}$ | TCK frequency | | | 25 | MHz | |
| $T_{TCKDC}$ | TCK duty cycle | 40 | | 60 | % | |
| $T_{TDOCQ}$ | TDO clock to Q out | | | 8.4 | ns | $C_{LOAD}$ = 40 pf |
| $T_{RSTBCQ}$ | TRSTB clock to Q out | | | 23.5 | ns | $C_{LOAD}$ = 40 pf |
| $T_{RSTBPW}$ | TRSTB min pulse width | 50 | | | ns | |
| $T_{RSTBREM}$ | TRSTB removal time | 0.0 | | | ns | |
| $T_{RSTBREC}$ | TRSTB recovery time | 12.0 | | | ns | |
| $CIN_{TDI}$ | TDI input pin capacitance | | | 5.3 | pf | |
| $CIN_{TMS}$ | TMS input pin capacitance | | | 5.3 | pf | |
| $CIN_{TCK}$ | TCK input pin capacitance | | | 5.3 | pf | |
| $CIN_{TRSTB}$ | TRSTB input pin capacitance | | | 5.3 | pf | |

### 7.10.2 SPI Switching Characteristics

The following tables describe characteristics of SPI switching.

**Table 110 • SPI Master Mode (PolarFire Master) During Programming**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|-----------|--------|-----|-----|-----|------|-----------|
| SCK frequency | $F_{MSCK}$ | | | 20 | MHz | |

**Table 111 • SPI Master Mode (PolarFire Master) During Device Initialization**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|-----------|--------|-----|-----|-----|------|-----------|
| SCK frequency | $F_{MSCK}$ | | | 40 | MHz | |

**Table 112 • SPI Slave Mode (PolarFire Slave)**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|-----------|--------|-----|-----|-----|------|-----------|
| SCK frequency | $F_{SSCK}$ | | | 80 | MHz | |

### 7.10.3 SmartDebug Probe Switching Characteristics

The following table describes characteristics of SmartDebug probe switching.

**Table 113 • SmartDebug Probe Performance Characteristics**

| Parameter | Symbol | V$_{DD}$ = 1.0 V STD | V$_{DD}$ = 1.0 V – 1 | V$_{DD}$ = 1.05 V STD | V$_{DD}$ = 1.05 V – 1 | Unit |
|---|---|---|---|---|---|---|
| Maximum frequency of probe signal | F$_{MAX}$ | 100 | 100 | 100 | 100 | MHz |
| Minimum delay of probe signal | T$_{Min\_delay}$ | | | | | ns |
| Maximum delay of probe signal | T$_{Max\_delay}$ | | | | | ns |

### 7.10.4 DEVRST_N Switching Characteristics

The following table describes characteristics of DEVRST_N switching.

**Table 114 • DEVRST_N Electrical Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| DEVRST_N ramp rate | DR$_{RAMP}$ | | 10 | | µs | It must be a normal clean digital signal, with typical rise and fall times |
| DEVRST_N assert time | DR$_{ASSERT}$ | 1 | | | µs | The minimum time for DEVRST_N assertion to be recognized |
| DEVRST_N de-assert time | DR$_{DEASSERT}$ | 2.75 | | | ms | The minimum time DEVRST_N needs to be de-asserted before assertion |

## 7.11 User Crypto

The following section describes user crypto.

### 7.11.1 TeraFire 5200B Switching Characteristics

The following table describes TeraFire 5200B switching characteristics.

**Table 115 • TeraFire F5200B Switching Characteristics**

| Parameter | Symbol | VDD = 1.0 V STD | VDD = 1.0 V – 1 | VDD = 1.05 V STD | VDD = 1.05 V – 1 | Unit | Condition |
|---|---|---|---|---|---|---|---|
| F$_{MAX}$ with DLL | F$_{MAX\_DLL}$ | 189 | 189 | 189 | 189 | MHz | –40 °C to 100 °C |
| F$_{MIN}$ with DLL | F$_{MIN\_DLL}$ | 125 | 125 | 125 | 125 | MHz | –40 °C to 100 °C |
| F$_{MAX}$ with DLL in bypass mode | F$_{MAX\_DLL\_BYPASS}$ | 70 | 70 | 70 | 70 | MHz | –40 °C to 100 °C |
| F$_{MIN}$ with DLL in bypass mode | F$_{MIN\_DLL\_BYPASS}$ | 0 | 0 | 0 | 0 | MHz | –40 °C to 100 °C |

### 7.11.2 TeraFire 5200B Throughput Characteristics

The following tables for each algorithm describe the TeraFire 5200B throughput characteristics.

**Note:** Throughput cycle count collected with Athena TeraFire Core and RISCV running at 70 MHz.

**Table 116 • AES**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| AES-ECB-128 encrypt[1] | 128 | 515 | 1095 |
|  | 64K | 50157 | 933 |
| AES-ECB-128 decrypt[1] | 128 | 557 | 1760 |
|  | 64K | 48385 | 1524 |
| AES-ECB-256 encrypt[1] | 128 | 531 | 1203 |
|  | 64K | 58349 | 1203 |
| AES-ECB-256 decrypt[1] | 128 | 589 | 1676 |
|  | 64K | 56673 | 1671 |
| AES-CBC-256 encrypt[1] | 128 | 576 | 1169 |
|  | 64K | 52547 | 1169 |
| AES-CBC-256 decrypt[1] | 128 | 585 | 1744 |
|  | 64K | 48565 | 1652 |
| AES-GCM-128 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1925 | 2740 |
|  | 64K | 60070 | 2158 |
| AES-GCM-256 encrypt[1], 128-bit tag, (full message encrypted/authenticated) | 128 | 1973 | 2268 |
|  | 64K | 60102 | 2151 |

1. With DPA counter measures.

**Table 117 • GMAC**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| AES-GCM-256[1], 128-bit tag, (message is only authenticated) | 128 | 1863 | 2211 |
|  | 64K | 49707 | 2128 |

1. With DPA counter measures.

### Table 118 • HMAC

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| HMAC-SHA-256[1], 256-bit key | 512 | 7477 | 2361 |
| | 64K | 88367 | 2099 |
| HMAC-SHA-384[1], 384-bit key | 1024 | 13049 | 2257 |
| | 64K | 106103 | 2153 |

1. With DPA counter measures.

### Table 119 • CMAC

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| AES-CMAC-256[1] (message is only authenticated) | 128 | 446 | 9058 |
| | 64K | 45494 | 111053 |

1. With DPA counter measures.

### Table 120 • KEY TREE

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| 128-bit nonce + 8-bit optype | | 102457 | 2751 |
| 256-bit nonce + 8-bit optype | | 103218 | 2089 |

### Table 121 • SHA

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| SHA-1[1] | 512 | 2386 | 1579 |
| | 64K | 77576 | 990 |
| SHA-256[1] | 512 | 2516 | 884 |
| | 64K | 84752 | 938 |
| SHA-384[1] | 1024 | 4154 | 884 |
| | 64K | 100222 | 938 |
| SHA-512[1] | 1024 | 4154 | 881 |
| | 64K | 100222 | 935 |

1. With DPA counter measures.

### Table 122 • ECC

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| ECDSA SigGen, P-384/SHA-384[1] | 1024 | 12528912 | 6944 |
| | 8K | 12540448 | 5643 |
| ECDSA SigGen, P-384/SHA-384 | 1024 | 5502928 | 6155 |
| | 1024 | 6421841 | 5759 |
| | 8K | 6273510 | 5759 |

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| Key Agreement (KAS), P-384 | | 5039125 | 6514 |
| Point Multiply, P-256[1] | | 5176923 | 4482 |
| Point Multiply, P-384[1] | | 12043199 | 5319 |
| Point Multiply, P-521[1] | | 26887187 | 6698 |
| Point Addition, P-384 | | 3018067 | 5779 |
| KeyGen (PKG), P-384 | | 12055368 | 6908 |
| Point Verification, P-384 | | 5091 | 3049 |

1. With DPA counter measures.

## Table 123 • IFC (RSA)

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| Encrypt, RSA-2048, e=65537 | 2048 | 436972 | 8,972 |
| Encrypt, RSA-3072, e=65537 | 3072 | 962162 | 12,583 |
| Decrypt, RSA-2048[1], CRT | 2048 | 26862392 | 15900 |
| Decrypt, RSA-3072[1], CRT | 3072 | 75153782 | 22015 |
| Decrypt, RSA-4096, CRT | 4096 | 89235615 | 23710 |
| Decrypt, RSA-3072, CRT | 3072 | 37880180 | 18638 |
| SigGen, RSA-3072/SHA-384[1],CRT, PKCS #1 V 1 1.5 | 1024 | 75197644 | 20032 |
| | 8K | 75213653 | 19303 |
| SigGen, RSA-3072/SHA-384, PKCS #1, V 1.5 | 1024 | 148090970 | 14642 |
| | 8K | 148102576 | 13936 |
| SigVer, RSA-3072/SHA-384, e = 65537, PKCS #1 V 1.5 | 1024 | 970991 | 12000 |
| | 8K | 982011 | 11769 |
| SigVer, RSA-2048/SHA-256, e = 65537, PKCS #1 V 1.5 | 1024 | 443493 | 8436 |
| | 8K | 453007 | 8436 |
| SigGen, RSA-3072/SHA-384, ANSI X9.31 | 1024 | 147138254 | 13945 |
| | 8K | 147155896 | 13523 |
| SigVer, RSA-3072/SHA-384, e = 65537, ANSI X9.31 | 1024 | 973269 | 11313 |
| | 8K | 983255 | 11146 |

1. With DPA counter measures.

**Table 124 • FFC (DH)**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| SigGen, DSA-3072/SHA-384[1] | 1024 | 27932907 | 13969 |
| | 8K | 27942415 | 13501 |
| SigGen, DSA-3072/SHA-384 | 1024 | 12086356 | 13602 |
| SigVer, DSA-3072/SHA-384 | 1024 | 24597916 | 15662 |
| | 8K | 24229420 | 15133 |
| SigVer, DSA-2048/SHA-256 | 1024 | 9810527 | 10884 |
| | 8K | 9597000 | 10719 |
| Key Agreement (KAS), DH-3072 (p=3072, security=256) | | 4920705 | 9338 |
| Key Agreement (KAS), DH-3072 (p=3072, security=256)[1] | | 78914533 | 9083 |

1. With DPA counter measures.

**Table 125 • NRBG**

| Modes | Message Size (bits) | Athena TeraFire Crypto Core Clock-Cycles | CAL Delay In CPU Clock-Cycles |
|---|---|---|---|
| Instantiate: strength, s=256, 384-bit nonce, 384-bit personalization string | | 18221 | 2841 |
| Reseed: no additional input, s=256 | | 13585 | 1180 |
| Reseed: 384-bit additional input, s=256 | | 15922 | 1342 |
| Generate: (no additional input), prediction resistance enabled, s= 256 | 128 | 15262 | 1755 |
| | 8K | 27169 | 8223 |
| Generate: (no additional input), prediction resistance disabled, s= 256 | 128 | 2138 | 1167 |
| | 8K | 14045 | 8223 |
| Generate: (384-bit additional input), prediction resistance enabled, s= 256 | 128 | 21299 | 1944 |
| | 8K | 33206 | 8949 |
| Generate: (384-bit additional input), prediction resistance disabled, s= 256 | 128 | 11657 | 1894 |
| | 8K | 23564 | 8950 |
| Un-instantiate | | 761 | 666 |

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www microsemi.com.

51700141