DS1080L

Spread-Spectrum Crystal Multiplier

General Description

The DS1080L is a low-jitter, crystal-based clock generator with an integrated phase-locked loop (PLL) to generate spread-spectrum clock outputs from 16MHz to 134MHz. The device is pin-programmable to select the clock multiplier rate as well as the dither magnitude. The DS1080L has a spread-spectrum disable mode and a power-down mode to conserve power.

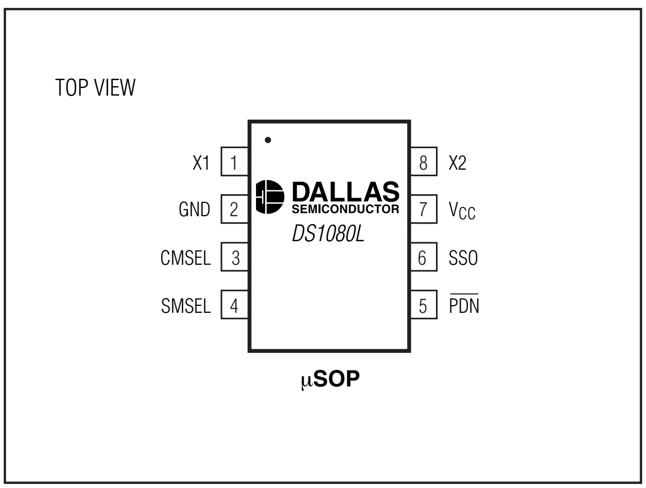
Applications

Automotive
Cable Modems
Cell Phones
Computer Peripherals
Copiers
Infotainment
PCs
Printers

Features

- **Generates Spread-Spectrum Clocks from 16MHz to 134MHz**
- **Selectable Clock Multiplier Rates of 1x, 2x, and 4x**
- **Center Spread-Spectrum Dithering**
- **Selectable Spread-Spectrum Modulation Magnitudes of ±0.5%, ±1.0%, and ±1.5%**
- **Spread-Spectrum Disable Mode**
- **Low Cycle-to-Cycle Jitter**
- **Power-Down Mode with High-Impedance Output**
- **Low Cost**
- **Low Power Consumption**
- **3.0V to 3.6V Single-Supply Operation**
- **-40°C to +125°C Temperature Operation**
- **Small 8-Lead µSOP Package**

Pin Configuration



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1080L+	-40°C to +125°C	8 µSOP

+Denotes lead-free package.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Spread-Spectrum Crystal Multiplier

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} Relative to GND ....-0.5V to +3.63V
Voltage on Any Lead Relative
to GND ....-0.5V to (V_{CC} + 0.5V), not to exceed +3.63V
Operating Temperature Range ....-40°C to +125°C
Storage Temperature Range ....-55°C to +125°C
Soldering Temperature..................See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +125°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	3.0		3.6	V
Input Logic 1	V_{IH}		0.8 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		GND - 0.3		0.2 x V_{CC}	V
Input Logic Float	I_{IF}	0v < V_{IN} < V_{CC} (Note 2)			±1	µA
Input Leakage	I_{IL}	0V < V_{IN} < V_{CC} (Note 3)			±80	µA
SSO Load	C_{SSO}	SSO < 67MHz			15	pF
		67MHz ≤ SSO < 101MHz			10	
		101MHz ≤ SSO < 134MHz			7	
Crystal or Clock Input Frequency	f_{IN}		16.0		33.4	MHz
Crystal ESR	X_{ESR}				90	Ω
Clock Input Duty Cycle	F_{INDC}		40		60	%
Crystal Parallel Load Capacitance	C_L	(Note 4)			18	pF

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +125°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC1}	C_{SSO} = 15pF, SSO = 16MHz			13	mA
Power-Down Current	I_{CCQ}	$\overline{PDN}$ = GND, all input pins floating			200	µA
Output Leakage (SSO)	I_{OZ}	$\overline{PDN}$ = GND	-1		+1	µA
Low-Level Output Voltage (SSO)	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Output Voltage (SSO)	V_{OH}	I_{OH} = -4mA	2.4			V
Input Capacitance (X1/X2)	C_{IN}	(Note 5)		5		pF

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0 to +3.6V, T_A = -40°C to +125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SSO Duty Cycle	SSODC	Measured at V_{CC} / 2		40		60	%
Rise Time	t_R	(Note 6)			1.6		ns
Fall Time	t_F	(Note 6)			1.6		ns
Peak Cycle-to-Cycle Jitter	t_J	f_{SSO} = 16MHz, T_A = -40 to +85°C, 10,000 cycles (Note 5)			75		ps
Power-Up Time	t_{POR}	$\overline{PDN}$ pin (Note 7)	16MHz			20	ms
			33.4MHz			11	
Power-Down Time	$t_{\overline{PDN}}$	$\overline{PDN}$ pin (Notes 8 and 9)				100	ns
Dither Rate	f_{DITHER}				f_{IN} / 1024		

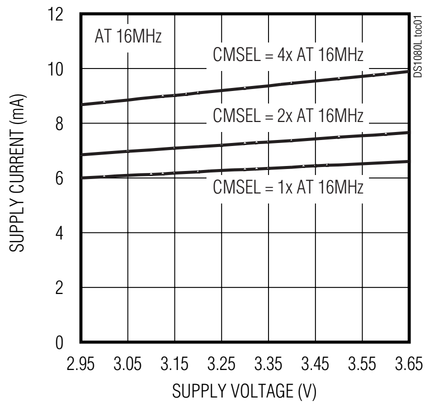
Note 1: All voltages referenced to ground.
Note 2: Maximum source/sink current applied to input to be considered a float.
Note 3: Applicable to pins CMSEL, SMSEL, and $\overline{PDN}$.
Note 4: See information about C_{L1} and C_{L2} in the *Applications Information* section at the end of the data sheet.
Note 5: Not production tested.
Note 6: For 7pF load.
Note 7: Time between $\overline{PDN}$ deasserted to output active.
Note 8: Time between $\overline{PDN}$ asserted to output high impedance.
Note 9: Guaranteed by design.

Spread-Spectrum Crystal Multiplier

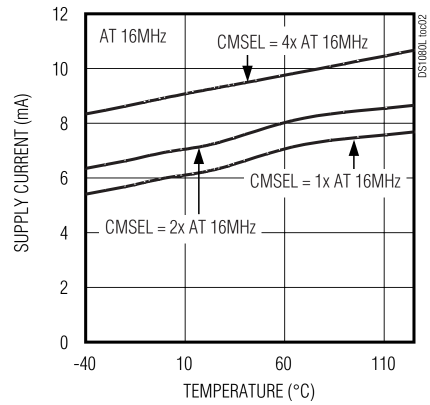
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

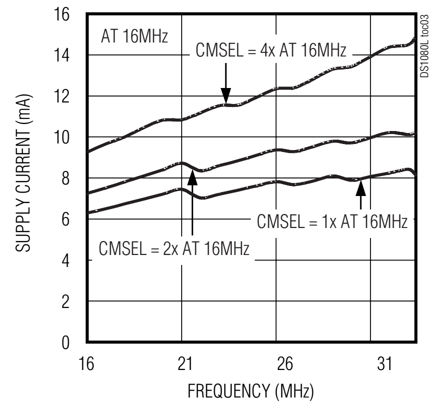
SUPPLY CURRENT vs. SUPPLY VOLTAGE



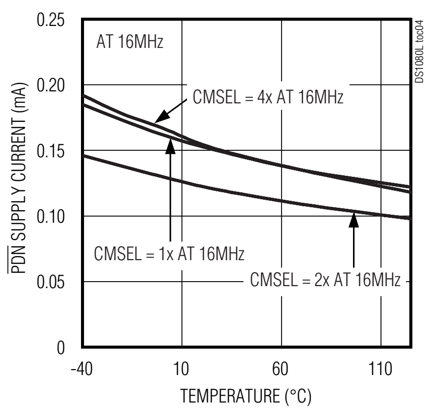
SUPPLY CURRENT vs. TEMPERATURE



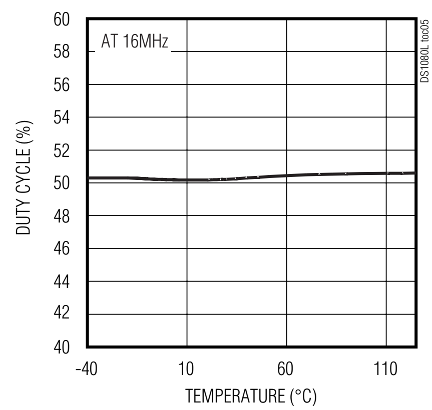
SUPPLY CURRENT vs. FREQUENCY



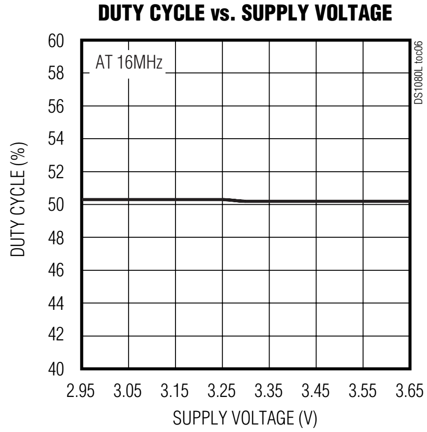
$\overline{PDN}$ SUPPLY CURRENT vs. TEMPERATURE



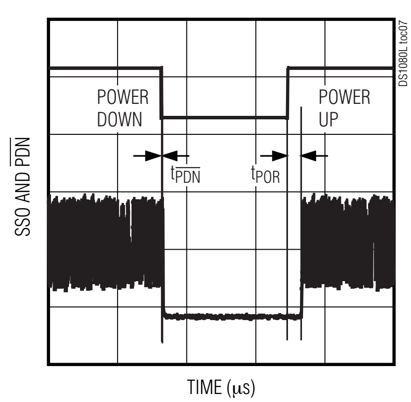
DUTY CYCLE vs. TEMPERATURE



DUTY CYCLE vs. SUPPLY VOLTAGE



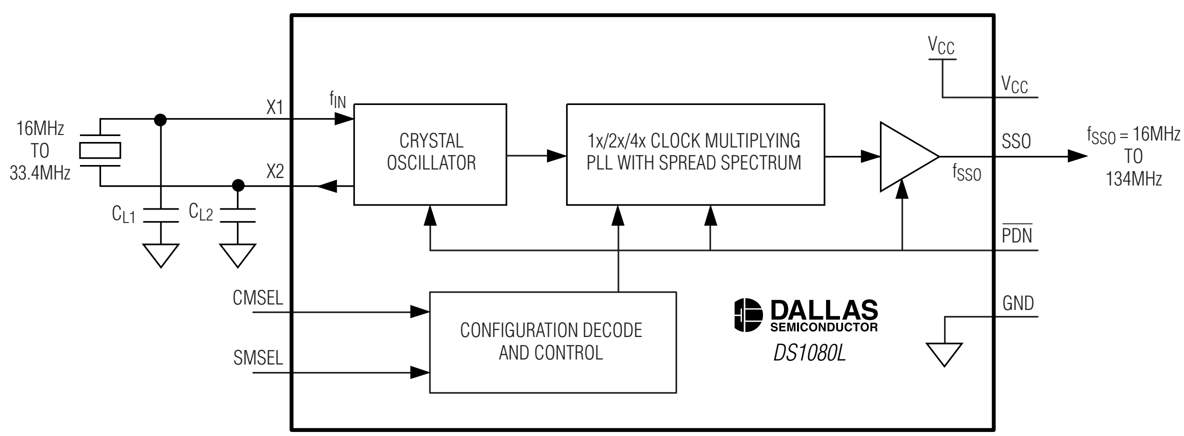
OUTPUT DURING POWER UP AND POWER DOWN



Pin Description

PIN	NAME	FUNCTION
1	X1	Crystal Drive/Clock Input. A crystal with the proper loading capacitors is connected across X1 and X2. Instead of a crystal, a clock can be applied at the X1 input.
2	GND	Signal Ground
3	CMSEL	Clock Multiplier Select. Tri-level digital input. 0 = 1x Float = 2x 1 = 4x
4	SMSEL	Spread-Spectrum Magnitude Select. Tri-level digital input. 0 = ±0.5% Float = ±1.0% 1 = ±1.5%
5	$\overline{PDN}$	Power-Down/Spread-Spectrum Disable. Tri-level digital input. 0 = Power-Down/SSO Tri-Stated Float = Power-Up/Spread Spectrum Disabled 1 = Power-Up/Spread Spectrum Enabled
6	SSO	Spread-Spectrum Clock Multiplier Output. Outputs a 1x, 2x, or 4x spread-spectrum version of the crystal or clock applied at the X1/X2 pins.
7	V_{CC}	Supply Voltage
8	X2	Crystal Drive Output. A crystal with the proper loading capacitors is connected across X1 and X2. If a clock is connected to X1, then X2 should be left open circuit.

Block Diagram



NOTE: SEE INFORMATION ABOUT C_{L1} AND C_{L2} IN THE *APPLICATIONS INFORMATION* SECTION AT THE END OF THE DATA SHEET.

Detailed Description

The DS1080L is a crystal multiplier with center spread-spectrum capability. A 16MHz to 33.4MHz crystal is connected to the X1 and X2 pins. Alternately, a 16MHz to 33.4MHz clock can be applied to X1 in place of the crystal. In such applications, X2 would be left open circuit. Using the CMSEL input, the user selects whether the attached crystal or input clock is multiplied by 1, 2, or 4. The DS1080L is capable of generating spread-spectrum clocks from 16MHz to 134MHz.

The PLL can dither the output clock about its center frequency at a user-selectable magnitude. Using the SMSEL input, the user selects the dither magnitude. The $\overline{PDN}$ input can be used to place the device into a low-power standby mode where the SSO output is tri-stated. If the $\overline{PDN}$ pin is floated, the SSO output is active but the spread-spectrum dithering is disabled. The spread-spectrum dither rate is fixed at f_{IN} / 1024 to keep the dither rate above the audio frequency range. On power-up, the output clock (SSO) remains tri-stated until the PLL reaches a stable frequency (f_{SSO}) and dither (f_{DITHER}).

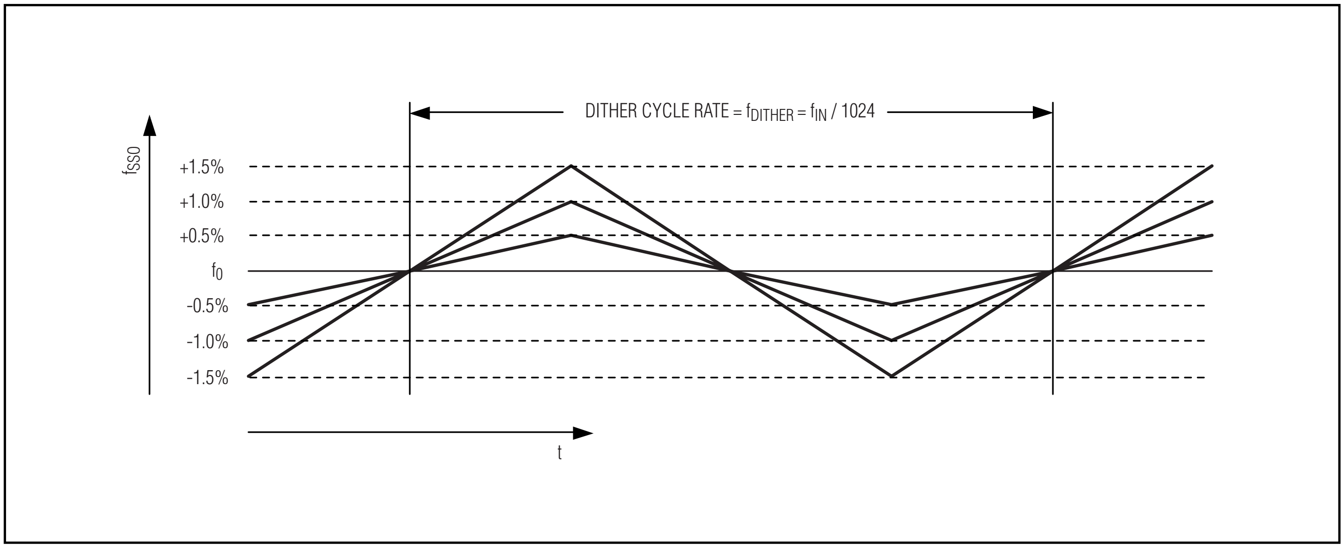
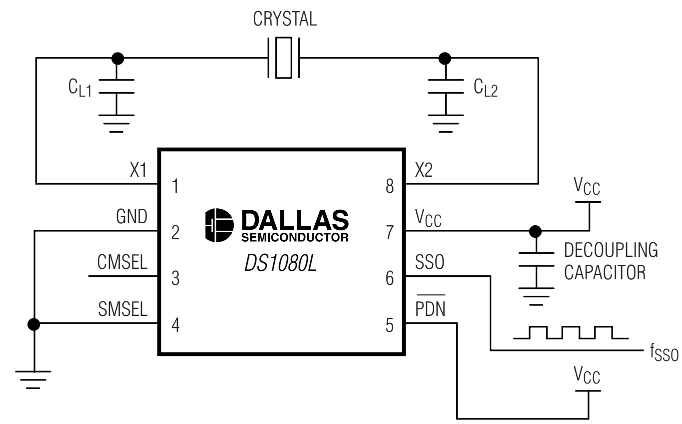


Figure 1. Spread-Spectrum Frequency Modulation

Typical Operating Circuit



NOTE: IN THE ABOVE CONFIGURATION WITH $\overline{PDN}$ CONNECTED TO V_{CC}, SMSEL CONNECTED TO GND AND CMSEL FLOATING, THE DEVICE IS IN NORMAL OPERATION WITH 2x CLOCK MULTIPLICATION, AND SPREAD-SPECTRUM MAGNITUDE OF ±0.5%.

Applications Information

Crystal Selection

The DS1080L requires a parallel resonating crystal operating in the fundamental mode, with an ESR of less than 90Ω. The crystal should be placed very close to the device to minimize excessive loading due to parasitic capacitances.

Oscillator Input

When driving the DS1080L using an external oscillator clock, consider the input (X1) to be high impedance.

Crystal Capacitor Selection

The load capacitors C_{L1} and C_{L2} are selected based on the crystal specifications (from the data sheet of the crystal used). The crystal parallel load capacitance is calculated as follows:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} C_{IN} \qquad \text{Equation 1}$$

For the DS1080L use $C_{L1} = C_{L2} = C_{LX}$.

In this case, the equation then reduces to:

$$C_L = \frac{C_{LX}}{2} + C_{IN} \qquad \text{Equation 2}$$

where $C_{L1} = C_{L2} = C_{LX}$.

Equation 2 is used to calculate the values of C_{L1} and C_{L2} based on values on C_L and C_{IN} noted in the data sheet electrical specifications.

Power-Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor is used on the IC power-supply pins. Typical values of decoupling capacitors are 0.001µF and 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the V_{CC} and GND pins of the IC to minimize lead inductance.

Layout Considerations

As noted earlier, the crystal should be placed very close to the device to minimize excessive loading due to parasitic capacitances. Care should also be taken to minimize loading on pins that could be floated as a programming option (SMSEL and CMSEL). Coupling on inputs due to clocks should be minimized.

Spread-Spectrum Crystal Multiplier

Chip Technology

TRANSISTOR COUNT: 3951

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.