National Semiconductor

April 2007

DS10BR150
1.0 Gbps LVDS Buffer / Repeater

General Description

The DS10BR150 is a single channel 1.0 Gbps LVDS buffer optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count and further minimize board space.

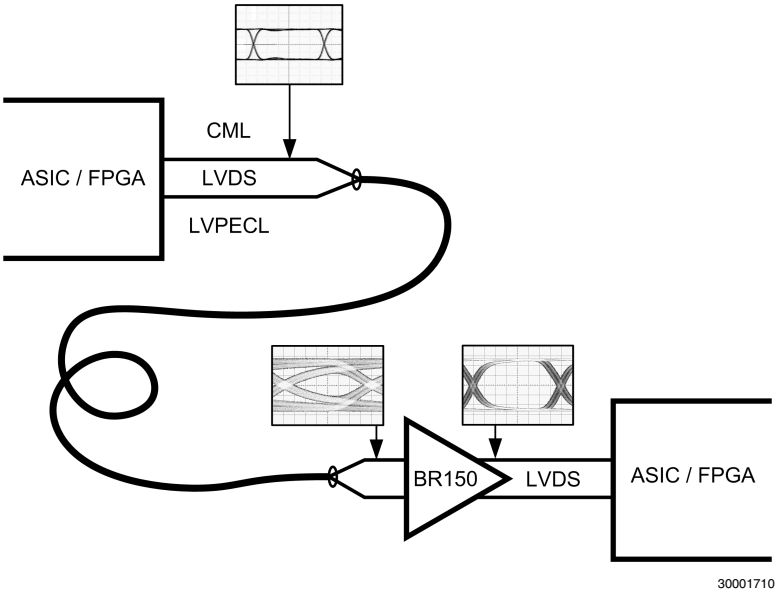
Features

- DC - 1.0 Gbps low jitter, high noise immunity, low power operation
- On-chip 100Ω input and output termination minimizes insertion and return losses, reduces component count and minimizes board space
- 7 kV ESD on LVDS I/O pins protects adjoining components
- Small 3 mm x 3 mm 8-LLP space saving package

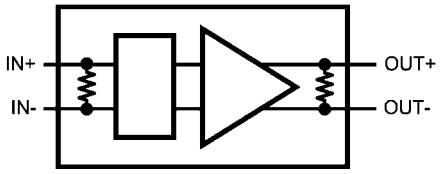
Applications

- Clock and data buffering
- OC-12 / STM-4
- Fibre Channel (1GFC)
- FireWire 800

Typical Application

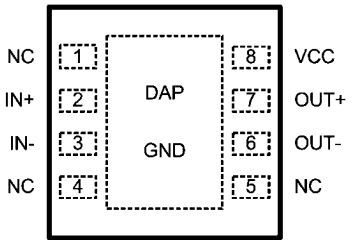


Block Diagram



30001701

Pin Diagram



30001702

Pin Descriptions

Pin Name	Pin Name	Pin Type	Pin Description
NC	1	NA	"NO CONNECT" pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
NC	4	NA	"NO CONNECT" pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)

Ordering Code

NSID	Function
DS10BR150TSD	Buffer / Repeater

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
LVDS Input Voltage (IN+, IN−)	−0.3V to +4V
LVDS Differential Input Voltage ((IN+) - (IN−))	0V to 1V
LVDS Output Voltage (OUT+, OUT−)	−0.3V to +4V
LVDS Differential Output Voltage ((OUT+) - (OUT−))	0V to 1V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
SDA Package	2.08W
Derate SDA Package	16.7 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+60.0°C/W
θ_{JC}	+12.3°C/W
ESD Susceptibility	
HBM	≥7 kV
MM	≥250V
CDM	≥1250V

Note 1: Human Body Model, applicable std. JESD22-A114C

Note 2: Machine Model, applicable std. JESD22-A115-A

Note 3: Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 6, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current (Note 8)	OUT to GND		-30	-50	mA
		OUT to V_{CC}		7.5	50	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT- Pins		100		Ω
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V_{ID}	Input Differential Voltage	V_{CM} = +0.05V or V_{CC}-0.05V	0		1	V
V_{TH}	Differential Input High Threshold			0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = 3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance			1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN- Pins		100		Ω
SUPPLY CURRENT						
I_{CCD}	Total Supply Current			16	21	mA

AC Electrical Characteristics (Note 9)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 5, 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t_{PHLD2}	Differential Propagation Delay High to Low	R_L = 100Ω			380	600	ps
t_{PLHD2}	Differential Propagation Delay Low to High				410	600	ps
t_{SKD1}	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ (Note 10)				30	150	ps
t_{SKD2}	Part to Part Skew (Note 11)				45	160	ps
t_{LHT}	Rise Time	R_L = 100Ω			165	400	ps
t_{HLT}	Fall Time				155	400	ps
JITTER PERFORMANCE (*Figure 5*)							
t_{DJ}	Deterministic Jitter (Peak-to-Peak Value) (Note 13)	V_{ID} = 350 mV V_{CM} = 1.2V K28.5 (NRZ)	622 Mbps		12	39	ps
			1.06 Gbps		15	42	ps
t_{RJ}	Random Jitter (RMS Value) (Note 12)	V_{ID} = 350 mV V_{CM} = 1.2V Clock (NRZ)	311 MHz		0.6	1.3	ps
			503 MHz		0.6	1.1	ps
t_{TJ}	Total Jitter (Peak to Peak Value) (Note 14)	V_{ID} = 350 mV V_{CM} = 1.2V PRBS-23 (NRZ)	622 Mbps		0.02	0.04	UI_{P-P}
			1.06 Gbps		0.02	0.05	UI_{P-P}

Note 4: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 5: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 6: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.

Note 7: Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 9: Specification is guaranteed by characterization and is not tested in production.

Note 10: t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 11: t_{SKD2}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

Note 12: Measured on a clock edge with a histogram and an acummulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

Note 13: Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

Note 14: Measured on an eye diagram with a histogram and an acummulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits

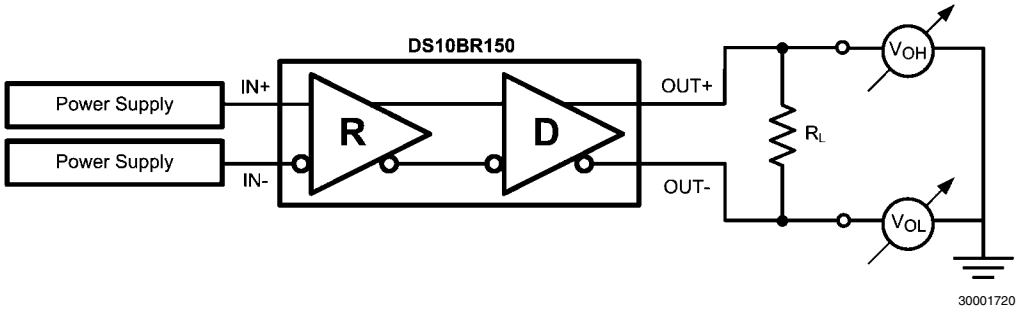


FIGURE 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

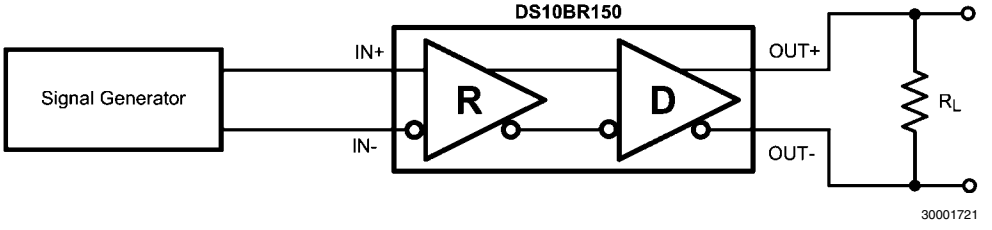


FIGURE 2. Differential Driver AC Test Circuit

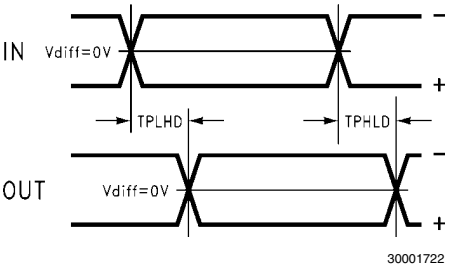


FIGURE 3. Propagation Delay Timing Diagram

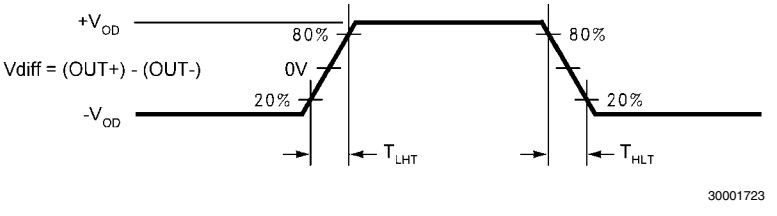


FIGURE 4. LVDS Output Transition Times

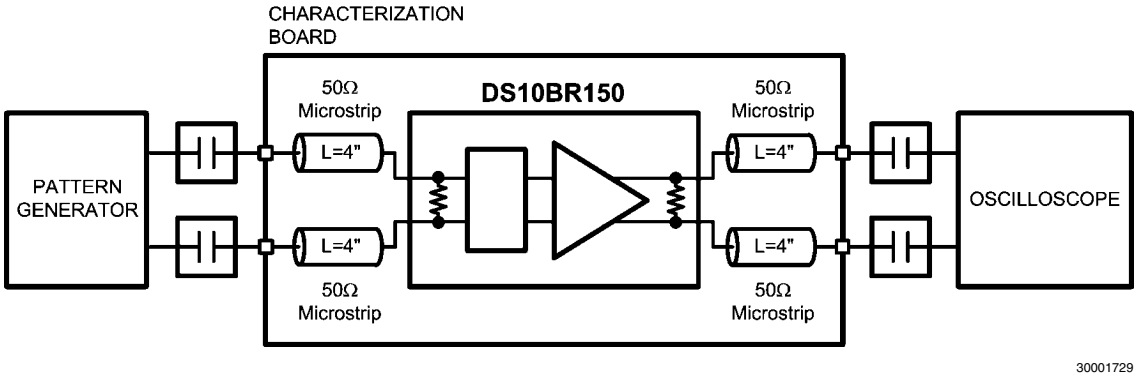
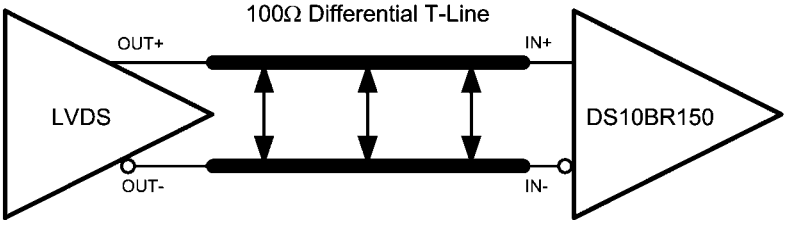


FIGURE 5. Jitter Measurements Test Circuit

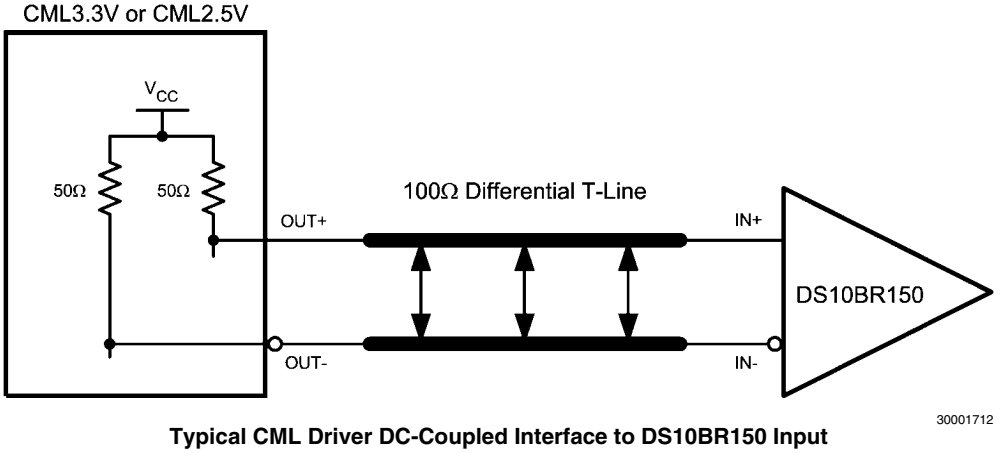
Device Operation

INPUT INTERFACING

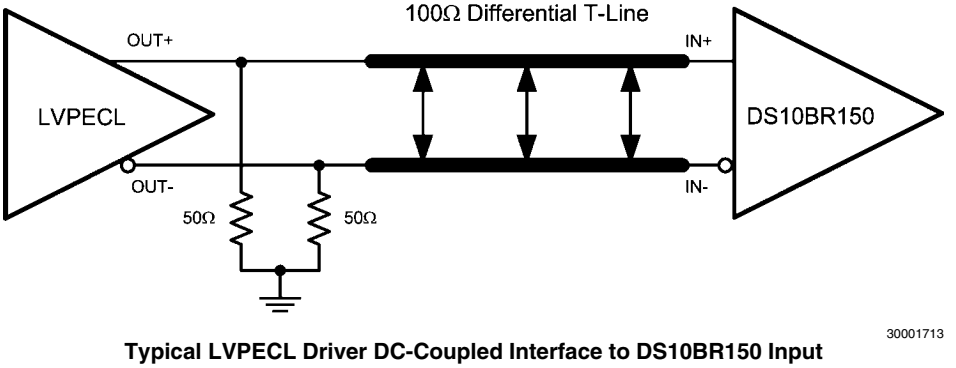
The DS10BR150 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS10BR150 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS10BR150 inputs are internally terminated with a 100Ω resistor.



Typical LVDS Driver DC-Coupled Interface to DS10BR150 Input



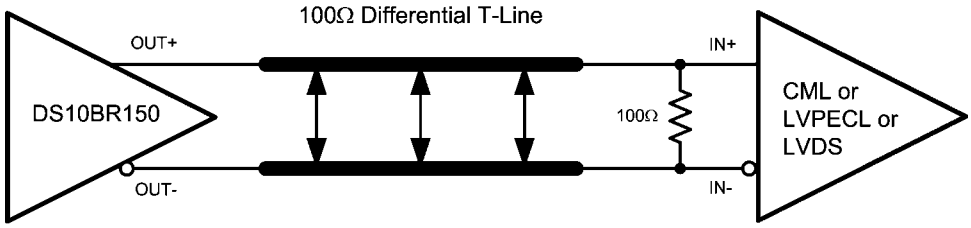
Typical CML Driver DC-Coupled Interface to DS10BR150 Input



Typical LVPECL Driver DC-Coupled Interface to DS10BR150 Input

OUTPUT INTERFACING

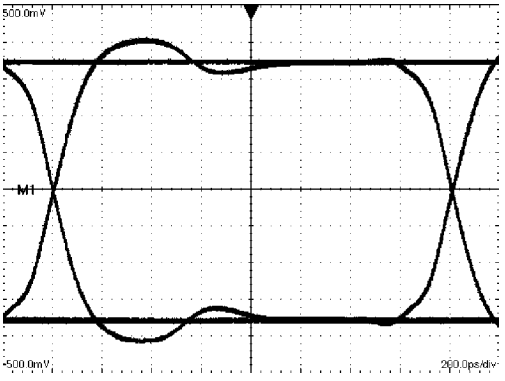
The DS10BR150 outputs signals are compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



30001714

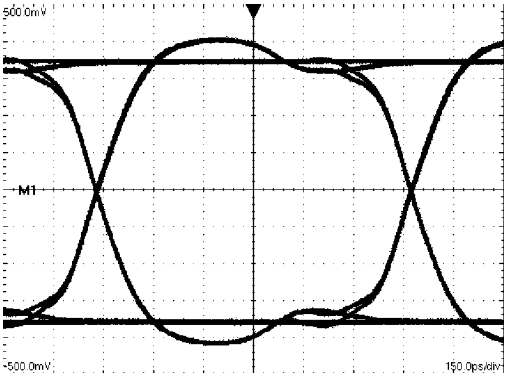
Typical DS10BR150 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance



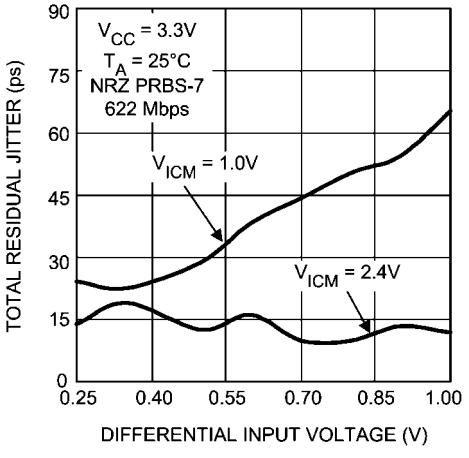
30001730

A 622 Mbps NRZ PRBS-7 Output Eye Diagram
V:100 mV / DIV, H:200 ps / DIV



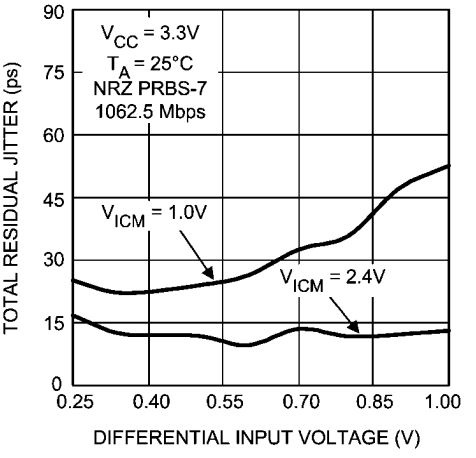
30001731

A 1062.5 Mbps NRZ PRBS-7 Output Eye Diagram
V:100 mV / DIV, H:150 ps / DIV



30001732

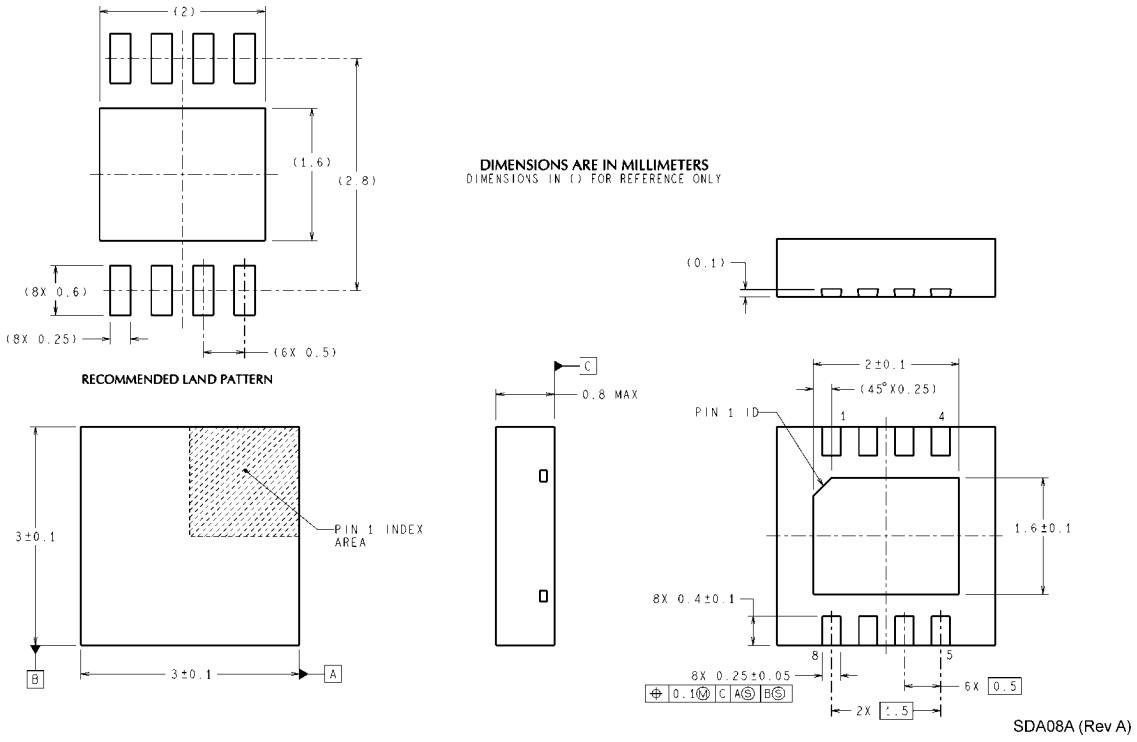
Total Jitter as a Function of Input Amplitude



30001733

Total Jitter as a Function of Input Amplitude

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS10BR150TSD
NS Package Number SDA08A
(See AN-1187 for PCB Design and Assembly Recommendations)

Notes

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560