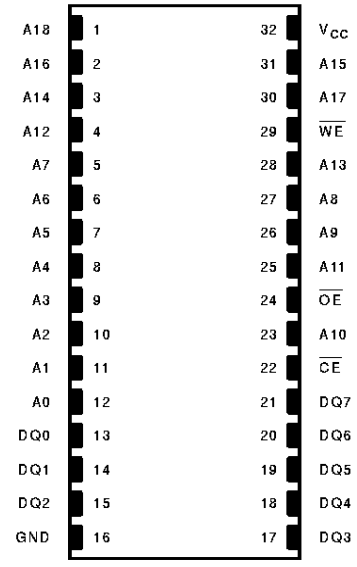
DALLAS SEMICONDUCTOR

DS1247Y
4096K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS operation
- Over 10 years of data retention
- Standard 32-pin JEDEC pinout
- Available in 85 or 100 ns read access times
- Read cycle time equals write cycle time
- Full ±10% operating range
- Optional industrial temperature range of -40°C to +85°C, designated IND

PIN ASSIGNMENT



PIN DESCRIPTION

A0 - A18	–	Address Inputs
$\overline{CE}$	–	Chip Enable
GND	–	Ground
DQ0 - DQ7	–	Data In/Data Out
V_{CC}	–	Power (+5V)
$\overline{WE}$	–	Write Enable
$\overline{OE}$	–	Output Enable

DESCRIPTION

The DS1247Y 4096K Nonvolatile SRAM is a 4,184,304-bit, fully static, nonvolatile SRAM organized as 524,288 words by 8 bits. The DS1247Y has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of existing 512K x 8 static RAM directly conforming to the popular bytewide 32-pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

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OPERATION - READ MODE

The DS1247Y executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) is active (low). The unique address specified by the 19 address inputs (A_0 - A_{18}) defines which of the 524,288 bytes of data is accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

OPERATION - WRITE MODE

The DS1247Y is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1247Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.37 volts nominal. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1247Y constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for Ind parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for Ind parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	–4.0		+4.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	–4.0		+4.0	µA	
Output Current @ 2.4V	I_{OH}	–1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $\overline{CE}$=2.2V	I_{CCS1}		5.0	10.0	mA	
Standby Current $\overline{CE}$=V_{CC}–0.5V	I_{CCS2}		3.0	5.0	mA	
Operating Current	I_{CCO1}			85	mA	
Write Protection Voltage)	V_{TP}	4.25	4.37	4.5	V	

CAPACITANCE

(t_A = 25°C)

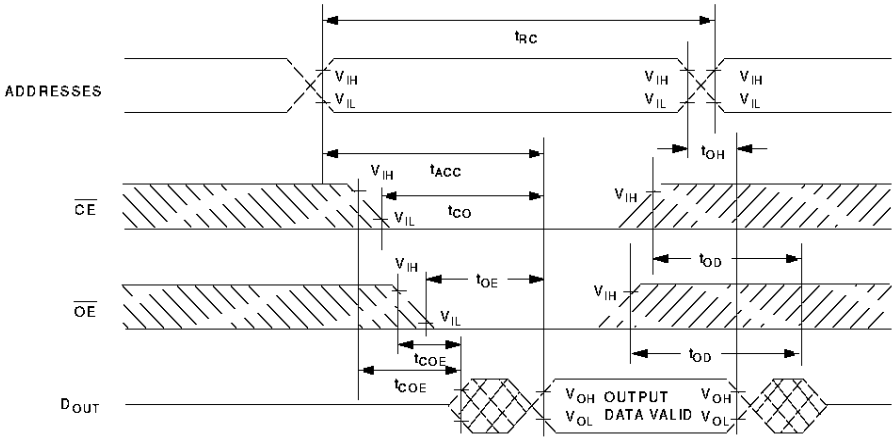
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		20	40	pF	
Input/Output Capacitance	$C_{I/O}$		20	40	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V ± 10%)

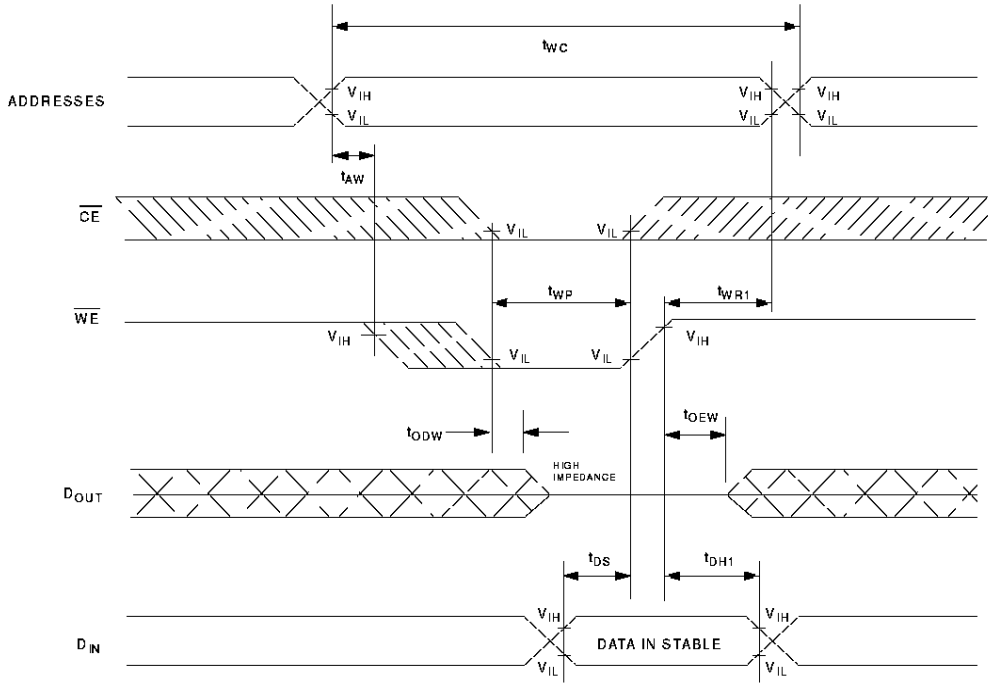
PARAMETER	SYMBOL	DS1247Y–85		DS1247Y–100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	85		100		ns	
Access Time	t_{ACC}		85		100	ns	
$\overline{OE}$ to Output Valid	t_{OE}		45		50	ns	
$\overline{CE}$ to Output Valid	t_{CO}		85		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		30		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	85		100		ns	
Write Pulse Width	t_{WP}	65		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15		5 15		ns ns	13 14
Output High Z from $\overline{WE}$	t_{ODW}		30		35	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	35		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10		0 10		ns ns	13 14

READ CYCLE



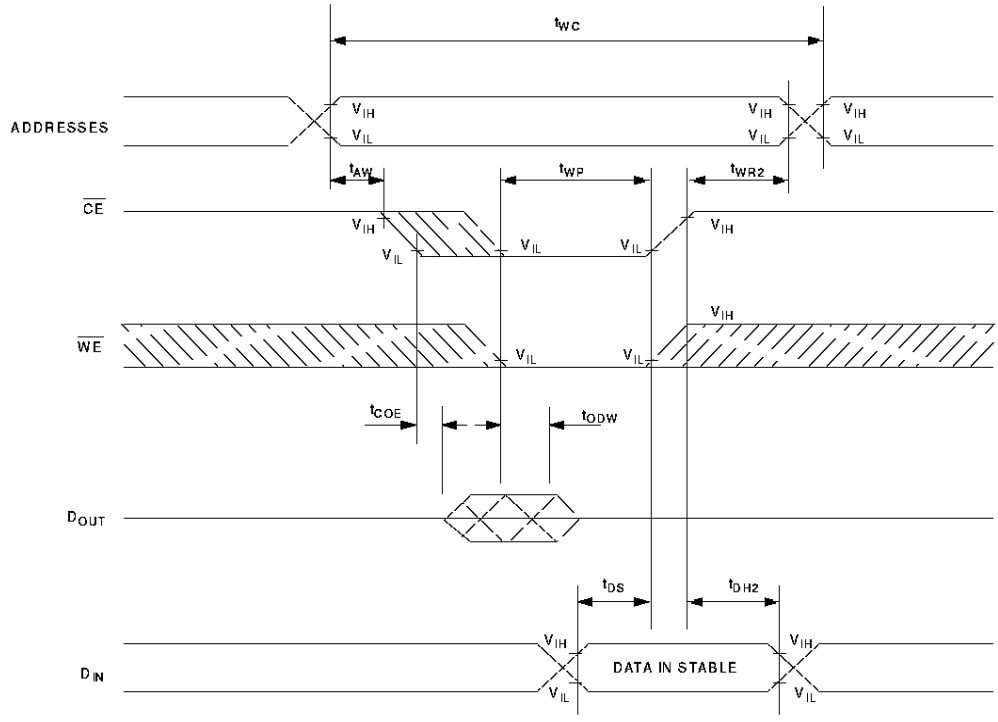
SEE NOTE 1

WRITE CYCLE 1



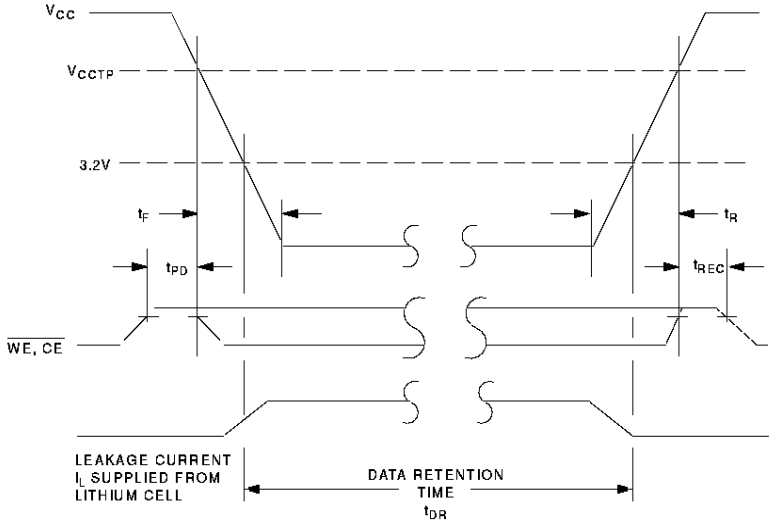
SEE NOTES 2, 3, 4, 6, 7, 8, and 13

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8, and 14

POWER-DOWN/POWER-UP CONDITION



SEE NOTE 12

POWER-DOWN/POWER-UP TIMING

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power–Down	0		µs	12
t_F	V_{CC} slew from 4.5V to 0V ($\overline{CE}$ at V_{IH})	300		µs	
t_R	V_{CC} slew from 0V to 4.5V ($\overline{CE}$ at V_{IH})	0		µs	
t_{REC}	$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power–Up	2	10	ms	

(t_A = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9, 11

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1247Y is marked with a 4–digit date code AABB, AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified t_{DR} at 25°C. IND parts which are continuously exposed to 85°C will have a t_{DR} of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a t_{DR} of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
13. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
14. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.

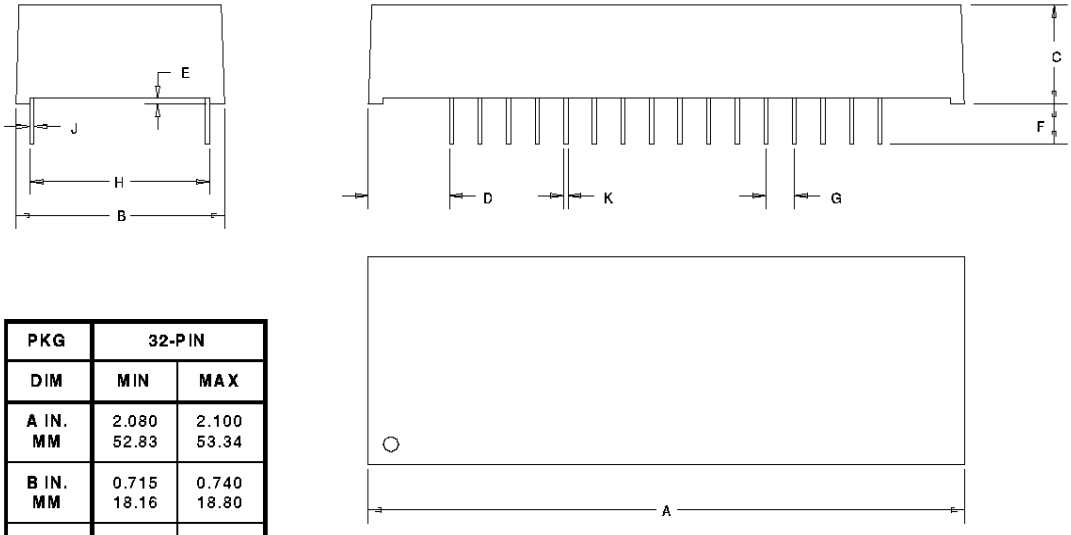
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns for operating current
All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 - 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input pulse Rise and Fall Times: 5 ns

DS1247Y NONVOLATILE SRAM



PKG	32-PIN	
DIM	MIN	MAX
A IN.	2.080	2.100
MM	52.83	53.34
B IN.	0.715	0.740
MM	18.16	18.80
C IN.	0.345	0.365
MM	8.76	9.27
D IN.	0.280	0.31.0
MM	7.11	7.49
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN	0.590	0.630
MM	14.99	16.00
J IN	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.025
MM	0.43	0.58