

# DALLAS

SEMICONDUCTOR

## DS1250YL/BL

### 4096K Nonvolatile SRAM

**NOT RECOMMENDED FOR NEW DESIGNS. SEE DS1250Y/AB DATA SHEET.**

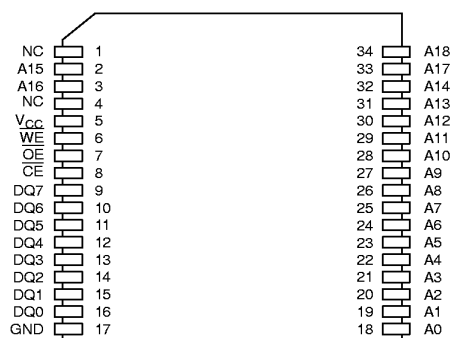
#### FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 70 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time.
- Full  $\pm 10\%$   $V_{CC}$  operating range (DS1250YL)
- Optional  $\pm 5\%$   $V_{CC}$  operating range (DS1250BL)
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , designated IND
- JEDEC standard 32-pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68-pin PLCC surface-mountable sockets
  - 250 mil package height

#### DESCRIPTION

The DS1250 4096K Nonvolatile SRAMs are 4,194,304-bit, fully static, nonvolatile SRAMs organized as 524,288 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the

#### PIN ASSIGNMENT



34-PIN LOW PROFILE MODULE (LPM)

#### PIN DESCRIPTION

A0 – A18	– Address Inputs
DQ0 – DQ7	– Data In/Data Out
$\overline{\text{CE}}$	– Chip Enable
$\overline{\text{WE}}$	– Write Enable
$\overline{\text{OE}}$	– Output Enable
$V_{CC}$	– Power (+5V)
GND	– Ground

lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interfacing.

### READ MODE

The DS1250 devices execute a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) and  $\overline{OE}$  (Output Enable) are active (low). The unique address specified by the 17 address inputs ( $A_0 - A_{16}$ ) defines which of the 131,072 bytes of data is accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

### WRITE MODE

The DS1250 devices execute a write cycle whenever the  $\overline{WE}$  and  $\overline{CE}$  signals are active (low) after address inputs are stable. The later occurring falling edge of  $\overline{CE}$  or  $\overline{WE}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{CE}$  or  $\overline{WE}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{WE}$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) before another cycle can be initiated. The  $\overline{OE}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ( $\overline{CE}$  and  $\overline{OE}$  active) then  $\overline{WE}$  will disable the outputs in  $t_{ODW}$  from its falling edge.

### DATA RETENTION MODE

The DS1250BL provides full functional capability for  $V_{CC}$  greater than 4.75 volts and write protects by 4.5 volts. The DS1250YL provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The nonvolatile static RAMs constantly monitor  $V_{CC}$ . Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.75 volts for the DS1250BL and 4.5 volts for the DS1250YL.

### FRESHNESS SEAL

Each DS1250 device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is first applied at a level greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground  
 Operating Temperature  
 Storage Temperature  
 Soldering Temperature

-0.3V to +7.0V  
 0°C to 70°C, -40°C to +85°C for Ind parts  
 -40°C to +70°C, -40°C to +85°C for Ind parts  
 260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**(t<sub>A</sub>: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1250BL Power Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.25	V	
DS1250YL Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub>	V	
Logic 0	V <sub>IL</sub>	0.0		+0.8	V	

**DC ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub>=5V ± 5% for DS1250BL)  
(t<sub>A</sub>: See Note 10) (V<sub>CC</sub>=5V ± 10% for DS1250YL)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0		+1.0	μA	
I/O Leakage Current C <sub>E</sub> ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0		+1.0	μA	
Output Current @ 2.4V	I <sub>OH</sub>	-1.0			mA	
Output Current @ 0.4V	I <sub>OL</sub>	2.0			mA	
Standby Current C <sub>E</sub> =2.2V	I <sub>CCS1</sub>		5.0	10.0	mA	
Standby Current C <sub>E</sub> =V <sub>CC</sub> -0.5V	I <sub>CCS2</sub>		3.0	5.0	mA	
Operating Current	I <sub>CCO1</sub>			85	mA	
Write Protection Voltage (DS1250BL)	V <sub>TP</sub>	4.50	4.62	4.75	V	
Write Protection Voltage (DS1250YL)	V <sub>TP</sub>	4.25	4.37	4.5	V	

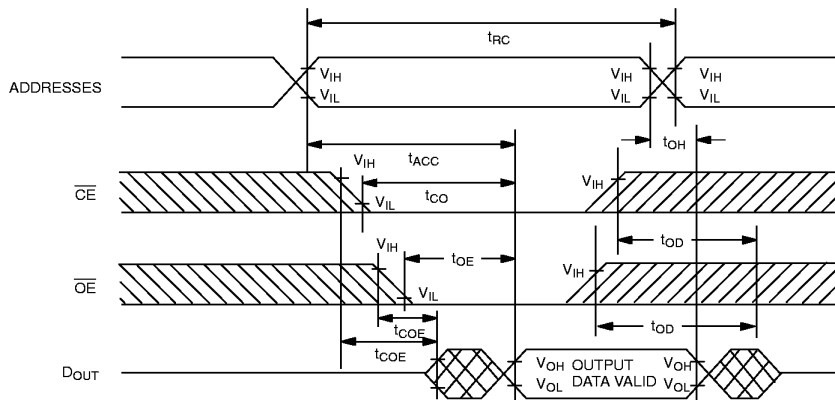
**CAPACITANCE**(t<sub>A</sub> = 25°C)

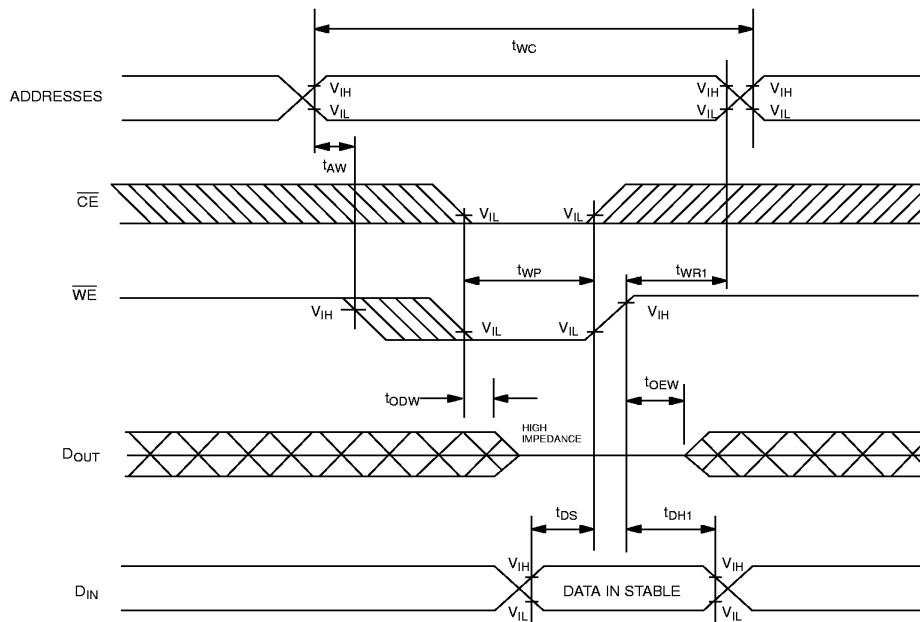
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Input/Output Capacitance	C <sub>I/O</sub>		5	10	pF	

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V \pm 5\%$  for DS1250BL)  
( $t_A$ : See Note 10) ( $V_{CC}=5V \pm 10\%$  for DS1250YL)

PARAMETER	SYMBOL	DS1250BL-70 DS1250YL-70		DS1250BL-100 DS1250YL-100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	$t_{RC}$	70		100		ns	
Access Time	$t_{ACC}$		70		100	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$		35		50	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$		70		100	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	$t_{COE}$	5		5		ns	5
Output High-Z from Deselection	$t_{OD}$		25		35	ns	5
Output Hold from Address Change	$t_{OH}$	5		5		ns	
Write Cycle Time	$t_{WC}$	70		100		ns	
Write Pulse Width	$t_{WP}$	55		75		ns	3
Address Setup Time	$t_{AW}$	0		0		ns	
Write Recovery Time	$t_{WR1}$ $t_{WR2}$	5 15		5 15		ns ns	12 13
Output High-Z from $\overline{WE}$	$t_{ODW}$		25		35	ns	5
Output Active from $\overline{WE}$	$t_{OEWE}$	5		5		ns	5
Data Setup Time	$t_{DS}$	30		40		ns	4
Data Hold Time	$t_{DH1}$ $t_{DH2}$	0 10		0 10		ns ns	12 13

**READ CYCLE**

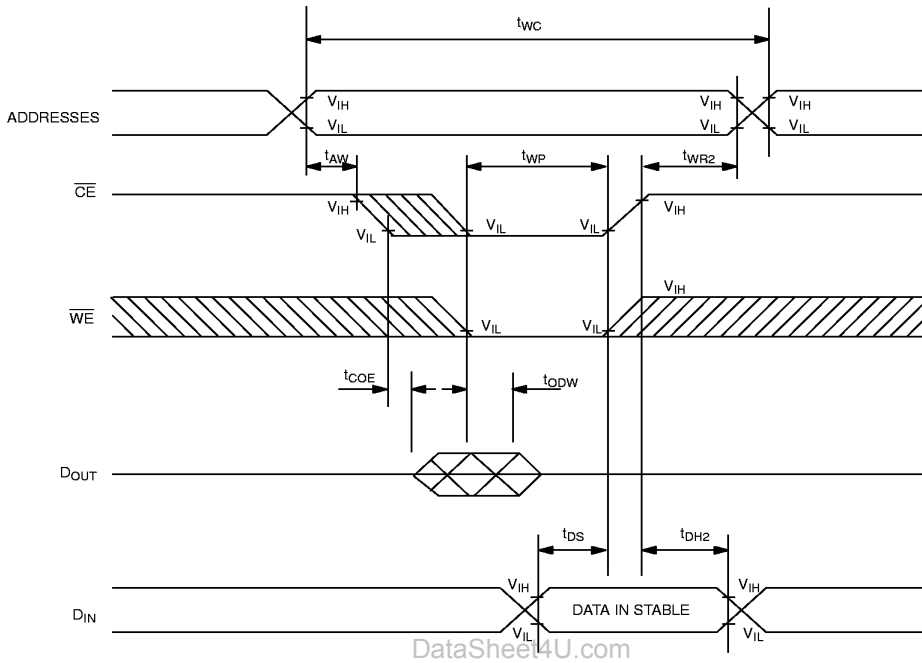


**WRITE CYCLE 1**

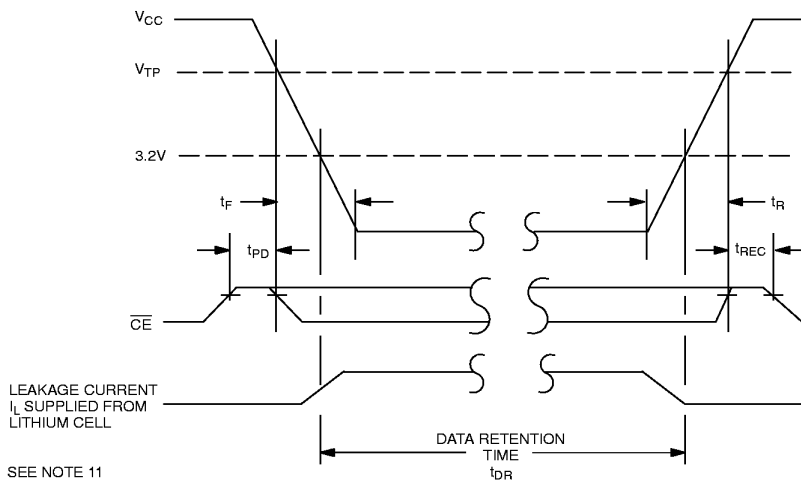
SEE NOTES 2, 3, 4, 6, 7, 8, AND 12

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**WRITE CYCLE 2**

SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

**POWER-DOWN/POWER-UP CONDITION**

SEE NOTE 11

**POWER-DOWN/POWER-UP TIMING**(t<sub>A</sub>: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ , $\overline{WE}$ at V <sub>IH</sub> before Power-Down	t <sub>PD</sub>	0			μs	11
V <sub>CC</sub> Slew from V <sub>TP</sub> to 0V	t <sub>F</sub>	300			μs	
V <sub>CC</sub> Slew from 0V to V <sub>TP</sub>	t <sub>R</sub>	300			μs	
$\overline{CE}$ , $\overline{WE}$ at V <sub>IH</sub> after Power-Up	t <sub>REC</sub>	2		125	ms	

(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t <sub>DR</sub>	10			years	9

**WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

- $\overline{WE}$  is high for a read cycle.
- $\overline{OE} = V_{IH}$  or V<sub>IL</sub>. If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
- t<sub>WP</sub> is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ . t<sub>WP</sub> is measured from the later of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- t<sub>DS</sub> is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the  $\overline{CE}$  low transition occurs simultaneously with or later than the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state during this period.
- If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in high impedance state during this period.
- If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high impedance state during this period.
- Each DS1250 has a built-in switch that disconnects the lithium source until V<sub>CC</sub> is first applied by the user. The expected t<sub>DR</sub> is defined as accumulative time in the absence of V<sub>CC</sub> starting from the time power is first applied by the user.
- All AC and DC electrical characteristics are valid over the full operating temperature range. For standard products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
- In a power down condition the voltage on any pin may not exceed the voltage on V<sub>CC</sub>.
- t<sub>WR1</sub>, t<sub>DH1</sub> are measured from  $\overline{WE}$  going high.
- t<sub>WR2</sub>, t<sub>DH2</sub> are measured from  $\overline{CE}$  going high.

DS1250YL/BL

**DC TEST CONDITIONS**

Outputs Open

Cycle = 200 ns for operating current

All voltages are referenced to ground

**AC TEST CONDITIONS**

Output Load: 100 pF + 1TTL Gate

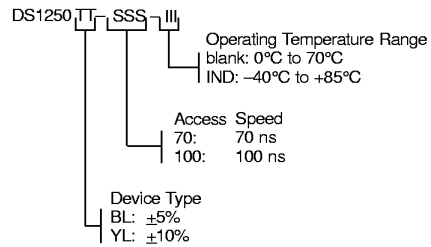
Input Pulse Levels: 0 – 3.0V

Timing Measurement Reference Levels

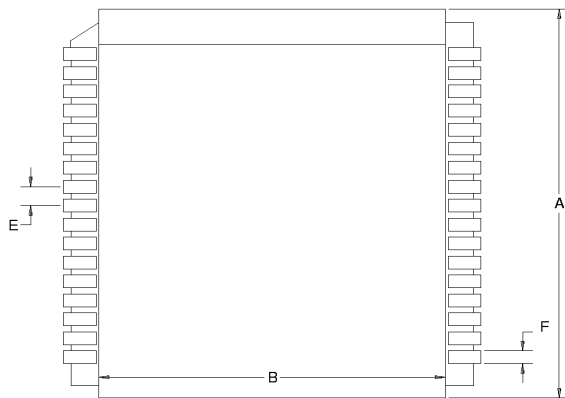
Input: 1.5V

Output: 1.5V

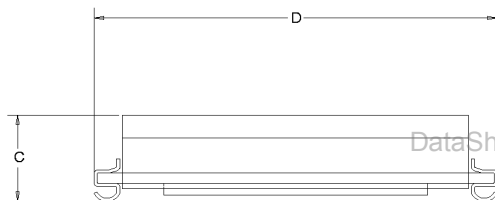
Input pulse Rise and Fall Times: 5 ns

**ORDERING INFORMATION**



**DS1250YL/BL 34-PIN LOW PROFILE MODULE (LPM)**

PKG	INCHES	
	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
D	0.047	0.053
F	0.015	0.025



Dallas Semiconductor Low Profile Modules **must** be inserted into 68-pin PLCC sockets for proper operation. Direct surface-mounting of these products by reflow soldering will destroy internal lithium batteries.

For recommended PLCC sockets, contact the Dallas Semiconductor factory.