



DS1350Y/AB

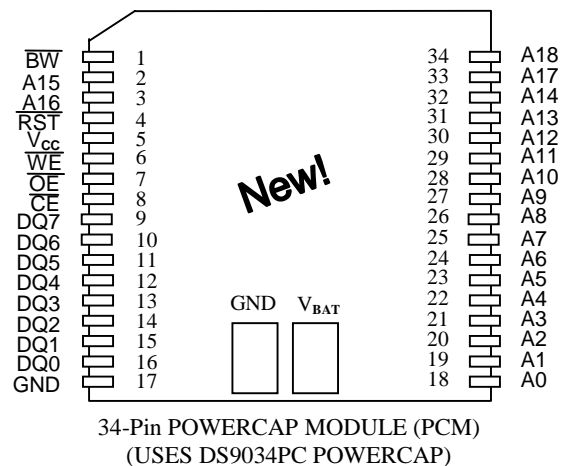
4096k Nonvolatile SRAM with Battery Monitor

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FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Power supply monitor resets processor when V_{CC} power loss occurs and holds processor in reset during V_{CC} ramp-up
- Battery monitor checks remaining capacity daily
- Read and write access times as fast as 70 ns
- Unlimited write cycle endurance
- Typical standby current 50 μ A
- Upgrade for 512k x 8 SRAM, EEPROM or Flash
- Lithium battery is electrically disconnected to retain freshness until power is applied for the first time
- Full $\pm 10\%$ V_{CC} operating range (DS1350Y) or optional $\pm 5\%$ V_{CC} operating range (DS1350AB)
- Optional industrial temperature range of -40°C to $+85^{\circ}\text{C}$, designated IND
- New PowerCap Module (PCM) package
 - Directly surface-mountable module
 - Replaceable snap-on PowerCap provides lithium backup battery
 - Standardized pinout for all nonvolatile SRAM products
 - Detachment feature on PowerCap allows easy removal using a regular screwdriver

PIN ASSIGNMENT



PIN DESCRIPTION

A0 - A18	- Address Inputs
DQ0 - DQ7	- Data In/Data Out
$\overline{\text{CE}}$	- Chip Enable
$\overline{\text{WE}}$	- Write Enable
$\overline{\text{OE}}$	- Output Enable
$\overline{\text{RST}}$	- Reset Output
$\overline{\text{BW}}$	- Battery Warning
V_{CC}	- Power (+5V)
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS1350 4096k Nonvolatile SRAMs are 4,194,304-bit, fully static, nonvolatile SRAMs organized as 524,288 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. Additionally, the DS1350 devices have dedicated circuitry for monitoring the status of V_{CC} and the status of the internal lithium battery. DS1350 devices in the PowerCap Module package are directly surface mountable and are normally paired with a DS9034PC PowerCap to form a complete Nonvolatile SRAM module. The devices can be used in place of 512k x 8 SRAM, EEPROM or Flash components.

READ MODE

The DS1350 devices execute a read cycle whenever \overline{WE} (Write Enable) is inactive (high) and \overline{CE} (Chip Enable) and \overline{OE} (Output Enable) are active (low). The unique address specified by the 19 address inputs (A_0 - A_{18}) defines which of the 524,288 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that \overline{CE} and \overline{OE} (Output Enable) access times are also satisfied. If \overline{OE} and \overline{CE} access times are not satisfied, then data access must be measured from the later-occurring signal (\overline{CE} or \overline{OE}) and the limiting parameter is either t_{CO} for \overline{CE} or t_{OE} for \overline{OE} rather than address access.

WRITE MODE

The DS1350 devices execute a write cycle whenever the \overline{WE} and \overline{CE} signals are in the active (low) state after address inputs are stable. The later-occurring falling edge of \overline{CE} or \overline{WE} will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of \overline{CE} or \overline{WE} . All address inputs must be kept valid throughout the write cycle. \overline{WE} must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The \overline{OE} control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled (\overline{CE} and \overline{OE} active) then \overline{WE} will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1350AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects by 4.5 volts. The DS1350Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC} . Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become “don’t care,” and all outputs become high-impedance. As V_{CC} falls below approximately 2.7 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.7 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts for the DS1350AB and 4.5 volts for the DS1350Y.

SYSTEM POWER MONITORING

DS1350 devices have the ability to monitor the external V_{CC} power supply. When an out-of-tolerance power supply condition is detected, the NV SRAMs warn a processor-based system of impending power failure by asserting \overline{RST} . On power-up, \overline{RST} is held active for 200 ms nominal to prevent system operation during power-on transients and to allow t_{REC} to elapse. \overline{RST} has an open drain output driver.

BATTERY MONITORING

The DS1350 devices automatically perform periodic battery voltage monitoring on a 24-hour time interval. Such monitoring begins within t_{REC} after V_{CC} rises above V_{TP} and is suspended when power failure occurs.

After each 24-hour period has elapsed, the battery is connected to an internal $1M\Omega$ test resistor for one second. During this one second, if battery voltage falls below the battery voltage trip point (2.6V), the battery warning output \overline{BW} is asserted. Once asserted, \overline{BW} remains active until the module is replaced. The battery is still retested after each V_{CC} power-up, however, even if \overline{BW} is active. If the battery voltage is found to be higher than 2.6V during such testing, \overline{BW} is de-asserted and regular 24-hour testing resumes. \overline{BW} has an open drain output driver.

FRESHNESS SEAL

Each DS1350 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{TP} , the lithium energy source is enabled for battery backup operation.

PACKAGES

The 34-pin PowerCap Module integrates SRAM memory and nonvolatile control along with contacts for connection to the lithium battery in the DS9034PC PowerCap. The PowerCap Module package design allows a DS1350 PCM device to be surface mounted without subjecting its lithium backup battery to destructive high-temperature reflow soldering. After a DS1350 PCM is reflow soldered, a DS9034PC is snapped on top of the PCM to form a complete Nonvolatile SRAM module. The DS9034PC is keyed to prevent improper attachment. DS1350 PowerCap Modules and DS9034PC PowerCaps are ordered separately and shipped in separate containers. See the DS9034PC data sheet for further information.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C, -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C, -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1350AB Power Supply Voltage	V _{CC}	4.75	5.0	5.25	V	
DS1350Y Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V	
Logic 1	V _{IH}	2.2		V _{CC}	V	
Logic 0	V _{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ± 5% for DS1350AB) (t_A: See Note 10) (V_{CC}=5V ± 10% for DS1350Y)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I _{IL}	-1.0		+1.0	μA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I _{IO}	-1.0		+1.0	μA	
Output Current @ 2.4V	I _{OH}	-1.0			mA	14
Output Current @ 0.4V	I _{OL}	2.0			mA	14
Standby Current $\overline{CE} = 2.2V$	I _{CCS1}		200	600	μA	
Standby Current $\overline{CE} = V_{CC} - 0.5V$	I _{CCS2}		50	150	μA	
Operating Current	I _{CCO1}			85	mA	
Write Protection Voltage (DS1350AB)	V _{TP}	4.50	4.62	4.75	V	
Write Protection Voltage (DS1350Y)	V _{TP}	4.25	4.37	4.5	V	

CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C _{IN}		5	10	pF	
Input/Output Capacitance	C _{I/O}		5	10	pF	

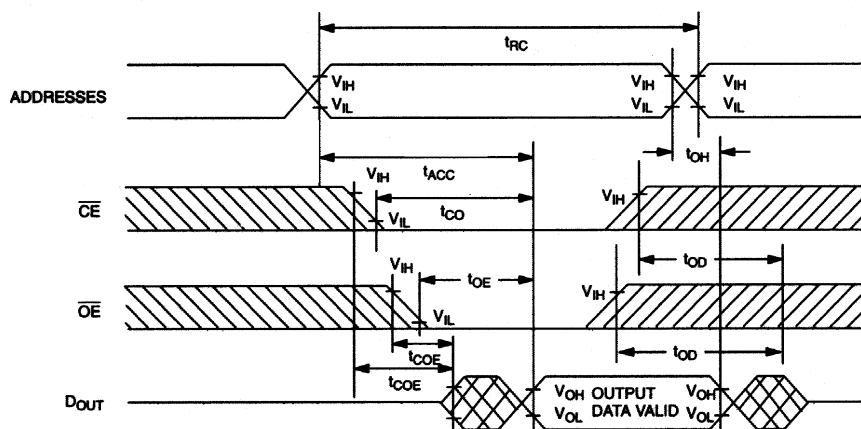
AC ELECTRICAL CHARACTERISTICS

($V_{CC}=5V \pm 5%$ for DS1350AB)

(t_A : See Note 10) ($V_{CC}=5V \pm 10%$ for DS1350Y)

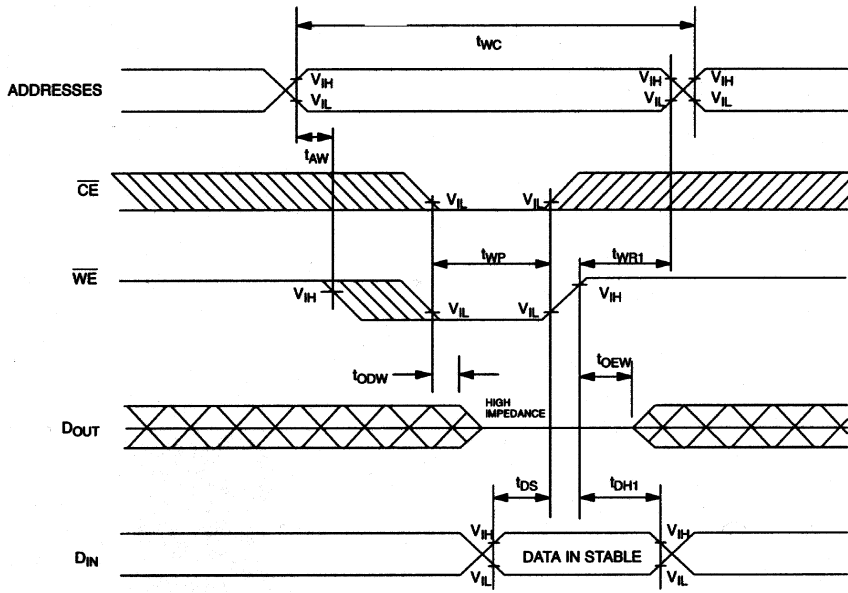
PARAMETER	SYMBOL	DS1350AB-70 DS1350Y-70		DS1350AB-100 DS1330Y-100		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		100		ns	
Access Time	t_{ACC}		70		100	ns	
\overline{OE} to Output Valid	t_{OE}		35		50	ns	
\overline{CE} to Output Valid	t_{CO}		70		100	ns	
\overline{OE} or \overline{CE} to Output Active	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	70		100		ns	
Write Pulse Width	t_{WP}	55		75		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 12		5 12		ns	12 13
Output High Z from \overline{WE}	t_{ODW}		25		35	ns	5
Output Active from \overline{WE}	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	30		40		ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 7		0 7		ns	12 13

READ CYCLE



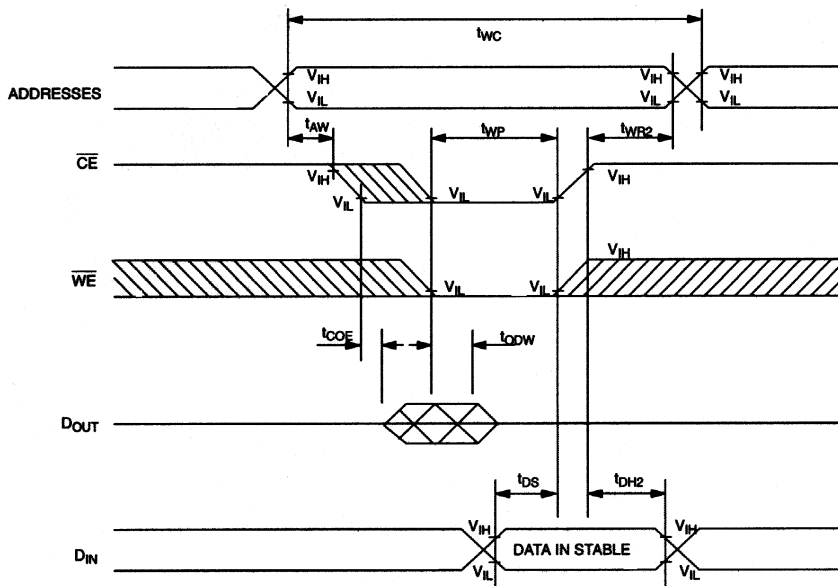
SEE NOTE 1

WRITE CYCLE 1



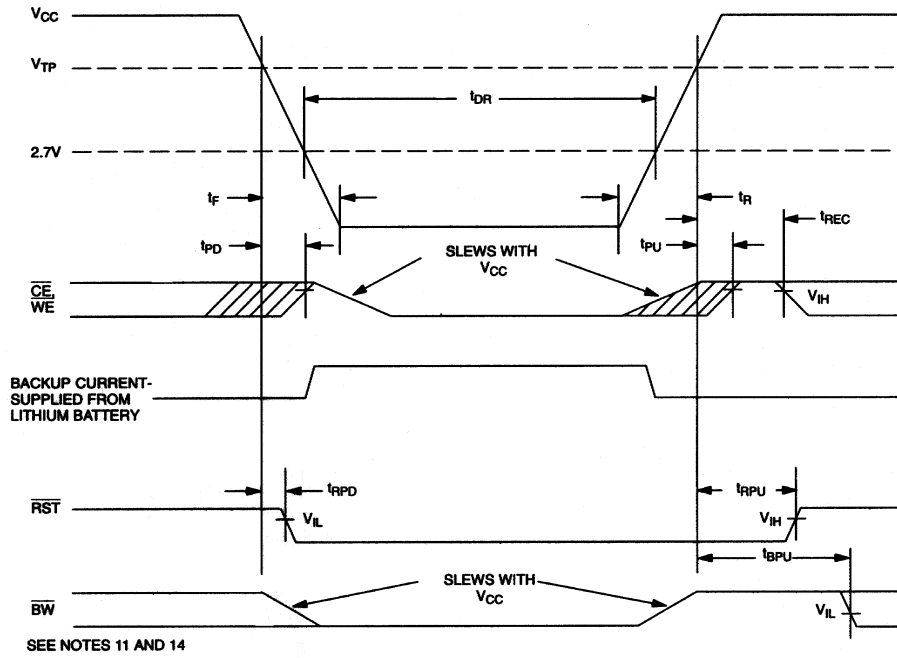
SEE NOTES 2, 3, 4, 6, 7, 8, and 12

WRITE CYCLE 2

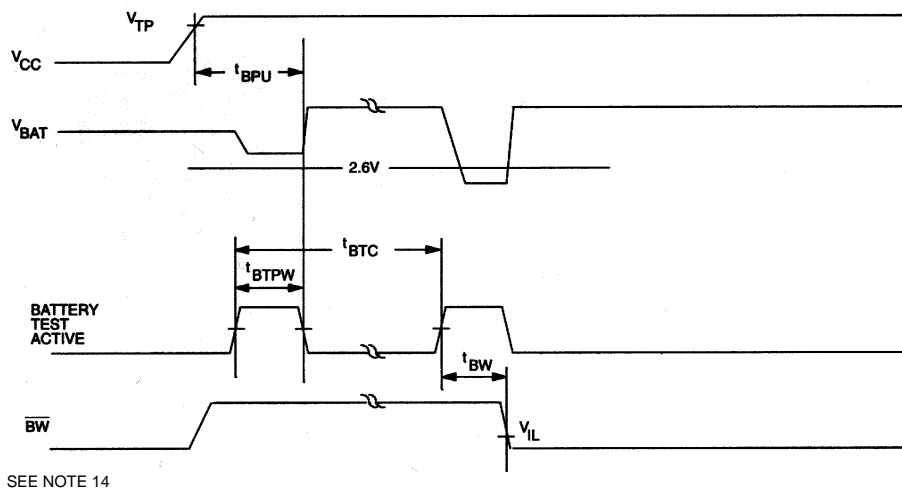


SEE NOTES 2, 3, 4, 6, 7, 8, and 13

POWER-DOWN/POWER-UP CONDITION



BATTERY WARNING DETECTION



POWER-DOWN/POWER-UP TIMING(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{CC} Fail Detect to $\overline{\text{CE}}$ and $\overline{\text{WE}}$ Inactive	t _{PD}			1.5	μs	11
V _{CC} slew from V _{TP} to 0V	t _F	150			μs	
V _{CC} Fail Detect to $\overline{\text{RST}}$ Active	t _{RPD}			15	μs	14
V _{CC} slew from 0V to V _{TP}	t _R	150			μs	
V _{CC} Valid to $\overline{\text{CE}}$ and $\overline{\text{WE}}$ Inactive	t _{PU}			2	ms	
V _{CC} Valid to End of Write Protection	t _{REC}			125	ms	
V _{CC} Valid to $\overline{\text{RST}}$ Inactive	t _{RPU}	150	200	350	ms	14
V _{CC} Valid to $\overline{\text{BW}}$ Valid	t _{BPU}			1	s	14

BATTERY WARNING TIMING(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Battery Test Cycle	t _{BTC}		24		hr	
Battery Test Pulse Width	t _{BTPW}			1	s	
Battery Test to $\overline{\text{BW}}$ Active	t _{BW}			1	s	

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t _{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

- $\overline{\text{WE}}$ is high for a Read Cycle.
- $\overline{\text{OE}} = V_{\text{IH}}$ or V_{IL} . If $\overline{\text{OE}} = V_{\text{IH}}$ during write cycle, the output buffers remain in a high-impedance state.
- t_{WP} is specified as the logical AND of $\overline{\text{CE}}$ and $\overline{\text{WE}}$. t_{WP} is measured from the latter of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going low to the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.
- t_{DS} are measured from the earlier of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the $\overline{\text{CE}}$ low transition occurs simultaneously with or latter than the $\overline{\text{WE}}$ low transition, the output buffers remain in a high-impedance state during this period.
- If the $\overline{\text{CE}}$ high transition occurs prior to or simultaneously with the $\overline{\text{WE}}$ high transition, the output buffers remain in high-impedance state during this period.
- If $\overline{\text{WE}}$ is low or the $\overline{\text{WE}}$ low transition occurs prior to or simultaneously with the $\overline{\text{CE}}$ low transition, the output buffers remain in a high-impedance state during this period.

9. Each DS1230Y has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C . For industrial products (IND), this range is -40°C to $+85^{\circ}\text{C}$.
11. In a power-down condition the voltage on any pin may not exceed the voltage on V_{CC} .
12. t_{WR1} and t_{DH1} are measured from \overline{WE} going high.
13. t_{WR2} and t_{DH2} are measured from \overline{CE} going high.
14. \overline{RST} and \overline{BW} are open drain outputs and cannot source current. External pullup resistors should be connected to these pins for proper operation. Both pins will sink 10 mA.

DC TEST CONDITIONS

Outputs Open

Cycle = 200 ns for operating current

All voltages are referenced to ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate

Input Pulse Levels: 0 - 3.0V

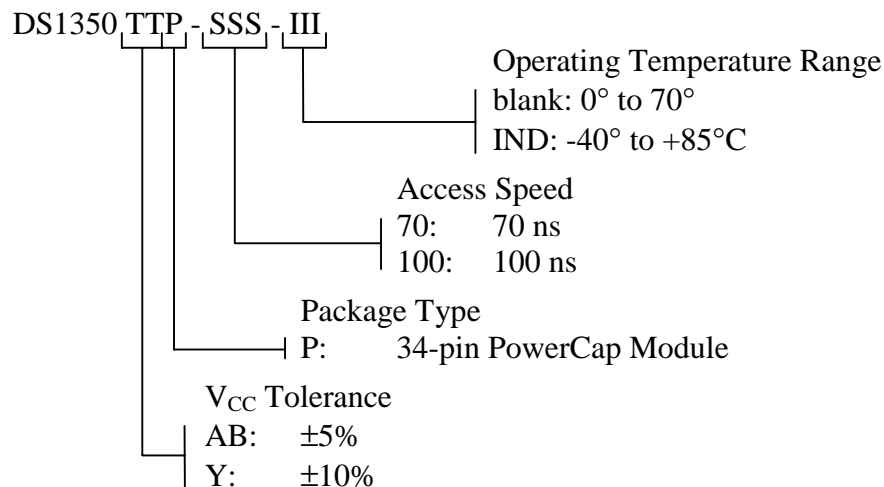
Timing Measurement Reference Levels

Input: 1.5V

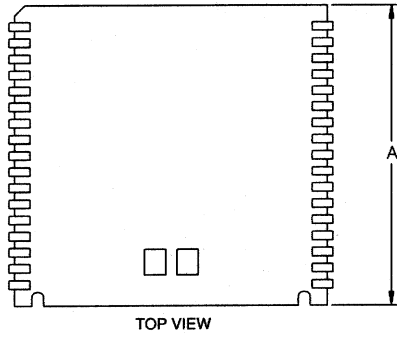
Output: 1.5V

Input pulse Rise and Fall Times: 5 ns

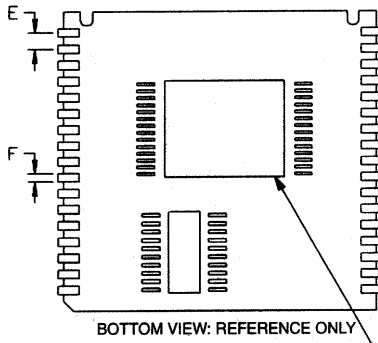
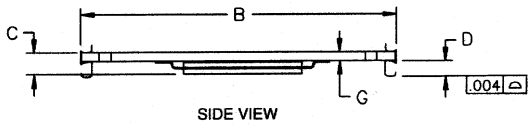
ORDERING INFORMATION



DS1350Y/AB NONVOLATILE SRAM, 34-PIN POWERCAP MODULE

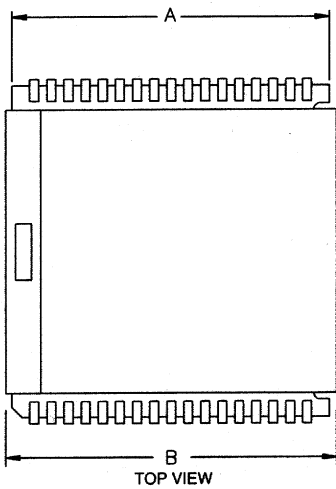


PKG DIM	INCHES		
	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.980	0.985	0.990
C	-	-	0.080
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.020	0.025	0.030

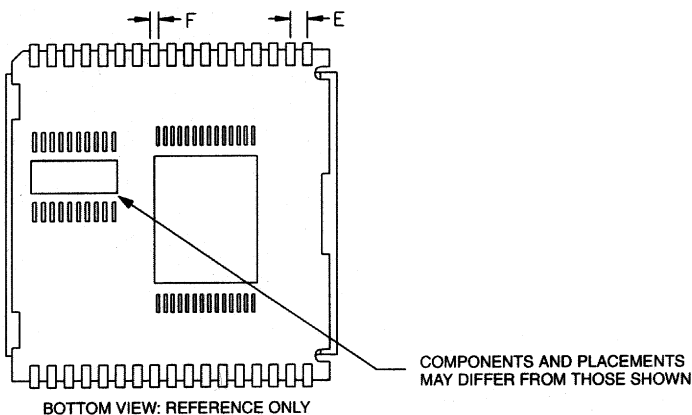
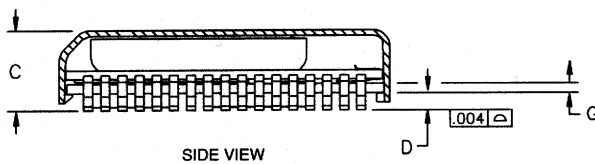


COMPONENTS AND PLACEMENTS
MAY DIFFER FROM THOSE SHOWN

DS1350Y/AB NONVOLATILE SRAM, 34-PIN POWERCAP MODULE WITH POWERCAP



PKG DIM	INCHES		
	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.955	0.960	0.965
C	0.240	0.245	0.250
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.020	0.025	0.030



ASSEMBLY AND USE

Reflow soldering

Dallas Semiconductor recommends that PowerCap Module bases experience one pass through solder reflow oriented label-side up (live-bug).

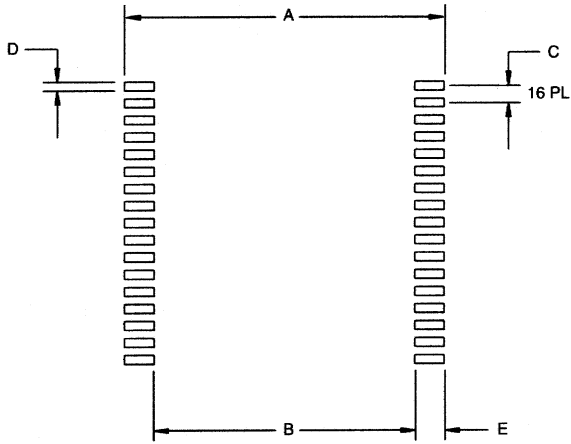
Hand soldering and touch-up

Do not touch soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove part, apply flux, heat pad until solder reflows, and use a solder wick.

LPM replacement in a socket

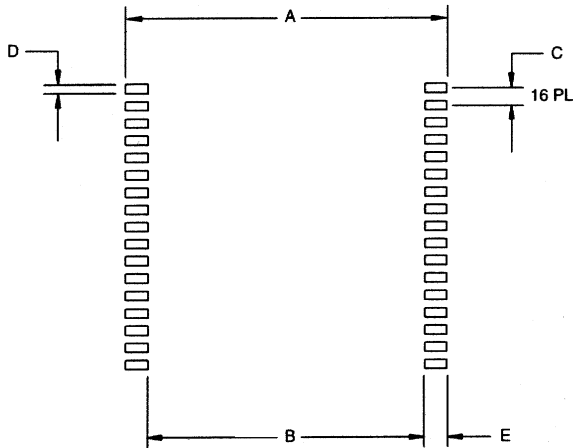
To replace a Low Profile Module in a 68-pin PLCC socket, attach a DS9034PC PowerCap to a module base then insert the complete module into the socket one row of leads at a time, pushing only on the corners of the cap. Never apply force to the center of the device. To remove from a socket, use a PLCC extraction tool and ensure that it does not hit or damage any of the module IC components. Do not use any other tool for extraction.

RECOMMENDED POWERCAP MODULE LAND PATTERN



PKG DIM	INCHES		
	MIN	NOM	MAX
A	-	1.050	-
B	-	0.826	-
C	-	0.050	-
D	-	0.030	-
E	-	0.112	-

RECOMMENDED POWERCAP MODULE SOLDER STENCIL



PKG DIM	INCHES		
	MIN	NOM	MAX
A	-	1.050	-
B	-	0.890	-
C	-	0.050	-
D	-	0.030	-
E	-	0.080	-