PRELIMINARY

DALLAS
SEMICONDUCTOR

DS1672
Low Voltage Serial Timekeeping Chip

FEATURES

- 32-bit counter
- 2-wire serial interface
- Automatic power-fail detect and switch circuitry
- Power-fail reset output
- Low-voltage oscillator operation (1.3V min.)
- Trickle charge capability
-

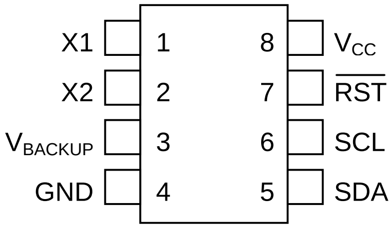
ORDERING INFORMATION

DS1672X-X

2	2.0V operation
3	3.0V operation
33	3.3V operation

blank	8-pin DIP
S	8-pin SOIC
U	8-pin µSOP

PIN ASSIGNMENT



PIN DESCRIPTION

V_{CC}, V_{BACKUP}	- Power Supply Inputs
GND	- Ground
X1, X2	- 32.768 kHz crystal pins
SCL	- Serial clock
SDA	- Serial data
$\overline{\text{RST}}$	- Reset output

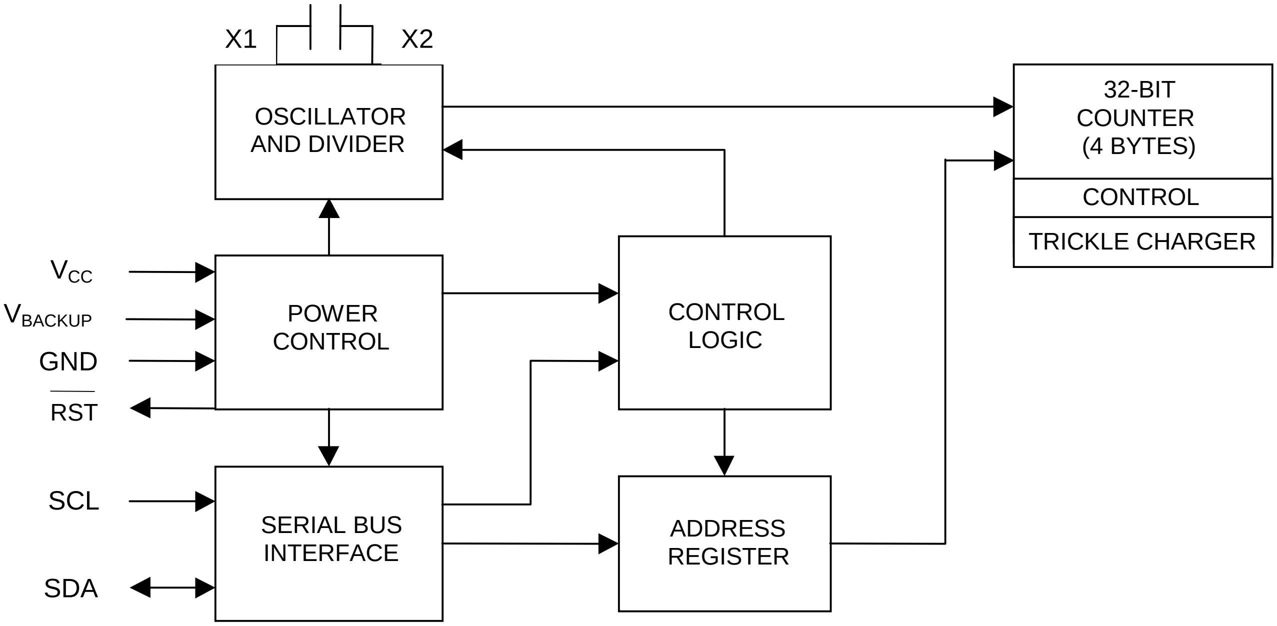
DESCRIPTION

The DS1672 incorporates a 32-bit counter and power monitoring functions. The 32-bit counter is designed to count seconds and can be used to derive time of day, week, month, month, and year by using a software algorithm. A precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated which forces the reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signal is kept in the active state for 250 ms to allow the power supply and processor to stabilize.

OPERATION

The block diagram in Figure 1 shows the main elements of the DS1672. As shown, communications to and from the DS1672 occur serially over a 2-wire bi-directional bus. The DS1672 operates as a slave device on the serial bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed.

DS1672 BLOCK DIAGRAM Figure 1



ADDRESS MAP

The counter is accessed by reading or writing the first 4 bytes of the DS1672 (00h - 03h). The control register and trickle charger are accessed by reading or writing the appropriate register bytes as illustrated in Figure 2. If the master continues to send or request more data after the address pointer has reached 05h, the address pointer will wrap around to location 00h.

DS1672 REGISTERS Figure 2

Address	B7	B6	B5	B4	B3	B2	B1	B0	Function
00h									Counter Byte 1
01h									Counter Byte 2
02h									Counter Byte 3
03h									Counter Byte 4
04h	$\overline{\text{EOSC}}$								Control
05h	TCS	TCS	TCS	TCS	DS	DS	RS	RS	Trickle Charger

DATA RETENTION MODE

The device is fully accessible and data can be written and ready only when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, (point at which write protection occurs) the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. The registers are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels.

OSCILLATOR CONTROL

The $\overline{\text{EOSC}}$ bit (bit 7 of the control register) controls the oscillator when in back-up mode. This bit when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1672 is placed into a low-power standby mode with a current drain of less than 200 nanoamps when in back-up mode. When the DS1672 is powered by $V_{CC,}$ the oscillator is always on regardless of the status of the $\overline{\text{EOSC}}$ bit; however, the counter is incremented only when $\overline{\text{EOSC}}$ is a logic 0.

CRYSTAL SELECTION

A standard 32.768 kHz quartz crystal should be directly connected to the X1 and X2 oscillator pins. The crystal selected for use should have a specified load capacitance (C_L) of 6 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Dallas Real Time Clocks."

MICROPROCESSOR MONITOR

A temperature-compensated comparator circuit monitors the level of V_{CC}. When V_{CC} falls to the power-fail trip point, the $\overline{\text{RST}}$ signal (open drain) is pulled active. When V_{CC} returns to nominal levels, the $\overline{\text{RST}}$ signal is kept in the active state for 250 ms (typically) to allow the power supply and microprocessor to stabilize. Note, however, that if the $\overline{\text{EOSC}}$ bit is set to a logic 1 (to disable the oscillator during write protection), the reset signal will be kept in an active state for 250 ms plus the start-up time of the oscillator.

TRICKLE CHARGER

The trickle charger is controlled by the trickle charge register. The simplified schematic of Figure 3 shows the basic components of the trickle charger. The trickle charge select (TCS) bit (bits 4-7) controls the selection of the trickle charger. In order to prevent accidental enabling, only a pattern on 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1672 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2-3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. If DS is 01, no diode is selected or if DS is 10, a diode is selected. The RS bits (bits 0-1) select whether a resistor is connected between V_{CC} and V_{BACKUP} and what the value of the resistor is. The resistor selected by the resistor select (RS) bits and the diode selected by the diode select (DS) bits are as follows:

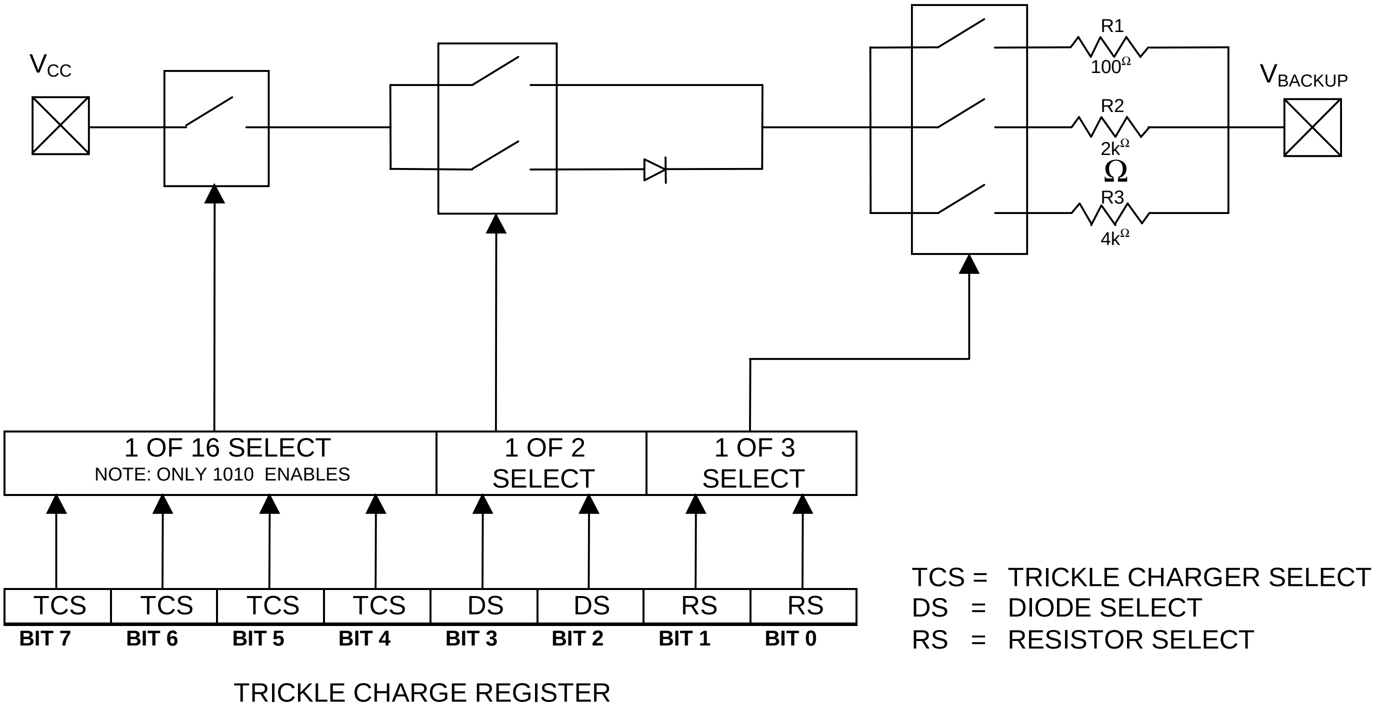
TCS	TCS	TCS	TCS	DS	DS	RS	RS	Function
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 100Ω resistor
1	0	1	0	1	0	0	1	One diode, 100Ω resistor
1	0	1	0	0	1	1	0	No diode, 2 kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2 kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4 kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4 kΩ resistor

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 3 volt is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{max} would therefore be calculated as follows:

$$
\begin{aligned}
I_{max} &= (3.0V - \text{diode drop}) / R2 \\
&\sim (3.0V - 0.7V) / 2\ k\Omega \\
&\sim 1.2\ mA
\end{aligned}
$$

Obviously, as the super cap changes, the voltage drop between V_{CC} and V_{BACKUP} will decrease and therefore the charge current will decrease.

DS1672 PROGRAMMABLE TRICKLE CHARGER Figure 3



2-WIRE SERIAL DATA BUS

The DS1672 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a “master." The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The DS1672 operates as a slave on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined (see Figure 4).
Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line from high to low, while the clock line is high, defines a START condition.

Stop data transfer: A change in the state of the data line from low to high, while the clock line is high, defines a STOP condition.

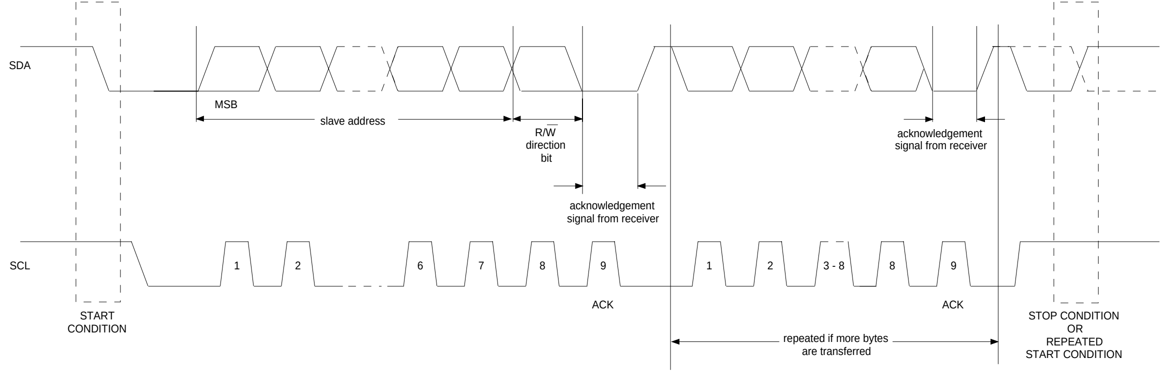
Data valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and the STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

DATA TRANSFER ON 2-WIRE SERIAL BUS Figure 4



Figures 5 and 6 detail how data transfer is accomplished on the 2-wire bus. Depending upon the state of the $R/\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.

2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows a number of data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a ‘not acknowledge’ is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

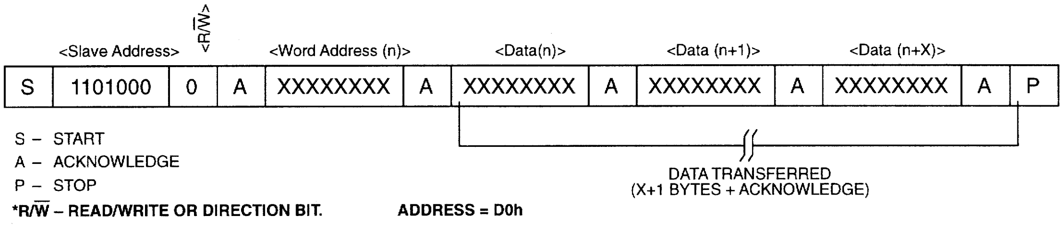
The DS1672 may operate in the following two modes:

1. **Slave receiver mode (DS1672 write mode):** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The address byte is the first byte received after the START condition is generated by the master. The address byte contains the 7-bit DS1672 address, which is 1101000, followed by the direction bit ($R/\overline{W}$), which for a write is a 0. After receiving and decoding the address byte the DS1672 outputs an acknowledge on the SDA line. After the DS1672 acknowledges the slave address + write bit, the master transmits a register address to the DS1672. This will set the register pointer on the DS1672. The master will then begin transmitting each byte of data with the DS1672 acknowledging each byte received. The master will generate a STOP condition to terminate the data write.

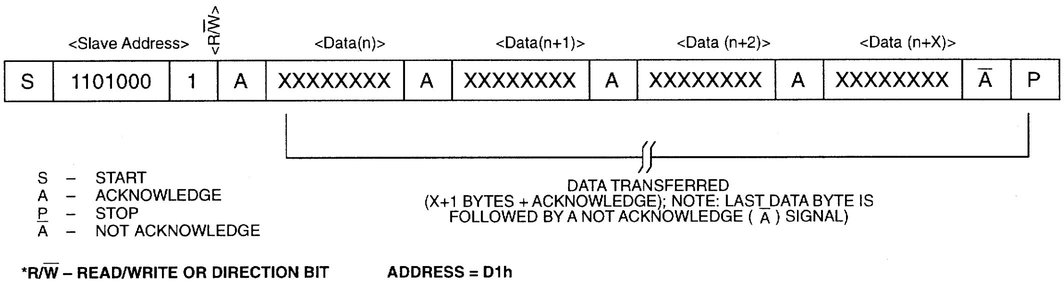
2. **Slave transmitter mode (DS1672 read mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the DS1672 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit. The address byte is the first byte received after the START condition is generated by the master. The address byte contains the 7-bit DS1672 address, which is 1101000, followed by the direction bit

($R/\overline{W}$), which for a read is a 1. After receiving and decoding the address byte the DS1672 inputs an Acknowledge on the SDA line. The DS1672 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The DS1672 must receive a not acknowledge to end a read.

DATA WRITE – SLAVE RECEIVER MODE Figure 5



DATA READ – SLAVE TRANSMITTER MODE Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to +6.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (DS1672-33)	V_{CC}	2.97	3.3	3.63	V	1
(DS1672-3)	V_{CC}	2.7	3.0	3.3	V	1
(DS1672-2)	V_{CC}	1.8	2.0	2.2	V	1
Logic 1	V_{IH}	$0.7V_{CC}$		$V_{CC} + 0.5$	V	1
Logic 0	V_{IL}	-0.5		$0.3V_{CC}$	V	1
Backup Supply Voltage	V_{BACKUP}	1.3		3.6	V	1

DC ELECTRICAL CHARACTERISTICS

DS1672-33 (-40°C to +85°C; V_{CC} = 2.97 to 3.63V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CCA}			2	mA	7
Standby Current	I_{CCS}			500	µA	8
Power-Fail Voltage	V_{PF}	2.80	2.88	2.97	V	1

DC ELECTRICAL CHARACTERISTICS

DS1672-3 (-40°C to +85°C; V_{CC} = 2.7 to 3.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CCA}			2	mA	7
Standby Current	I_{CCS}			500	µA	9
Power-Fail Voltage	V_{PF}	2.5	2.6	2.7	V	1

DC ELECTRICAL CHARACTERISTICS

DS1672-2 (-40°C to +85°C; V_{CC} = 1.8 to 2.2V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CCA}			2	mA	7
Standby Current	I_{CCS}			500	µA	10
Power-Fail Voltage	V_{PF}	1.6	1.7	1.8	V	1

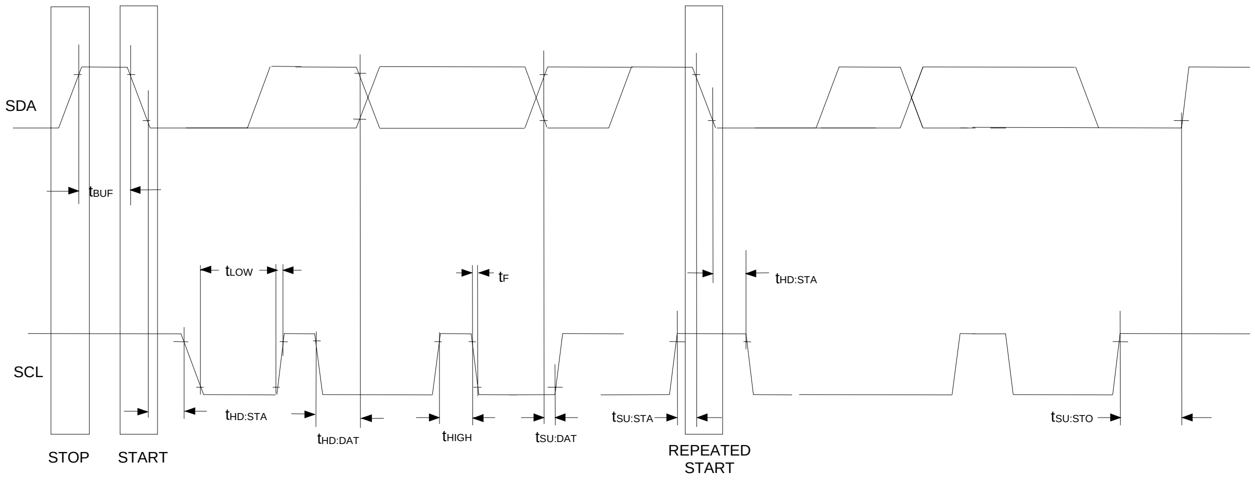
DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; $V_{CC} < V_{PF}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Timekeeping Current	I_{OSC}			1	µA	12
Backup Standby Current (Oscillator Off)	I_{BACKUP}			200	nA	13

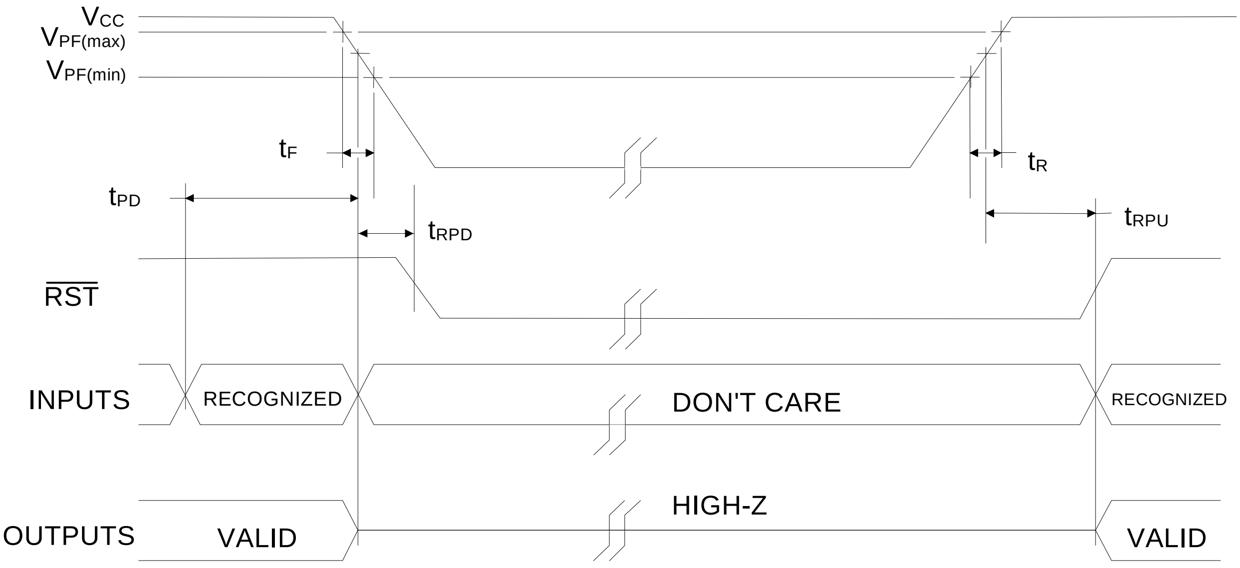
AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; $V_{CC} > V_{PF}$)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
SCL Clock Frequency	f_{SCL}	Fast Mode	100		400	kHz	
		Standard Mode			100		
Bus Free Time Between a STOP and START Condition	t_{BUF}	Fast Mode	1.3			µs	
		Standard Mode	4.7				
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Fast Mode	0.6			µs	2
		Standard Mode	4.0				
LOW Period of SCL Clock	t_{LOW}	Fast Mode	1.3			µs	
		Standard Mode	4.7				
HIGH Period of SCL Clock	t_{HIGH}	Fast Mode	0.6			µs	
		Standard Mode	4.0				
Set-up Time for a Repeated START Condition	$t_{SU:STA}$	Fast Mode	0.6			µs	
		Standard Mode	4.7				
Data Hold Time	$t_{HD:DAT}$	Fast Mode	0		0.9	µs	3, 4
		Standard Mode	0				
Data Set-up Time	$t_{SU:DAT}$	Fast Mode	100			µs	11
		Standard Mode	250				
Rise Time of Both SDA and SCL Signals	t_R	Fast Mode	$20 + 0.1C_B$		300	ns	5
		Standard Mode			1000		
Fall Time of Both SDA and SCL Signals	t_F	Fast Mode	$20 + 0.1C_B$		300	ns	5
		Standard Mode			300		
Set-up Time for STOP Condition	$t_{SU:STO}$	Fast Mode	0.6			µs	
		Standard Mode	4.0				
Capacitive Load for each Bus Line	C_B				400	pF	5
I/O Capacitance	$C_{I/O}$			10		pF	

Timing Diagram Figure 7



POWER-UP/DOWN TIMING Figure 8



POWER-UP DOWN CHARACTERISTICS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			10	µs	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising)	t_{RPU}		250		ms	6
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in write protection.

NOTES:

1. All voltages are referenced to ground.

2. After this period, the first clock pulse is generated.

3. A device must internally provide a hold time of at least 300 ns for the SDA signal (referenced to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

4. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

5. C_B - total capacitance of one bus line in pF.

6. If the $\overline{EOSC}$ bit in the Control Register is set to logic 1, t_{RPU} is equal to 250 ms plus the start-up time of the crystal oscillator.

7. I_{CCA} specified with SCL clocking at max frequency (400 kHz).

8. I_{CCS} specified with V_{CC} = 3.3V and SDA, SCL=3.3V.

9. I_{CCS} specified with V_{CC} = 3.0V and SDA, SCL=3.0V.

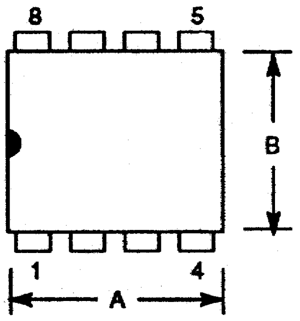
10. I_{CCS} specified with V_{CC} = 2.0V and SDA, SCL=2.0V.

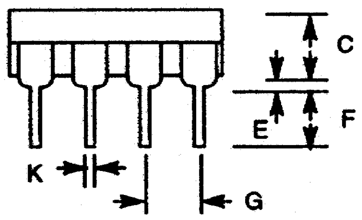
11. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ >= to 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_R max + $t_{SU:DAT}$ = 1000+250 = 1250 ns before the SCL line is released.

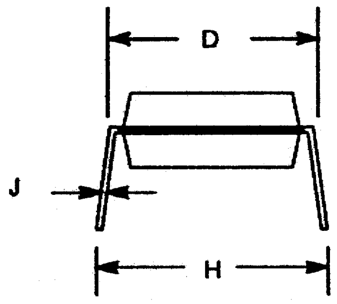
12. I_{OSC} specified with V_{CC} = 0V, V_{BACKUP} =3.6V and oscillator enabled.

13. I_{BACKUP} specified with V_{CC} = 0V, V_{BACKUP} =3.6V and oscillator disabled.

8-PIN DIP

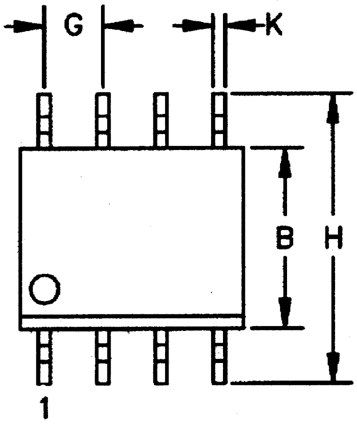


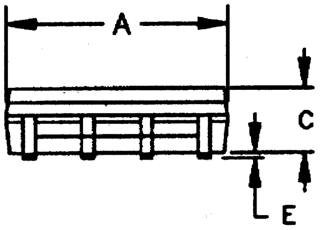


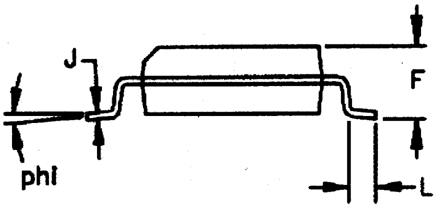


PKG	8-PIN	
DIM	**MIN**	**MAX**
A IN. **MM**	0.360 9.14	0.400 10.16
B IN. **MM**	0.240 6.10	0.260 6.60
C IN. **MM**	0.120 3.05	0.140 3.56
D IN. **MM**	0.300 7.62	0.325 8.26
E IN. **MM**	0.015 0.38	0.040 1.02
F IN. **MM**	0.120 3.04	0.140 3.56
G IN. **MM**	0.090 2.29	0.110 2.79
H IN. **MM**	0.320 8.13	0.370 9.40
J IN. **MM**	0.008 0.20	0.012 0.30
K IN. **MM**	0.015 0.38	0.021 0.53

8-PIN SOIC (150-MIL)







PKG	**8-PIN (150-MIL)**	
DIM	**MIN**	**MAX**
A IN. **MM**	0.188 4.78	0.196 4.98
B IN. **MM**	0.150 3.81	0.158 4.01
C IN. **MM**	0.048 1.22	0.062 1.57
E IN. **MM**	0.004 0.10	0.010 0.25
F IN. **MM**	0.053 1.35	0.069 1.75
G IN. **MM**	0.050 BSC 1.27 BSC	
H IN. **MM**	0.230 5.84	0.244 6.20
J IN. **MM**	0.007 0.18	0.011 0.28
K IN. **MM**	0.012 0.30	0.020 0.51
L IN. **MM**	0.016 0.41	0.050 1.27
phi	0°	8°