19-4986; Rev 1; 11/09

EVALUATION KIT AVAILABLE

SFP+ Controller with Analog LDD Interface

DS1873

General Description

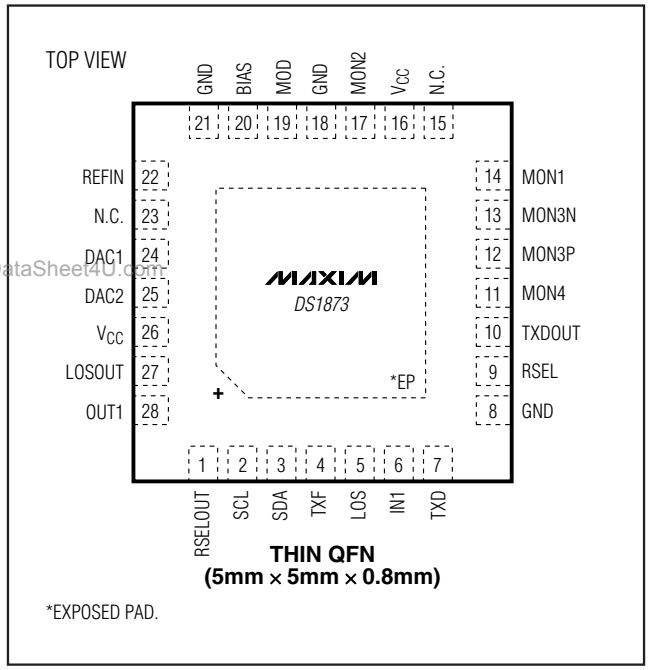
The DS1873 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality. The DS1873 provides APC loop, modulation current control, and eye safety functionality. The DS1873 continuously monitors for high output current, high bias current, and low and high transmit power to ensure that laser shutdown for eye safety requirements are met without adding external components.

Six ADC channels monitor V_{CC}, temperature, and four external monitor inputs (MON1–MON4) that can be used to meet all monitoring requirements. MON3 is differential with support for common mode to V_{CC}. Two digital-to-analog (DAC) outputs with temperature-indexed lookup tables (LUTs) are available for additional monitoring and control functionality.

Applications

SFF, SFP, and SFP+ Transceiver Modules

Pin Configuration



THIN QFN
(5mm × 5mm × 0.8mm)

*EXPOSED PAD.

Features

- **Meets All SFF-8472 Control and Monitoring Requirements**
- **Six Analog Monitor Channels: Temperature, V_{CC}, MON1–MON4**
  - **MON1–MON4 Support Internal and External Calibration**
  - **Scalable Dynamic Range**
  - **Internal Direct-to-Digital Temperature Sensor**
  - **Alarm and Warning Flags for All Monitored Channels**
- **Four 10-Bit Delta-Sigma Outputs with 36 Entry Temperature LUTs**
  - **Laser Bias Controlled by APC Loop and Temperature LUT to Compensate for Tracking Error**
  - **Laser Modulation Controlled by 72-Entry Temperature LUT**
  - **Two Additional DACs Controlled by One 72-Entry and One 36-Entry Temperature LUT**
- **Digital I/O Pins: Five Inputs, Five Outputs**
- **Comprehensive Fault-Measurement System with Maskable Laser Shutdown Capability**
- **Flexible, Two-Level Password Scheme Provides Three Levels of Security**
- **120 Bytes of Password-1 Protected Memory**
- **128 Bytes of Password-2 Protected Memory in Main Device Address**
- **256 Additional Bytes Located at A0h Slave Address**
- **I^2C-Compatible Interface**
- **+2.85V to +3.9V Operating Voltage Range**
- **-40°C to +95°C Operating Temperature Range**
- **28-Pin TQFN (5mm x 5mm) Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1873T+	-40°C to +95°C	28 TQFN-EP*
DS1873T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

SFP+ Controller with Analog LDD Interface

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on MON1–MON4, RSEL, IN1, LOS, TXF, and TXD Pins Relative to Ground .....-0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, OUT1, RSELOUT, and LOSOUT Pins Relative to Ground.....-0.5V to +4.2V

Operating Temperature Range .....-40°C to +95°C
Programming Temperature Range .....0°C to +95°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

**Subject to not exceeding +4.2V.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL)	$V_{IH:1}$		0.7 x V_{CC}		V_{CC} + 0.3	V
Low-Level Input Voltage (SDA, SCL)	$V_{IL:1}$		-0.3		0.3 x V_{CC}	V
High-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IH:2}$		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage (TXD, TXF, RSEL, IN1, LOS)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		2.5	10	mA
Output Leakage (SDA, OUT1, RSELOUT, LOSOUT, TXF)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, MOD, BIAS, OUT1, RSELOUT, LOSOUT, TXDOUT, DAC1, DAC2, TXF)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (MOD, BIAS, DAC1, DAC2, TXDOUT)	V_{OH}	I_{OH} = 4mA	V_{CC} - 0.4			V
TXDOUT Before EEPROM Recall		See Figure 14		10	100	nA
MOD, BIAS, DAC1, and DAC2 Before LUT Recall		See Figure 12		10	100	nA
Input Leakage Current (SCL, TXD, LOS, RSEL, IN1)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.75	V

MOD, BIAS, DAC1, DAC2 ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Oscillator Frequency	f_{OSC}			5		MHz
Delta-Sigma Input-Clock Frequency	f_{DS}			$f_{OSC}/2$		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution					10	Bits
Output Impedance	R_{DS}			35	100	Ω

ANALOG QUICK TRIP CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MON2, TXP HI, TXP LO Full-Scale Voltage	V_{APC}			2.5		V
HBIAS LOS Full-Scale Voltage				1.25		V
MON2 Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2.5		+2.5	%FS
LOS Offset				-5		mV

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution					13		Bits
Input/Supply Accuracy (MON1–MON4, V_{CC})		ACC	At factory setting		0.25	0.50	%FS
Update Rate for Temperature, MON1–MON4, and V_{CC}		t_{RR}			64	75	ms
Input/Supply Offset (MON1–MON4, V_{CC})		V_{OS}	(Note 3)		0	5	LSB
Factory Setting	MON1–MON4		(Note 4)		2.5		V
	V_{CC}				6.5536		
	MON3 Fine				312.5		µV

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-3		+3	°C

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXD Enable	t_{OFF}	From ↑ TXD to BIAS DAC and MOD DAC disable			5	µs
Recovery from TXD Disable (Figure 14)	t_{ON}	From ↓ TXD to BIAS DAC and MOD DAC enable			5	µs
Recovery After Power-Up	t_{INIT_DAC}	From ↑ V_{CC} > VCC LO alarm (Note 5)		20		ms
Fault Reset Time (to TXF = 0)	t_{INITR1}	From ↓ TXD		131		ms
	t_{INITR2}	From ↑ V_{CC} > VCC LO alarm (Note 5)		161		
Fault Assert Time (to TXF = 1)	t_{FAULT}	After HTXP, LTXP, HBATH, IBIASMAX (Note 6)			15	µs
LOSOUT Assert Time	t_{LOSS_ON}	LLOS (Notes 6, 7)			15	µs
LOSOUT Deassert Time	t_{LOSS_OFF}	HLOS (Notes 6, 8)			15	µs

TIMING CHARACTERISTICS (CONTROL LOOP AND QUICK TRIP)

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Enable Time Following POA	t_{INIT}	(Note 5)		20		ms
Binary Search Time	t_{SEARCH}	(Note 9)	8		10	BIAS Samples

I²C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$, unless otherwise noted.) (See Figure 16.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 10)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus-Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data Out Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 11)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 11)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
EEPROM Write Time	t_W	(Note 12)			20	ms
Capacitive Load for Each Bus Line	C_B				400	pF

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +25°C	200,000			
		At +85°C	50,000			

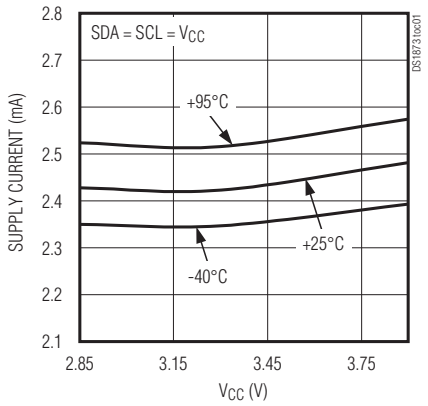
Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.
Note 2: Inputs are at supply rail. Outputs are not loaded.
Note 3: This parameter is guaranteed by design.

Note 4: Full-scale is user programmable.
Note 5: A temperature conversion is completed and the MOD DAC value is recalled from the LUT and V_{CC} has been measured to be above VCC LO alarm.
Note 6: The sampling time is 1.6µs per cycle. Each input is sampled every 8 cycles.
Note 7: This specification is the time it takes from MON3 voltage falling below the LLOS trip threshold to LOSOUT asserted high.
Note 8: This specification is the time it takes from MON3 voltage rising above the HLOS trip threshold to LOSOUT asserted low.
Note 9: Assuming an appropriate initial step is programmed that would cause the power to exceed the APC set point within four steps, the bias output will be within 3% within the time specified by the binary search time. See the *BIAS and MOD Output Control During Power-Up* section.
Note 10: I²C interface timing shown is for fast mode (400kHz). This device is also backward compatible with I²C standard mode timing.
Note 11: C_B—the total capacitance of one bus line in pF.
Note 12: EEPROM write begins after a STOP condition occurs.

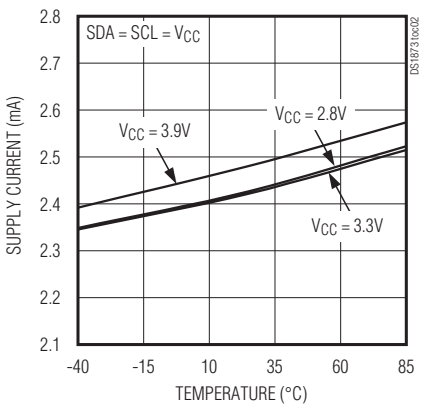
Typical Operating Characteristics

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

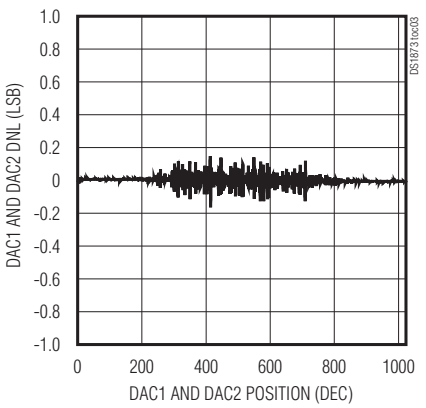
SUPPLY CURRENT vs. SUPPLY VOLTAGE



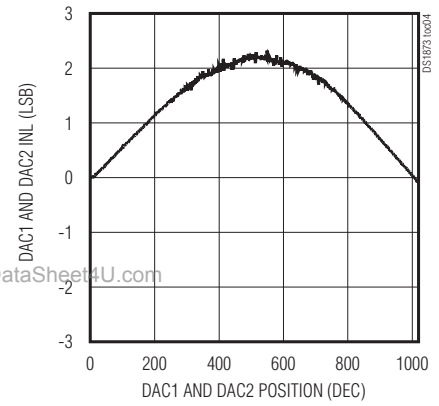
SUPPLY CURRENT vs. TEMPERATURE



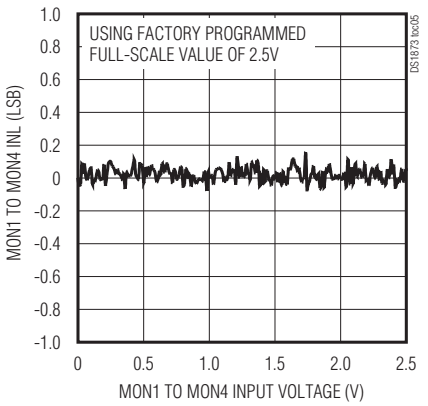
DAC1 AND DAC2 DNL



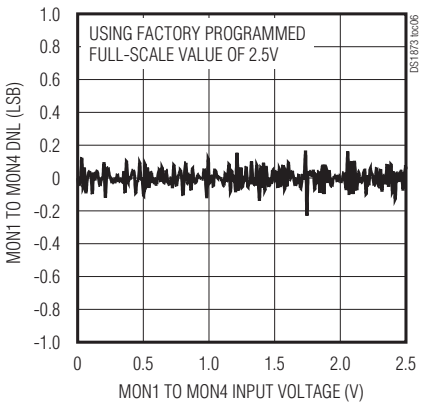
DAC1 AND DAC2 INL



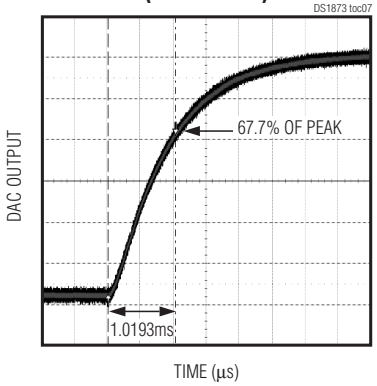
MON1 TO MON4 INL



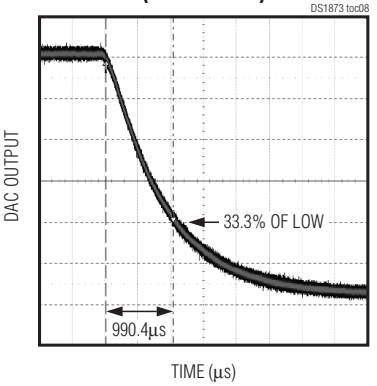
MON1 TO MON4 DNL



DAC SETTLING TIME (40% TO 60%)



DAC SETTLING TIME (60% TO 40%)

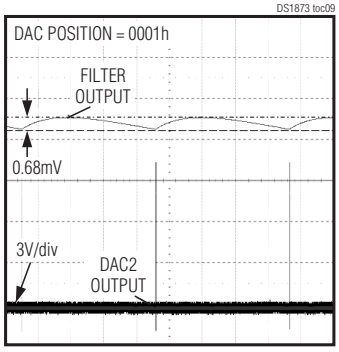


SFP+ Controller with Analog LDD Interface

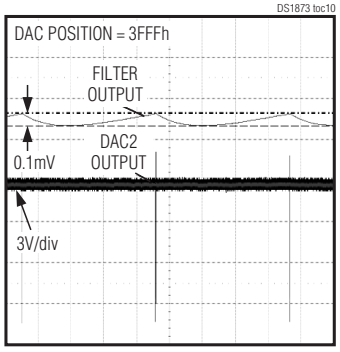
Typical Operating Characteristics (continued)

(V_{CC} = +2.85V to +3.9V, T_A = +25°C, unless otherwise noted.)

DAC OUTPUT RIPPLE AT 0001h



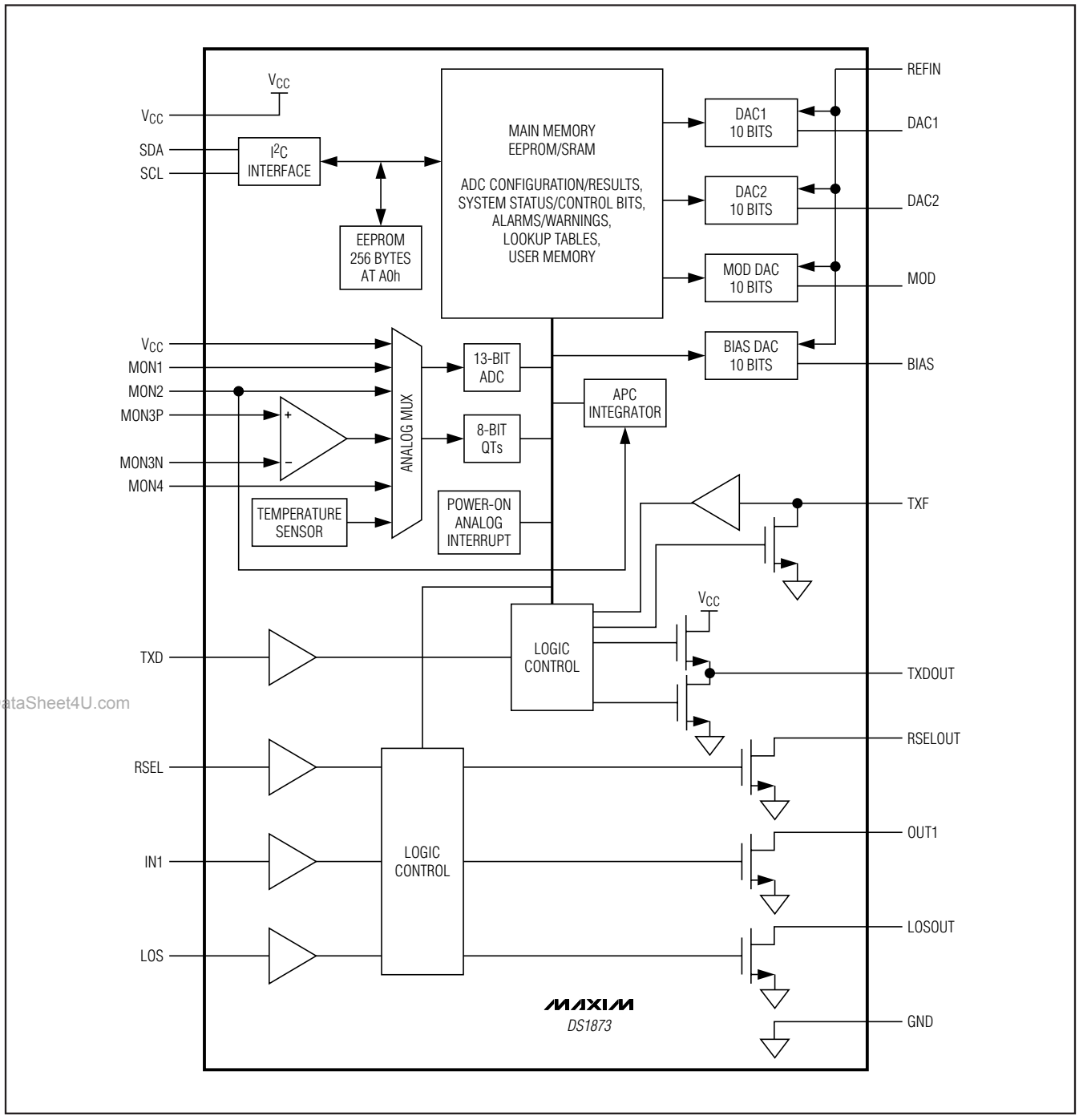
DAC OUTPUT RIPPLE AT 3FFFh



Pin Description

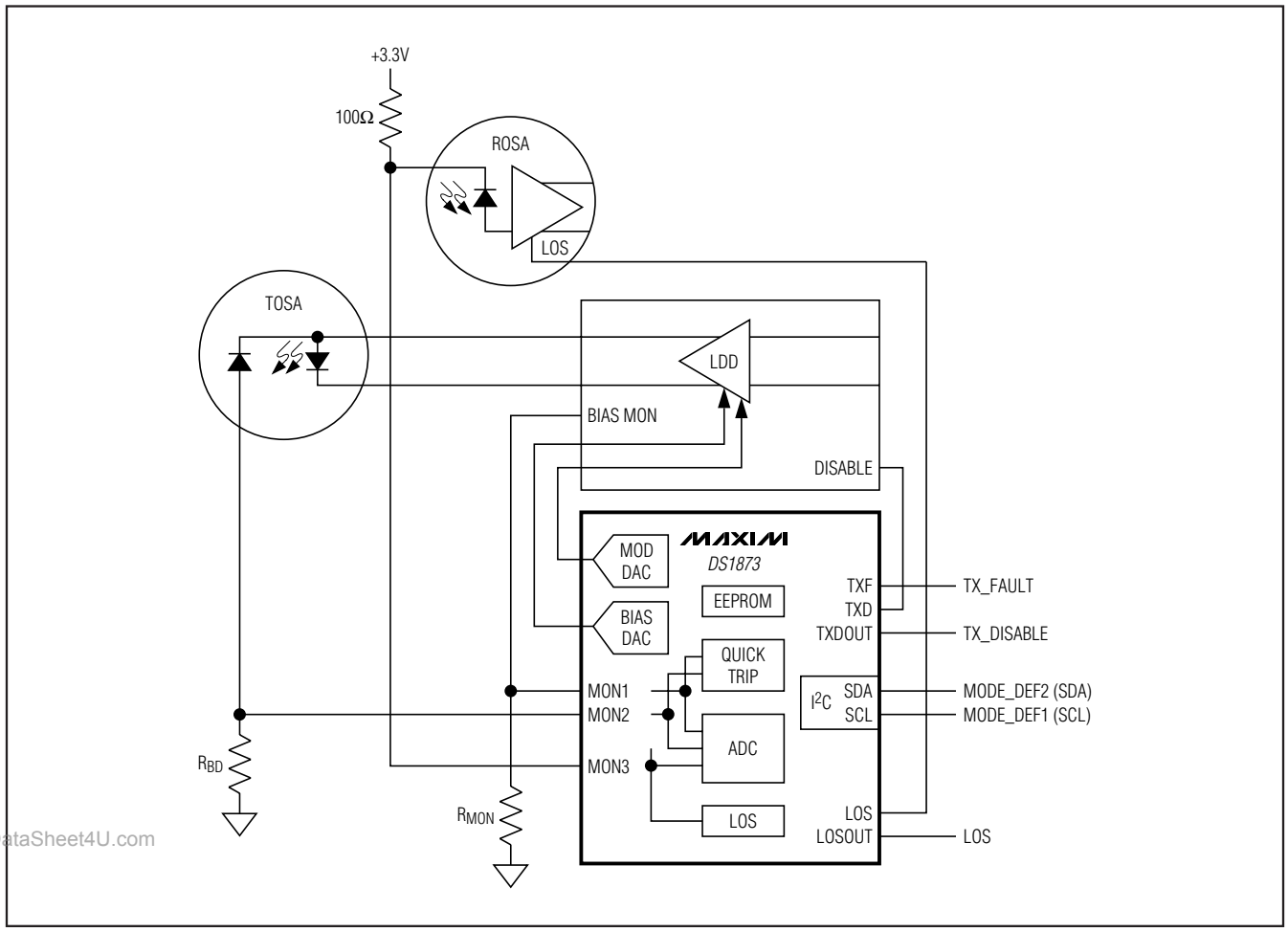
PIN	NAME	FUNCTION
1	RSELOUT	Open-Drain Rate-Select Output
2	SCL	I²C Serial-Clock Input
3	SDA	I²C Serial-Data Input/Output
4	TXF	Transmit-Fault Input and Output. The output is open drain.
5	LOS	Loss-of-Signal Input
6	IN1	Digital Input. General-purpose input with AS1 in SFF-8079 or RS1 in SFF-8431.
7	TXD	Transmit-Disable Input
8, 18, 21	GND	Ground Connection
9	RSEL	Rate-Select Input
10	TXDOUT	Transmit-Disable Output
11	MON4	External Monitor Input 4
12, 13	MON3P, MON3N	Differential External Monitor Input 3 and LOS LO Quick Trip
14	MON1	External Monitor Input 1 and HBATH Quick Trip
15, 23	N.C.	No Connection
16, 26	V_{CC}	Power-Supply Input
17	MON2	External Monitor Input 2. Feedback voltage for APC loop and HTXP/LTXP quick trip.
19	MOD	MOD DAC, Delta-Sigma Output
20	BIAS	BIAS DAC, Delta-Sigma Output
22	REFIN	Reference Input for DAC1 and DAC2
24, 25	DAC1, DAC2	Delta-Sigma Output 1/2
27	LOSOUT	Open-Drain Receive Loss-of-Signal Output
28	OUT1	Open-Drain Digital Output. General-purpose output with AS1 output in SFF-8079 or RS1 output in SFF-8431.
—	EP	Exposed Pad (Connect to GND)

Block Diagram



SFP+ Controller with Analog LDD Interface

Typical Operating Circuit



Detailed Description

The DS1873 integrates the control and monitoring functionality required to implement an SFP or SFP+ system. Key components of the DS1873 are shown in the *Block Diagram* and described in subsequent sections.

BIAS DAC/APC Control

The DS1873 controls its laser bias current using its BIAS DAC and the APC loop. The APC loop's feedback to the DS1873 is the monitor diode (MON2) current, which is converted to a voltage using an external resistor. The feedback is sampled by a comparator and compared to a digital set-point value. The output of the comparator has three states: up, down, or no-operation. The no-operation state prevents the output from excessive toggling once steady state is reached. As long as the comparator output is in either the up or down states, the bias is adjusted by incrementing and decrementing the BIAS DAC setting.

The DS1873 has an LUT to allow the APC set point to change as a function of temperature to compensate for tracking error (TE). The TE LUT has 36 entries that determine the APC setting in 4°C windows between -40°C to +100°C.

Table 1. Acronyms

ACRONYM	DEFINITION
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
ATB	Alarm Trap Bytes
BM	Burst Mode
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	Lookup Table
NV	Nonvolatile
QT	Quick Trip
TE	Tracking Error
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP
TOSA	Transmit Optical Subassembly
TXP	Transmit Power

BIAS and MOD Output Control During Power-Up

On power-up, the DS1873 sets the MOD and BIAS DACs to 0. After a temperature conversion is completed and if the VCC LO alarm is enabled, an additional V_{CC} conversion above the customer-defined VCC LO alarm level is required before the MOD DAC is updated with the value determined by the temperature conversion and the modulation LUT.

When the MOD DAC is set, the BIAS DAC is set to a value equal to ISTEP (see Figure 1). The startup algorithm checks if this bias current causes a feedback voltage above the APC set point, and if not, it continues increasing the BIAS DAC by ISTEP until the APC set-point is exceeded. When the APC set point is exceeded, the device begins a binary search to quickly reach the bias current corresponding to the proper power level. After the binary search is completed, the APC integrator is enabled and single LSB steps are used to tightly control the average power.

The TXP HI, TXP LO, HBAL, and BIAS MAX QT alarms are masked until the binary search is completed. However, the BIAS MAX alarm is monitored during this time to prevent the BIAS DAC from exceeding IBIASMAX. During the bias current initialization, the BIAS DAC is not allowed to exceed IBIASMAX. If this occurs during the ISTEP sequence, then the binary search routine is

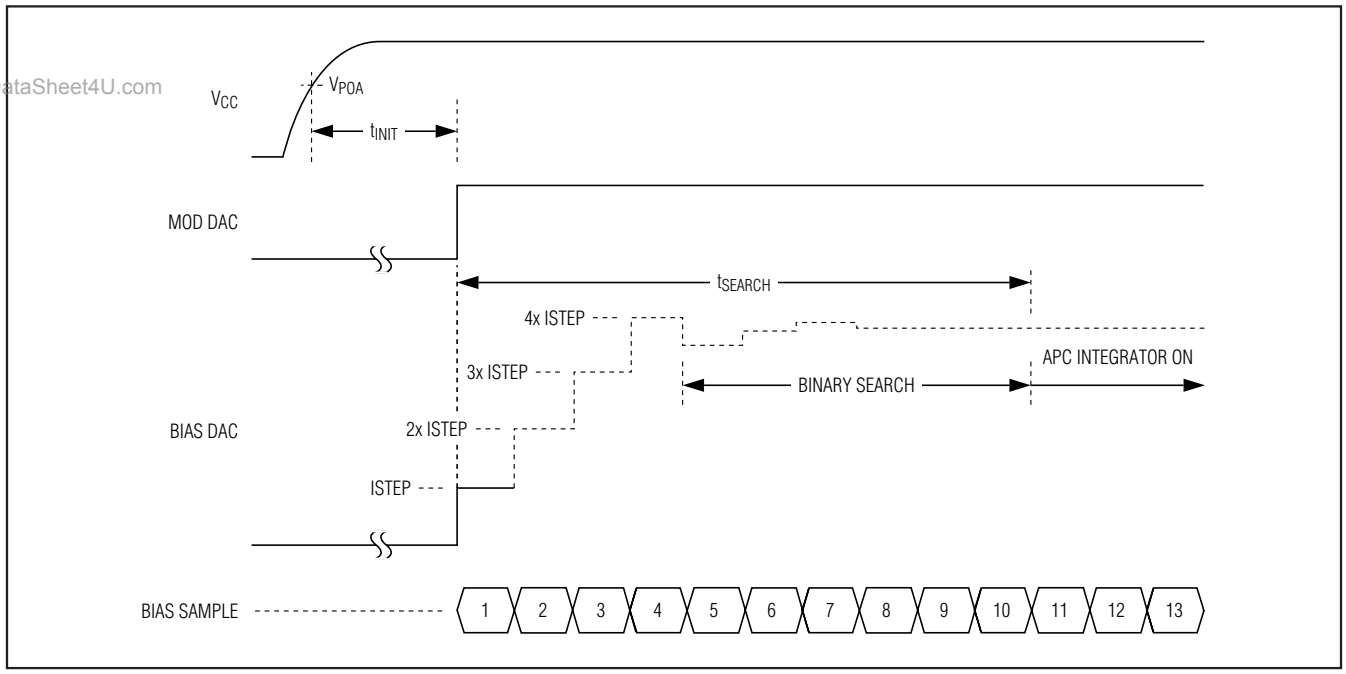


Figure 1. Power-Up Timing

enabled. If IBIASMAX is exceeded during the binary search, the next smaller step is activated. ISTEP or binary increments that would cause the BIAS DAC to exceed IBIASMAX are not taken. Masking the alarms until the completion of the binary search prevents false positive alarms during startup.

ISTEP is programmed by the customer using Table 02h, Register BBh. ISTEP should be programmed to the maximum safe increase that is allowable during startup. If this value is programmed too low, the DS1873 still operates, but it could take significantly longer for the algorithm to converge and hence to control the average power.

If a fault is detected, and TXD is toggled to reenable the outputs, the DS1873 powers up following a similar sequence to an initial power-up. The only difference is that the DS1873 already has determined the present temperature, so the t_{INIT} time is not required for the DS1873 to recall the APC and MOD set points from EEPROM.

BIAS and MOD DACs as a Function of Transmit Disable (TXD)

If TXD is asserted (logic 1) during normal operation, the outputs are disabled within t_{OFF}. When TXD is deasserted (logic 0), the DS1873 sets the MOD DAC register with the value associated with the present temperature, and initializes the BIAS DAC using the same search algorithm as done at startup. When asserted, soft TXD (TXDC) (Lower Memory, Register 6Eh) would allow a software control identical to the TXD pin (see Figure 2).

APC and Quick-Trip Timing

As shown in Figure 3, the DS1873's input comparator is shared between the APC control loop and the quick-trip alarms (TXP HI, TXP LO, LOS LO, and BIAS HI). The comparator polls the alarms in a multiplexed sequence. Five of every eight comparator readings are used for APC loop bias-current control. The other three updates are used to check the HTXP/LTXP (monitor diode voltage), the HBATH (MON1), and LOS (MON3) signals against the internal APC, BIAS, and MON3 reference, respectively. If the last APC comparison was higher than the APC set point, it makes an HTXP comparison, and if it is lower, it makes an LTXP comparison. Depending on the results of the comparison, the corresponding alarms and warnings (TXP HI, TXP LO) are asserted or deasserted.

The DS1873 has a programmable comparator sample time based on an internally generated clock to facilitate a wide variety of external filtering options and time delays. The UPDATE RATE register (Table 02h, Register 88h) determines the sampling time. Samples occur at a regular interval, t_{REP}, which is set at 1.6µs. Table 2 shows the sample rate options available. Any quick-trip alarm that is detected by default remains active until a subsequent comparator sample shows the condition no longer exists. A second bias current monitor (BIAS MAX) compares the BIAS DAC's code to a digital value stored in the IBIASMAX register. This comparison is made at every bias current update to ensure that a high-bias current is quickly detected.

The quick-trip comparator uses a 1.6µs window to sample each input. After an APC comparison that requires

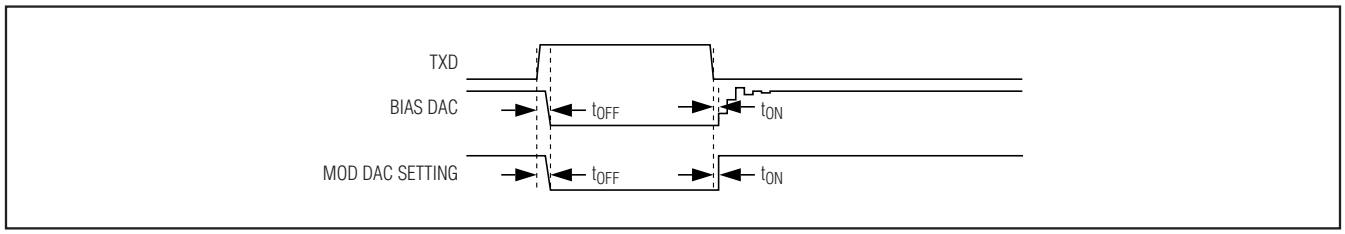


Figure 2. TXD Timing

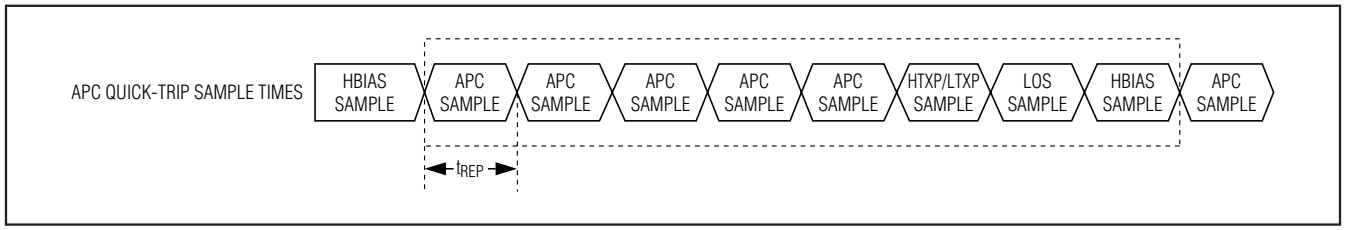


Figure 3. APC Loop and Quick-Trip Sample Timing

an update to the BIAS DAC, a settling time (as calculated below) is required to allow for the feedback on BMD (MON2) to stabilize. This time is dependent on the time constant of the filter pole used for the delta-to-sigma BIAS output. During the timing of the settling rate, comparisons of APC comparisons of BMD are ignored until 32 sample periods (t_{REP}) have passed.

SettlingTime = 51.2µs x (APC_SR[3:0] + 1)

Monitors and Fault Detection

Monitors

Monitoring functions on the DS1873 include five quick-trip comparators and six ADC channels. This monitoring combined with the alarm enables (Table 01h/05h) determines when/if the DS1873 turns off the MOD and BIAS DACs and triggers the TXF and TXDOUT outputs. All the monitoring levels and interrupt masks are user programmable.

Five Quick-Trip Monitors and Alarms

Five quick-trip monitors are provided to detect potential laser safety issues and LOS status. These monitor the following:

1) High Bias Current (HBATH)
2) Low Transmit Power (LTXP)
3) High Transmit Power (HTXP)
4) Max Output Current (IBIASMAX)
5) Loss-of-Signal (LOS LO)

The high-transmit and low-transmit power quick-trip registers (HTXP and LTXP) set the thresholds used to compare against the MON2 voltage to determine if the transmit power is within specification. The HBATH quick trip compares the MON1 input (generally from the laser driver's bias monitor output) against its threshold setting to determine if the present bias current is above specification. The BIAS MAX quick trip determines if the BIAS DAC is above specification (IBIASMAX). When the new BIAS DAC value is calculated, it is compared against the IBIAS MAX register. The BIAS DAC is not allowed to exceed the value set in the IBIASMAX register. When the DS1873 detects that the bias is at the limit, it sets the BIASMAX status bit and holds the BIAS DAC setting at the IBIASMAX level. The bias and power quick trips are routed to the TXF through interrupt masks to allow combinations of these alarms to be used to trigger these outputs. The user can program up to eight different temperature-indexed threshold levels for MON1 (Table 02h, Registers D0h–D7h). The LOS LO quick trip compares the MON3 input against its threshold setting to determine if the present received power is below the specification. The LOS LO quick trip can be used to set the LOSOUT pin.

Six ADC Monitors and Alarms

The ADC monitors six channels that measure temperature (internal temp sensor), V_{CC}, and MON1–MON4 using an analog multiplexer to measure them round robin with a single ADC (see the *ADC Timing* section). The five voltage channels have a customer-programmable full-scale range and all channels have a customer-programmable offset value that is factory programmed to default value (see Table 2). Additionally, MON1–MON4 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I^2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range to measure small signals. The DS1873 can then right-shift the results by n bits to maintain the bit weight of their specification (see the *Right-Shifting ADC Result* and *Enhanced RSSI Monitoring (Dual-Range Functionality)* sections).

Table 2. ADC Default Monitor Full-Scale Ranges

SIGNAL	+FS SIGNAL	+FS hex	-FS SIGNAL	-FS hex
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
MON1–MON4 (V)	2.4997	FFF8	0	0000

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms are set, which can be used to trigger the TXF output. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the TXF output.

ADC Timing

There are six analog channels that are digitized in a round-robin fashion in the order shown in Figure 4. The total time required to convert all six channels is t_{RR} (see the *Electrical Characteristics* for details).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of

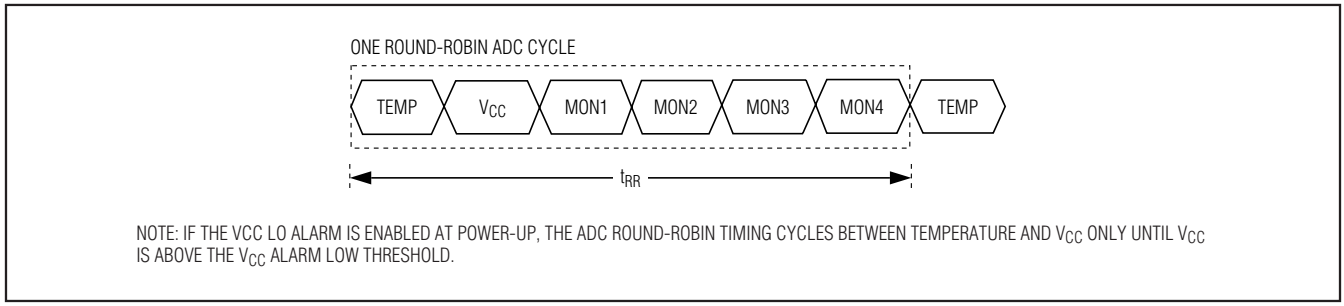


Figure 4. ADC Round-Robin Timing

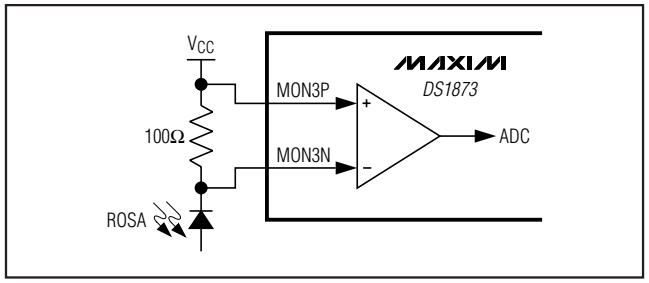


Figure 5. MON3 Differential Input for High-Side RSSI

the ADC results. The DS1873's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 of the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (Table 02h, Registers 8Eh–8Fh) in EEPROM. Four analog channels, MON1–MON4, each have 3 bits allocated to set the number of right-shifts. Up to 7 right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high-alarm and low-alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h–6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Differential MON3 Input

The DS1873 offers a fully differential input for MON3. This enables high-side monitoring of RSSI, as shown in Figure 5. This reduces board complexity by eliminating the need for a high-side differential amplifier or a current mirror.

Enhanced RSSI Monitoring (Dual-Range Functionality)

The DS1873 offers a feature to improve the accuracy and range of MON3, which is most commonly used for monitoring RSSI. The accuracy of the RSSI measurements is increased at the small cost of reduced range (of input signal swing). The DS1873 eliminates this trade-off by offering "dual range" calibration on the MON3 channel (see Figure 5). This feature enables right-shifting (along with its gain and offset settings) when the input signal is below a set threshold (within the range that benefits using right-shifting) and then automatically disables right-shifting (recalling different gain and offset settings) when the input signal exceeds the threshold. Also, to prevent "chattering," hysteresis prevents excessive switching between modes in addition to ensuring that continuity is maintained. Dual-range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled through the RSSI_FC and RSSI_FF bits, which are described in the *Register Descriptions* section. When dual-range operation is disabled, MON3 operates identically to the other MON channels, although featuring a differential input.

Dual-range functionality consists of two modes of operation: fine mode and coarse mode. Each mode is calibrated for a unique transfer function, hence the term, dual range. Table 4 highlights the registers related to MON3. Fine mode is equivalent to the other MON channels. Fine mode is calibrated using the gain, offset, and right-shifting registers at locations shown in Table 4 and is ideal for relatively small analog input voltages. Coarse mode is automatically switched to when the input exceeds a threshold (to be discussed in a subsequent paragraph). Coarse mode is calibrated using different gain and offset registers, but lacks right-shifting (since coarse mode is only used on large input signals). The gain and offset registers for coarse mode are also shown in Table 4.

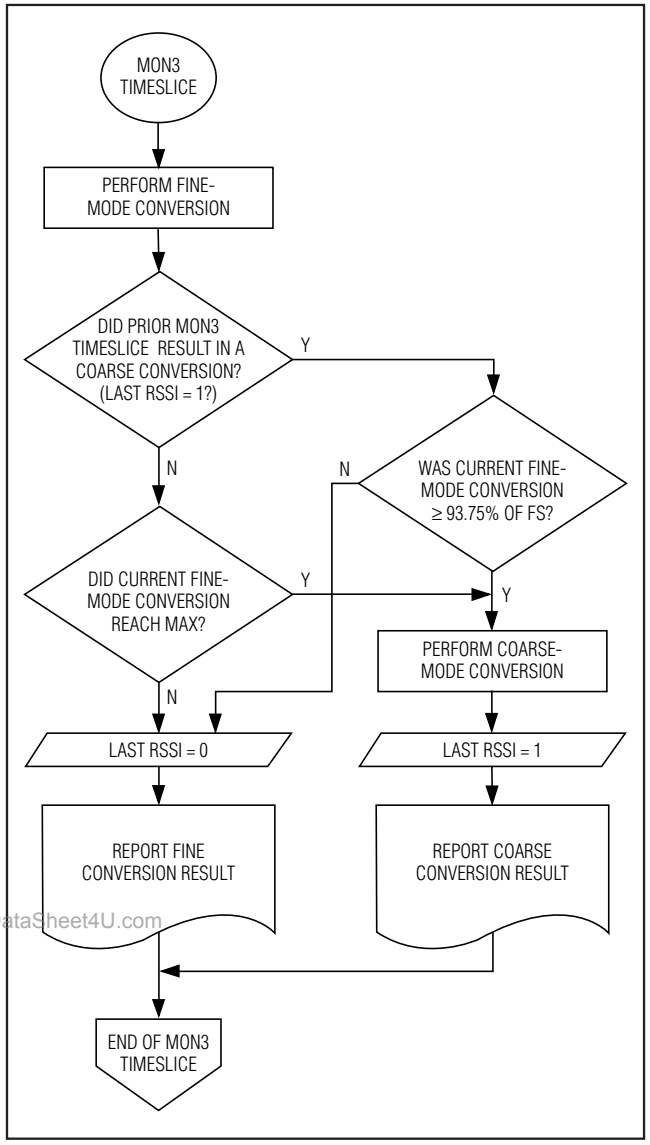


Figure 6. RSSI Flowchart

Additional information for each of the registers can be found in the *Register Descriptions* section.

Dual-range operation is transparent to the end user. The results of MON3 analog-to-digital conversions are still stored/reported in the same memory locations (68h–69h, Lower Memory) regardless of whether the conversion was performed in fine mode or coarse mode. The only way to tell which mode generated the digital result is by reading the RSSIS bit.

When the DS1873 is powered up, analog-to-digital conversions begin in a round-robin fashion. Every MON3 timeslice begins with a fine mode analog-to-digital conversion (using fine mode's gain, offset, and right-shifting settings). See the flowchart in Figure 6 for more details. Then, depending on whether the last MON3 timeslice resulted in a coarse-mode conversion and also depending on the value of the current fine conversion, decisions are made whether to use the current fine-mode conversion result or to make an additional conversion (within the same MON3 timeslice), using coarse mode (using coarse mode's gain and offset settings and no right-shifting) and reporting the coarse-mode result. The flowchart in Figure 6 also illustrates how hysteresis is implemented. The fine-mode conversion is compared to one of two thresholds. The actual threshold values are a function of the number of right-shifts being used. With the use of right-shifting, the fine mode full-scale is programmed to ($1/2^N$th) of the coarse mode full-scale. The DS1873 now auto ranges to choose the range that gives the best resolution for the measurement. Hysteresis is applied to eliminate chatter when the input resides at the boundary of the two ranges. See Figure 6 for details. Table 3 shows the threshold values for each possible number of right-shifts.

Table 3. MON3 Hysteresis Threshold Values

NUMBER OF RIGHT-SHIFTS	FINE MODE MAX (hex)	COARSE MODE MIN* (hex)
0	FFF8	F000
1	7FFC	7800
2	3FFE	3C00
3	1FFF	1E00
4	0FFF	0F00
5	07FF	0780
6	03FF	03C0
7	01FF	01E0

**This is the minimum reported coarse-mode conversion.*

Table 4. MON3 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
GAIN	98h–99h, Table 02h	9Ch–9Dh, Table 04h
OFFSET	A8h–A9h, Table 02h	ADh–ACh, Table 04h
RIGHT-SHIFT$_0$	8Fh, Table 04h	—
CNFGC	8Bh, Table 02h	
CONFIG (RSSIS BIT)	77h, Lower Memory	
MON3 VALUE	68h–69h, Lower Memory	

SFP+ Controller with Analog LDD Interface

The RSSI_FF and RSSI_FC bits are used to force fine-mode or coarse-mode conversions, or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSI_FC and RSSI_FF are factory programmed to 0 in EEPROM). It can be disabled by setting RSSI_FC to 0 and RSSI_FF to 1. These bits are also useful when calibrating MON3. For additional information, see Figure 18. The dual-range calibration can operate in two modes: crossover enabled and crossover disabled.

- **Crossover Enabled:** For systems with nonlinear relationships between the ADC input and the desired ADC result, the mode should be set to crossover enabled. The RSSI measurement of an APD receiver is one such application. Using the crossover-enabled mode allows a piecewise linear approximation of the nonlinear response of the APD's gain factor. The crossover point is the point between fine and coarse points. The ADC result transitions between the fine and coarse ranges with no hysteresis. Right-shifting, slope adjustment, and offset are configurable for both the fine and coarse ranges. See Figure 7.
- **Crossover Disabled:** The crossover-disabled mode is intended for systems with a linear relationship between the MON3 input and the desired ADC result. Hysteresis allows for a nonjittery response when the input is at the crossover boundary of the fine and coarse DAC. In a nonlinear system, the hysteresis could cause significant errors in the ADC result. See Figure 8.

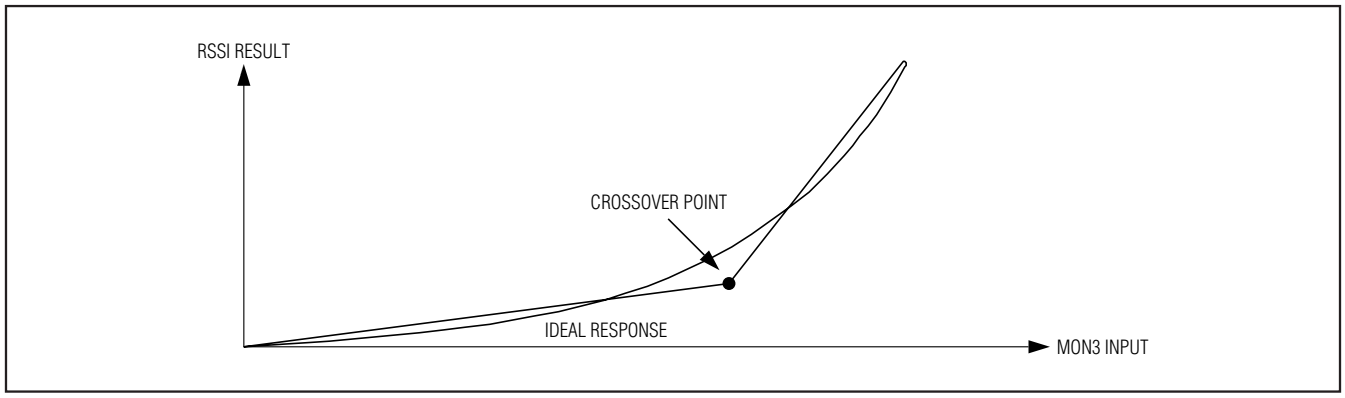


Figure 7. RSSI with Crossover Enabled

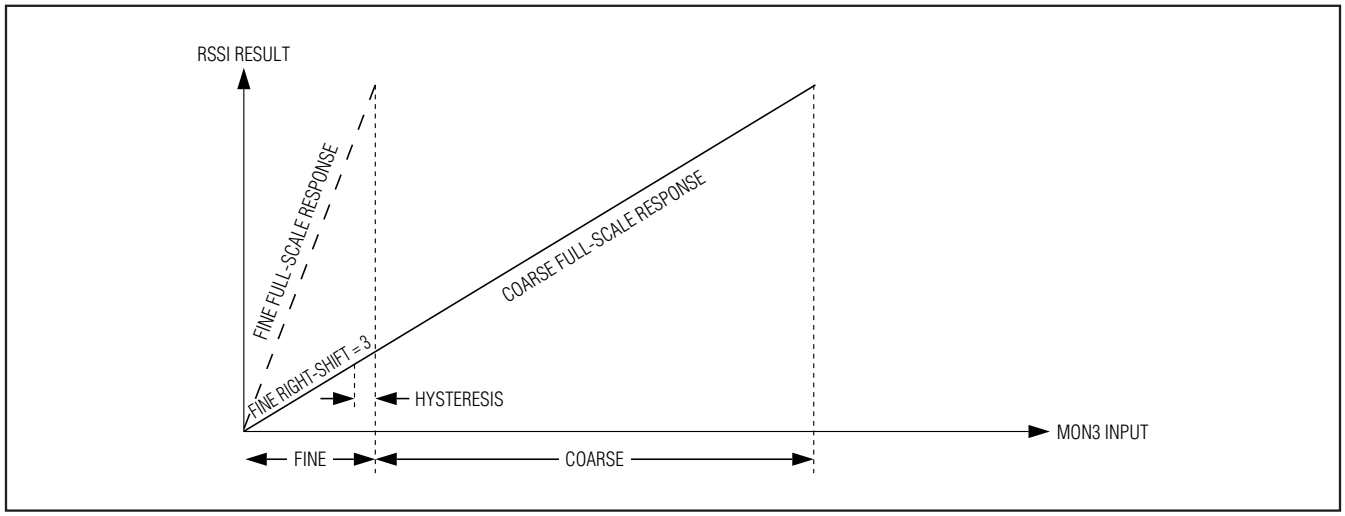


Figure 8. RSSI with Crossover Disabled

Low-Voltage Operation

The DS1873 contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM (SEE) locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, then the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs disabled. If the supply voltage recovers back above POA, then the device immediately resumes normal operation. If the supply voltage falls below POD, then the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} exceeds POA. Figure 8 shows the sequence of events as the voltage varies.

Any time V_{CC} is above POD, the I^2C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS (Lower Memory, Register 6Eh) byte. RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Ch), the default device address is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Power-On Analog (POA)

POA holds the DS1873 in reset until V_{CC} is at a suitable level (V_{CC} > POA) for the device to accurately measure with its ADC and compare analog signals with its quick-trip monitors. Because V_{CC} cannot be measured by the ADC when V_{CC} is less than POA, POA also asserts the VCC LO alarm, which is cleared by a V_{CC} ADC conversion greater than the customer-programmable V_{CC} alarm LO ADC limit. This allows a programmable limit to ensure that the headroom requirements of the transceiver are satisfied during a slow power-up. The TXF output does not latch until there is a conversion above V_{CC} low limit. The POA alarm is nonmaskable. The TXF output is asserted when V_{CC} is below POA. See the *Low-Voltage Operation* section for more information.

Delta-Sigma Outputs

Four delta-sigma outputs are provided: MOD DAC, BIAS DAC, DAC1, and DAC2. With the addition of an external RC filter, these outputs provide 10-bit resolution analog outputs with the full-scale range set by the input REFIN. Each output is either manually controlled or controlled using a temperature-indexed LUT, or in the case of the BIAS DAC, controlled by the APC loop. A delta-sigma is a digital output using pulse-density modulation. It provides much lower output ripple than a

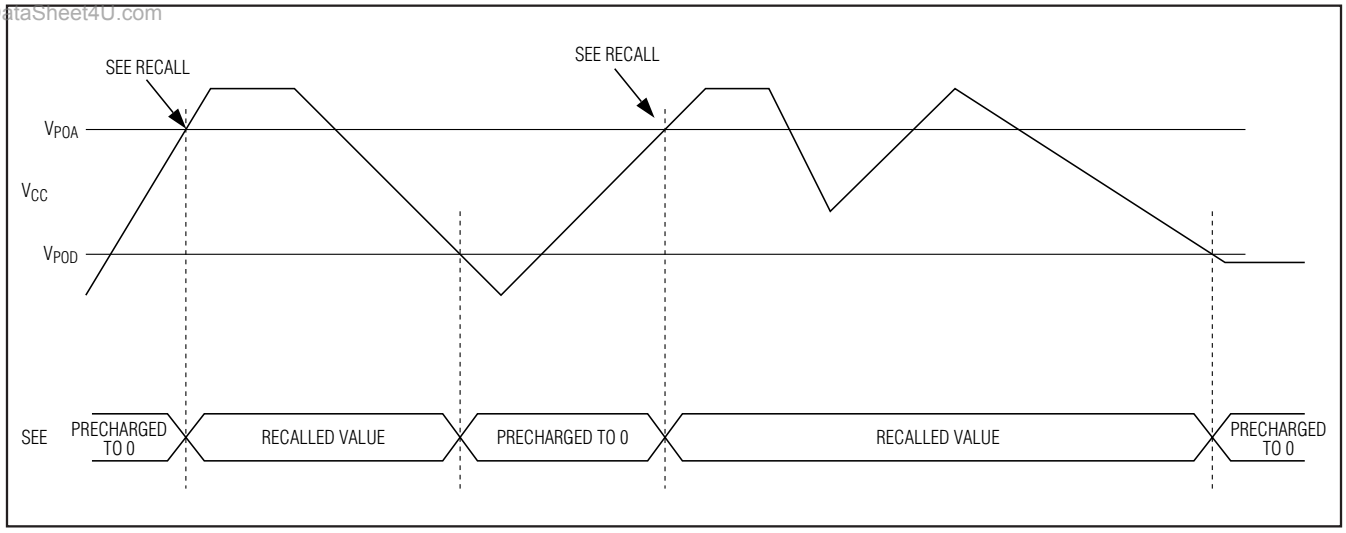


Figure 9. Low-Voltage Hysteresis Example

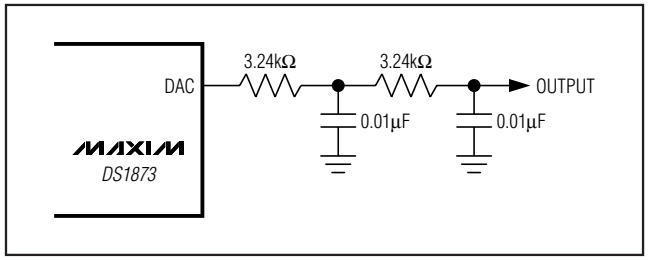


Figure 10. Recommended RC Filter for DAC1/DAC2

standard digital PWM output given the same clock rate and filter components. Before t_{INIT}, the DAC outputs are high impedance.

The external RC filter components are chosen based on ripple requirements, output load, delta-sigma frequency, and desired response time. A recommended filter is shown in Figure 10.

The DS1873's delta-sigma outputs are 10 bits. For illustrative purposes, a 3-bit example is provided. Each possible output of this 3-bit delta-sigma DAC is given in Figure 11.

In LUT mode, MOD, DAC1, and DAC2 are each controlled by an LUT with high-temperature resolution and an OFFSET LUT with lower temperature resolution. The MOD and DAC1 high-resolution LUTs each have 2°C resolution. The DAC2 high-resolution LUT has 4°C resolution. The OFFSET LUTs are located in the upper eight registers (F8h–FFh) of the table containing each high-resolution LUT. MOD DAC, DAC1 VALUE, and DAC2 VALUE are determined as follows:

MOD DAC = MOD LUT + 4 x (MOD OFFSET LUT)

DAC1 VALUE = DAC1 LUT + 4 x (DAC1 OFFSET LUT)

DAC2 VALUE = DAC1 LUT + 4 x (DAC1 OFFSET LUT)

Example calculation for MOD DAC:

Assumptions:

1) Temperature is 43°C.
2) Table 04h (MOD OFFSET LUT), Register FCh = 2Ah.
3) Table 04h (MOD LUT), Register A9h = 7Bh.

Because the temperature is 43°C, the MOD LUT index is A9h and the MOD OFFSET LUT index is FCh.

MOD DAC = 7Bh + 4 x 2Ah = 123h = 291

When temperature controlled, the DACs are updated after each temperature conversion.

The reference input, REFIN, is the supply voltage for all four DACs. The voltage connected to REFIN and its decoupling must be able to support the edge rate requirements of the delta-sigma outputs.

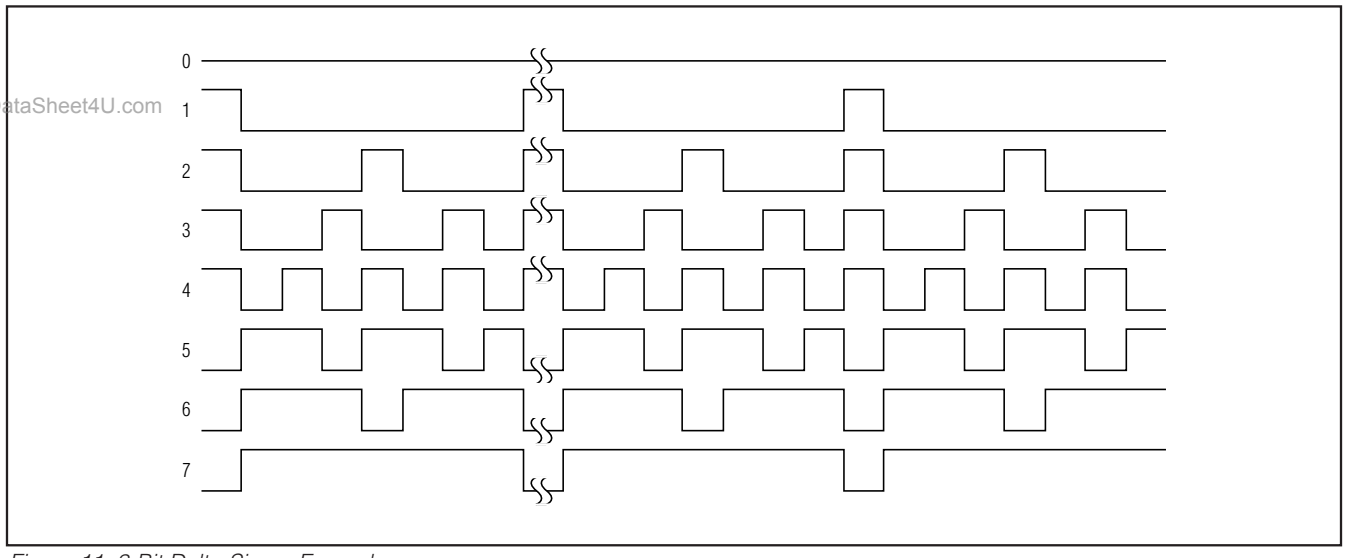


Figure 11. 3-Bit Delta-Sigma Example

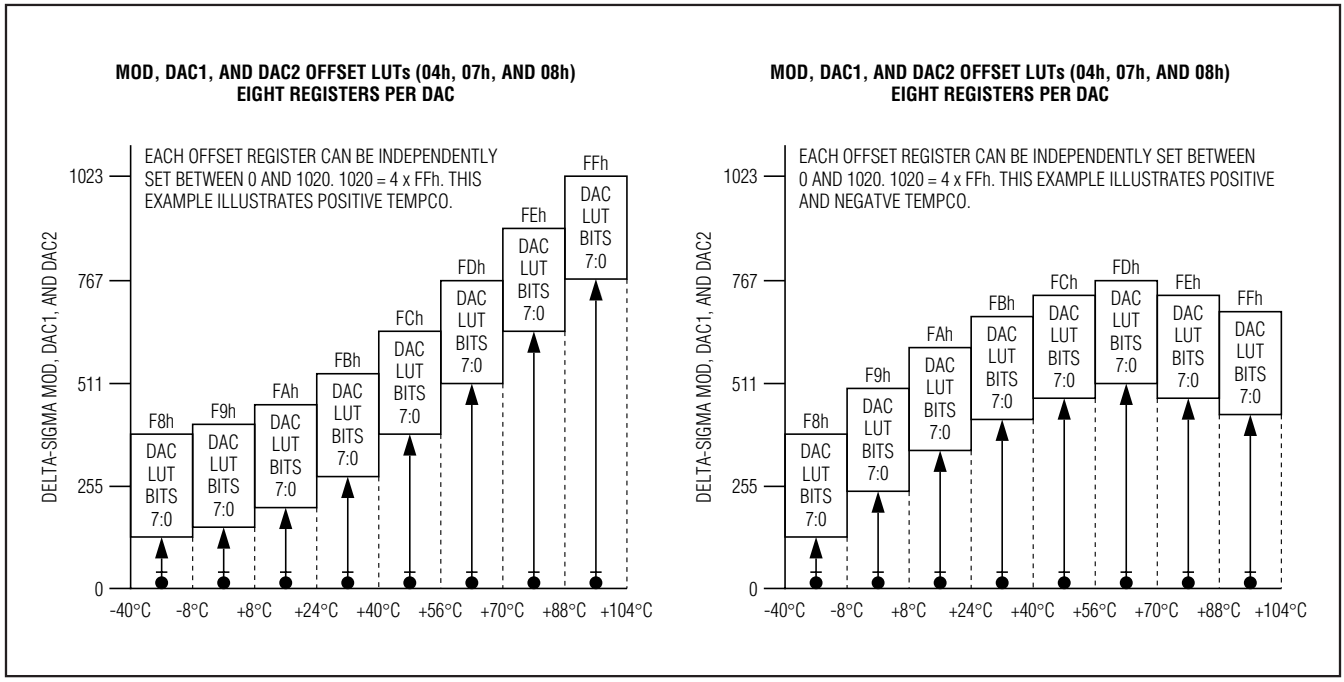


Figure 12. MOD, DAC1, and DAC2 Offset LUTs

Digital I/O Pins

Five digital input and five digital output pins are provided for monitoring and control.

LOS, LOSOUT

By default (LOSC = 1, Table 02h, Register 89h), the LOS pin is used to convert a standard comparator output for loss of signal (LOS) to an open-collector output. This means the mux shown in the *Block Diagram* by default selects the LOS pin as the source for the LOSOUT output transistor. The output of the mux can be read in the STATUS byte (Table 01h, Register 6Eh) as the RXL bit. The RXL signal can be inverted (INV LOS = 1) before driving the open-drain output transistor using the XOR gate provided. Setting LOSC = 0 configures the mux to be controlled by LOS LO, which is driven by the output of the LOS quick trip (Table 02h, Registers BEh and BFh). The mux setting (stored in EEPROM) does not take effect until V_{CC} > POA, allowing the EEPROM to recall.

IN1, RSEL, OUT1, RSELOUT

The digital input IN1 and RSEL pins primarily serve to meet the rate-select requirements of SFP and SFP+. They also serve as general-purpose inputs. OUT1 and RSELOUT are driven by a combination of the IN1, RSEL, and logic dictated by control registers in the EEPROM (Figure 14). The levels of IN1 and RSEL can be read using the STATUS register (Lower Memory, Register 6Eh). The open-drain output OUT1 can be controlled and/or inverted using the CNFGB register (Table 02h, Register 8Ah). The open-drain RSELOUT output is software-controlled and/or inverted through the STATUS register and CNFGA register (Table 02h, Register 89h). External pullup resistors must be provided on OUT1 and RSELOUT to realize high logic levels.

SFP+ Controller with Analog LDD Interface

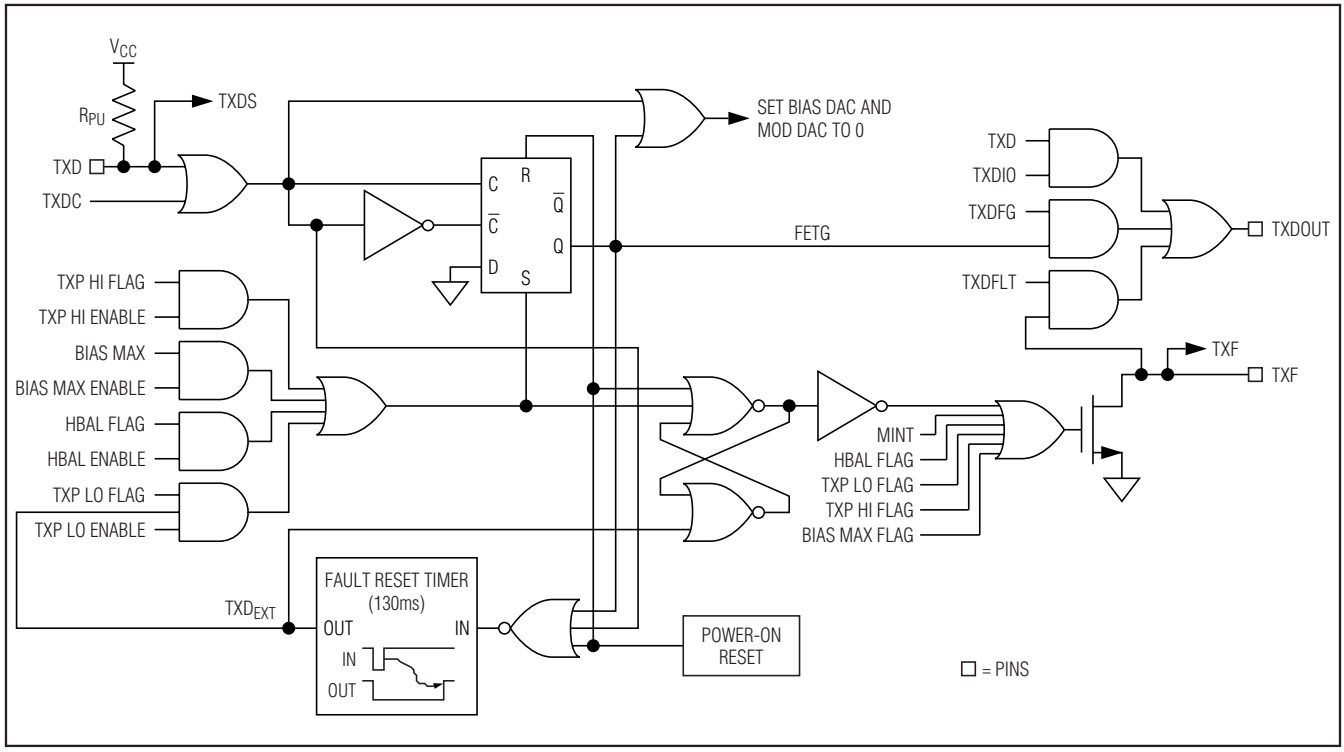


Figure 13. Logic Diagram 1

TXF, TXD, TXDOUT

TXDOUT is generated from a combination of TXF, TXD, and the internal signal FETG. A software control identical to TXD is available (TXDC, Lower Memory, Register 6Eh). A TXD pulse is internally extended (TXD_{EXT}) by time t_{INITR1} to inhibit the latching of low alarms and warnings related to the APC loop to allow for the loop to stabilize. The nonlatching alarms and warnings are TXP LO, LOS LO, and MON1–MON4 LO alarms and warnings. In addition, TXP LO is disabled from creating FETG. TXF is both an input and an output (Figure 13). See the *Transmit Fault (TXF) Output* section for a detailed explanation of TXF. Figure 13 shows that the same signals and faults can also be used to generate the internal signal FETG (Table 01h/05h, Registers FAh and FBh). FETG is used to send a fast "turn-off" command to the laser driver. The intended use is a direct connection to the laser driver's TXD input if this is desired. When V_{CC} < POA, TXDOUT is high impedance.

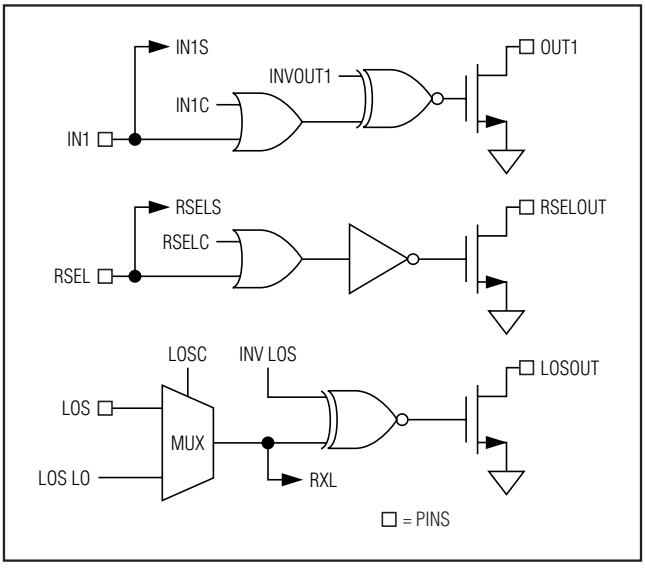


Figure 14. Logic Diagram 2

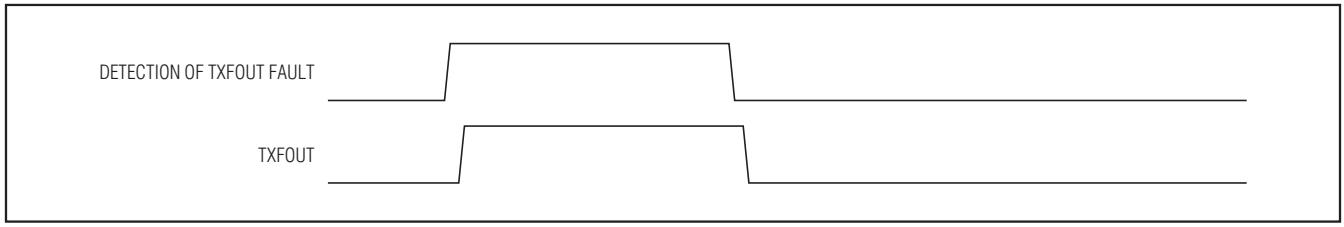


Figure 15a. TXF Nonlatched Operation

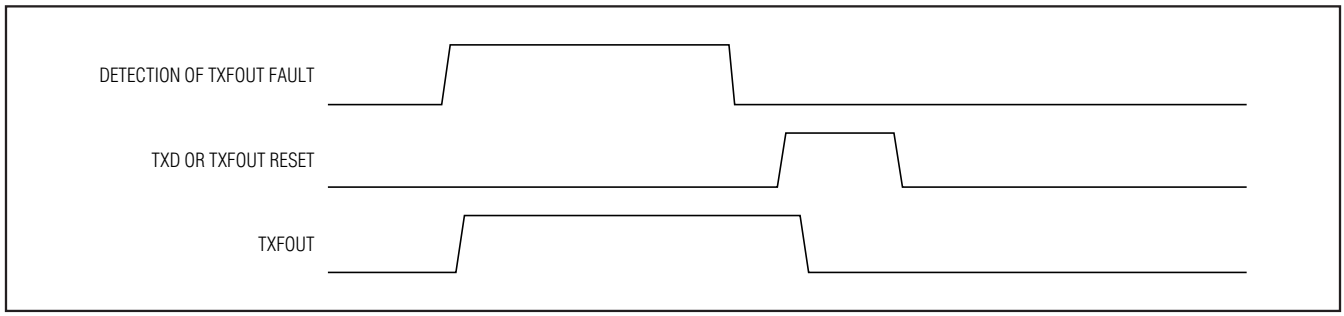


Figure 15b. TXF Latched Operation

Transmit Fault (TXF) Output

TXF can be triggered by all alarms, warnings, and quick trips (Figure 13). The six ADC alarms, warnings, and the LOS quick trips require enabling (Table 01h/05h, Registers F8h and FDh). See Figures 15a and 15b for nonlatched and latched operation. Latching of the alarms is controlled by the CNFGB and CNFGC registers (Table 02h, Registers 8Ah–8Bh).

Die Identification

The DS1873 has an ID hardcoded in its die. Two registers (Table 02h, Registers CEh–CFh) are assigned for this feature. The CEh register reads 73h to identify the part as the DS1873, while the CFh register reads the current device version.

I²C Communication

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 16 for applicable timing.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 16 for applicable timing.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 16 for applicable timing.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (Figure 16). Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 16) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not acknowledge (NACK) is always the ninth bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the ninth bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 16) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition and the acknowledgement is read using the bit-read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit-read definition, and the master transmits an ACK using the bit-write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave address byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS1873 responds to two slave addresses. The auxiliary memory always responds to a fixed I²C slave address, A0h. The Lower Memory and Tables 00h–08h respond to I²C slave addresses that can be configured to any value between 00h–FEh using the DEVICE ADDRESS byte (Table 02h, Register 8Ch). The user also must set the ASEL bit (Table 02h, Register 89h) for this address to be active. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it will write data to the slave. If R/$\overline{W}$

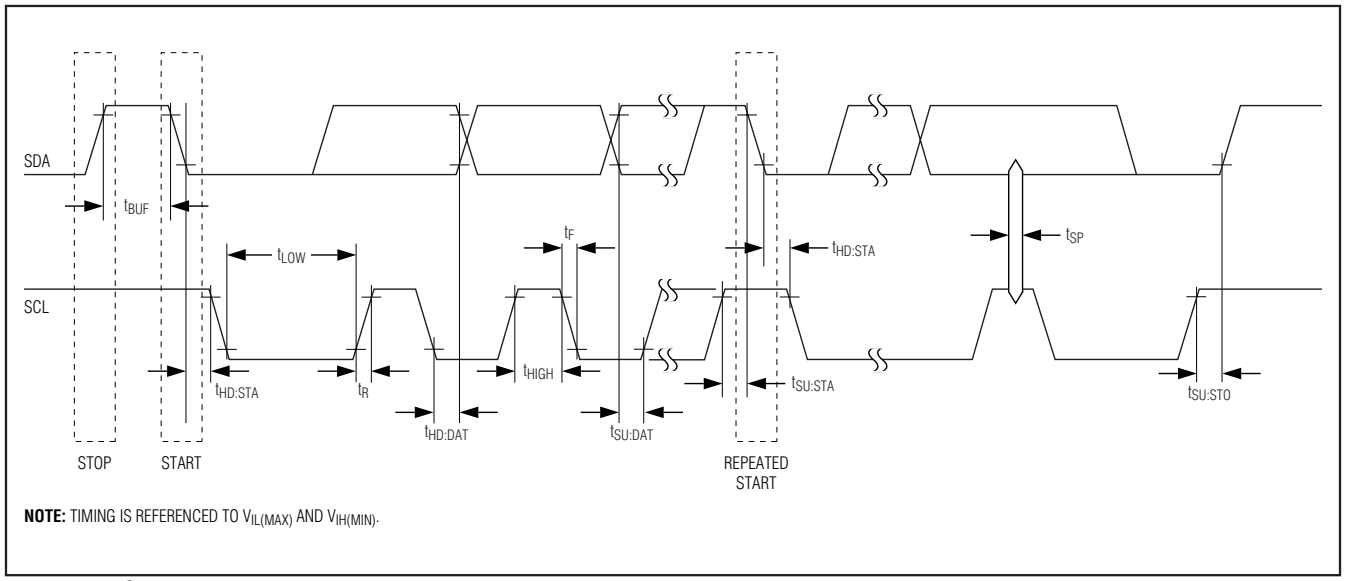


Figure 16. I²C Timing

= 1, the master reads data from the slave. If an incorrect slave address is written, the DS1873 assumes the master is communicating with another I²C device and ignores the communications until the next START condition is sent. If the main device's slave address is programmed to be A0h, access to the auxiliary memory is disabled.

Memory address: During an I²C write operation to the DS1873, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Protocol

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgement during all byte-write operations.

Writing multiple bytes to a slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS1873 writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row.

For example, a 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address

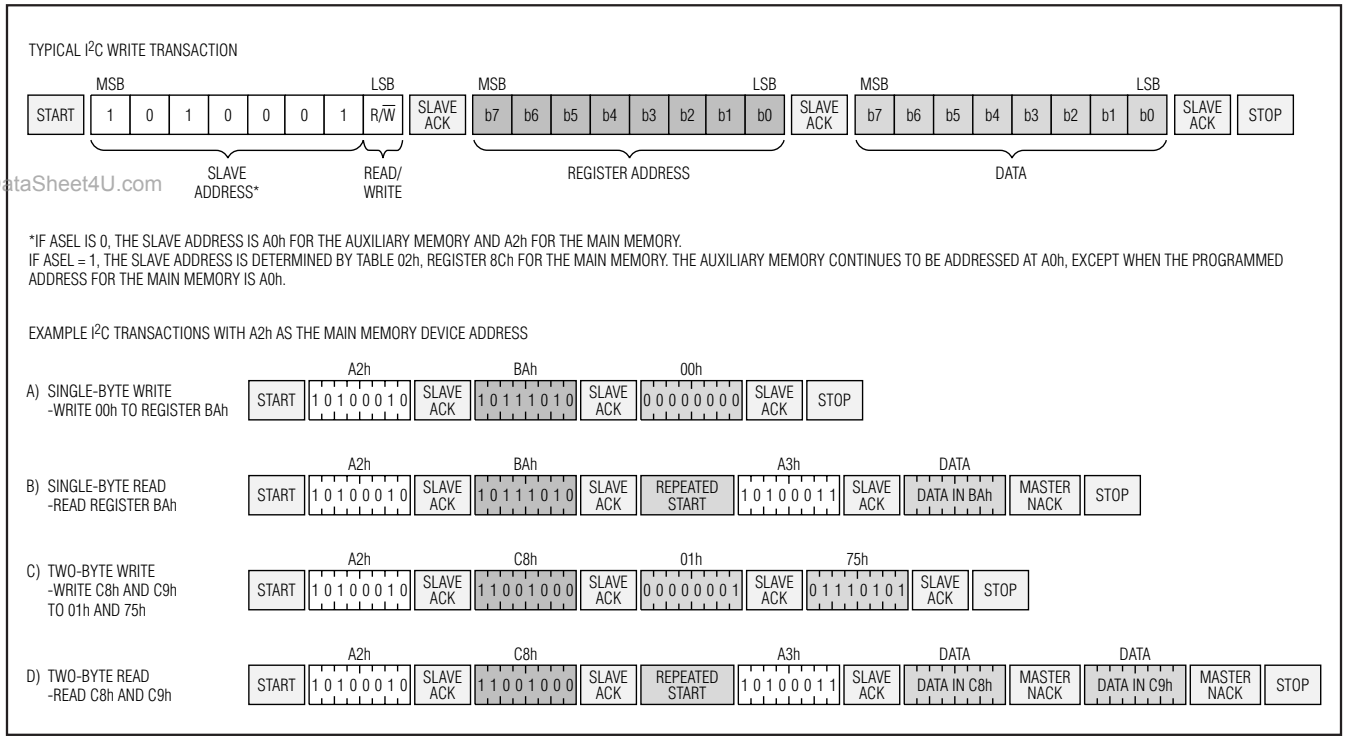


Figure 17. Example I²C Timing

byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge polling: Any time a EEPROM page is written, the DS1873 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the DS1873 will not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the DS1873, which allows the next page to be written as soon as the DS1873 is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t_W to elapse before attempting to write again to the DS1873.

EEPROM write cycles: When EEPROM writes occur, the DS1873 writes the whole EEPROM memory page, even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page one byte at a time wears the EEPROM out eight times faster than writing the entire page at once. The DS1873's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It can handle approximately ten times that many writes at room temperature. Writing to SRAM-shadowed EEPROM memory with SEEB = 1 does not count as an EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a single byte from a slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Memory Organization

The DS1873 features nine separate memory tables that are internally organized into 8-byte rows.

The DS1873 has two passwords that are each 4 bytes long. The lower level password (PW1) has all the access of a normal user plus those made available with PW1. The higher level password (PW2) has all the access of PW1 plus those made available with PW2. The values of the passwords reside in EEPROM inside of PW2 memory. At power-up, all PWE bits are set to 1, and all reads at this location are 0.

The **Lower Memory** is addressed from 00h to 7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the table-select byte.

Table 01h primarily contains user EEPROM (with PW1 level access) as well as alarm and warning-enable bytes.

Table 02h is a multifunction space that contains configuration registers, scaling and offset values, passwords, interrupt registers as well as other miscellaneous control bytes.

Table 04h contains a temperature-indexed LUT for control of the modulation output. The modulation LUT can be programmed in 2°C increments over the -40°C to +102°C range. The table also contains a temperature-indexed LUT for MOD offsets.

Table 05h is empty by default. It can be configured to contain the alarm- and warning-enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 89h). In this case Table 01h is empty.

Table 06h contains a temperature-indexed LUT that allows the APC set point to change as a function of temperature to compensate for tracking error (TE). The APC LUT has 36 entries that determine the APC setting in 4°C windows between -40°C and +100°C. The table also contains a temperature-indexed LUT for HBIAS thresholds.

Table 07h contains a temperature-indexed LUT for control of DAC1. The LUT has 72 entries that determine the DAC setting in 4°C windows between -40°C and +100°C. The table also contains a temperature-indexed LUT for DAC1 offsets.

Table 08h contains a temperature-indexed LUT for control of DAC2. The LUT has 36 entries that determine the DAC setting in 4°C windows between -40°C and +100°C.

Auxiliary Memory (device A0h) contains 256 bytes of EE memory accessible from address 00h–FFh. It is selected with the device address of A0h.

See the *Register Descriptions* section for more complete details of each byte's function, as well as for read/write permissions for each byte.

Shadowed EEPROM

Many NV memory locations (listed within the *Register Descriptions* section) are actually shadowed EEPROM that are controlled by the SEEB bit in Table 02h, Register 80h.

The DS1873 incorporates shadowed-EEPROM memory locations for key memory addresses that can be written many times. By default the shadowed-EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. Setting SEEB also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. Figure 18 indicates which locations are shadowed EEPROM.

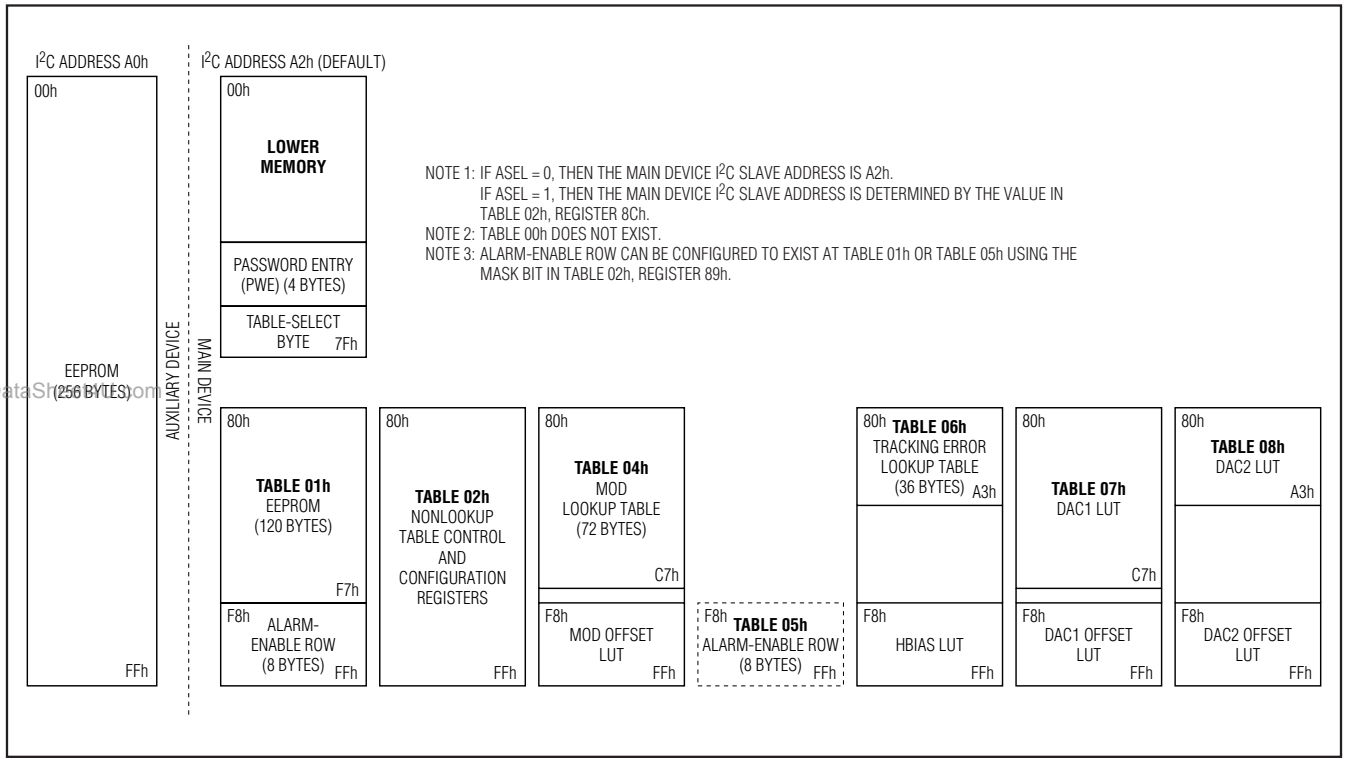


Figure 18. Memory Map

SFP+ Controller with Analog LDD Interface

Register Descriptions

The register maps show each byte/word (2 bytes) in terms of its row in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the leftmost column. Each subsequent byte on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. For more information about each of these bytes see the corresponding register description.

Lower Memory Register Map

LOWER MEMORY									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00	<1>THRESHOLD$_0$	TEMP ALARM HI		TEMP ALARM LO		TEMP WARN HI		TEMP WARN LO	
08	<1>THRESHOLD$_1$	V_{CC} ALARM HI		V_{CC} ALARM LO		V_{CC} WARN HI		V_{CC} WARN LO	
10	<1>THRESHOLD$_2$	MON1 ALARM HI		MON1 ALARM LO		MON1 WARN HI		MON1 WARN LO	
18	<1>THRESHOLD$_3$	MON2 ALARM HI		MON2 ALARM LO		MON2 WARN HI		MON2 WARN LO	
20	<1>THRESHOLD$_4$	MON3 ALARM HI		MON3 ALARM LO		MON3 WARN HI		MON3 WARN LO	
28	<1>THRESHOLD$_5$	MON4 ALARM HI		MON4 ALARM LO		MON4 WARN HI		MON4 WARN LO	
30–5F	<1>EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
60	<2>ADC VALUES$_0$	TEMP VALUE		V_{CC} VALUE		MON1 VALUE		MON2 VALUE	
68	<0>ADC VALUES$_1$	<2>MON3 VALUE		<2>MON4 VALUE		<2>RESERVED		<0>STATUS	<5>UPDATE
70	<2>ALARM/ WARN	ALARM$_3$	ALARM$_2$	ALARM$_1$	ALARM$_0$	WARN$_3$	WARN$_2$	RESERVED	
78	<0>TABLE SELECT	<5>RESERVED		<5> RESERVED	<6>PWE MSW		<6>PWE LSW		<5>TBL SEL

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1873 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 01h Register Map

TABLE 01h									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–BF	<7>EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
C0–F7	<8>EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
F8	<8>ALARM ENABLE	ALARM EN_3	ALARM EN_2	ALARM EN_1	ALARM EN_0	WARN EN_3	WARN EN_2	RESERVED	RESERVED

The ALARM ENABLE bytes (Registers F8h–FFh) can be configured to exist in Table 05h instead of here at Table 01h with the MASK bit (Table 02h, Register 89h). If the row is configured to exist in Table 05h, then these locations are empty in Table 01h.

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1873 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

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Table 02h Register Map

TABLE 02h									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<0>CONFIG$_0$	<8>MODE	<4>TINDEX	<4>MOD DAC		<4>DAC1 VALUE		<4>DAC2 VALUE	
88	<8>CONFIG$_1$	UPDATE RATE	CNFGA	CNFGB	CNFGC	DEVICE ADDRESS	RSHIFT$_2$	RSHIFT$_1$	RSHIFT$_0$
90	<8>SCALE$_0$	XOVER COARSE		V_{CC} SCALE		MON1 SCALE		MON2 SCALE	
98	<8>SCALE$_1$	MON3 FINE SCALE		MON4 SCALE		MON3 COARSE SCALE		RESERVED	
A0	<8>OFFSET$_0$	XOVER FINE		V_{CC} OFFSET		MON1 OFFSET		MON2 OFFSET	
A8	<8>OFFSET$_1$	MON3 FINE OFFSET		MON4 OFFSET		MON3 COARSE OFFSET		INTERNAL TEMP OFFSET*	
B0	<9>PWD VALUE	PW1 MSW		PW1 LSW		PW2 MSW		PW2 LSW	
B8	<8>THRESHOLD	LOS RANGING	COMP RANGING	IBIASMAX	ISTEP	HTXP	LTXP	HLOS	LLOS
C0	<8>PWD ENABLE	PW_ENA	PW_ENB	RESERVED	RESERVED	RESERVED	RESERVED	POLARITY	TBLSELPON
C8	<0>BIAS	<4>MAN BIAS		<4>MAN_ CNTL	<10>BIAS DAC		RESERVED	<10>DEVICE ID	<10>DEVICE VER
D0	<8>APC	<4>APC DAC	<4>HBIAS DAC	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
D8–E7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY

**The final result must be XORed with BB40h before writing to this register.*

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1873 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 04h Register Map

TABLE 04h (MODULATION LUT)									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
88	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
90	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
98	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
A0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
A8	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
B0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
B8	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
C0	<8>LUT4	MOD	MOD	MOD	MOD	MOD	MOD	MOD	MOD
C8–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<8>MOD OFFSET	MOD OFF	MOD OFF	MOD OFF	MOD OFF	MOD OFF	MOD OFF	MOD OFF	MOD OFF

Table 05h Register Map

TABLE 05h									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<8>ALARM ENABLE	ALARM EN_3	ALARM EN_2	ALARM EN_1	ALARM EN_0	WARN EN_3	WARN EN_2	RESERVED	RESERVED

Table 05h is empty by default. It can be configured to contain the alarm and warning-enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 89h). In this case Table 01h is empty.

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1873 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

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Table 06h Register Map

TABLE 06h (APC LUT)									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–9F	<8>LUT6	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
88	<8>LUT6	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
90	<8>LUT6	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
98	<8>LUT6	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF	APC REF
A0	<8>LUT6	APC REF	APC REF	APC REF	APC REF	RESERVED	RESERVED	RESERVED	RESERVED
A8–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<8>HBATH	HBIAS	HBIAS	HBIAS	HBIAS	HBIAS	HBIAS	HBIAS	HBIAS

Table 07h Register Map

TABLE 07h (DAC1 LUT)									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
88	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
90	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
98	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
A0	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
A8	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
B0	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
B8	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
C0	<8>LUT7	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
C8–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<8>DAC1 OFFSET	DAC1 OFF	DAC1 OFF	DAC1 OFF	DAC1 OFF	DAC1 OFF	DAC1 OFF	DAC1 OFF	DAC1 OFF

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1873 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 08h Register Map

TABLE 08h (DAC2 LUT)									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	<8>LUT8	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2
88	<8>LUT8	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2
90	<8>LUT8	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2
98	<8>LUT8	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2	DAC2
A0	<8>LUT8	DAC2	DAC2	DAC2	DAC2	RESERVED	RESERVED	RESERVED	RESERVED
C8–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8	<8>DAC2 OFFSET	DAC2 OFF	DAC2 OFF	DAC2 OFF	DAC2 OFF	DAC2 OFF	DAC2 OFF	DAC2 OFF	DAC2 OFF

Auxiliary A0h Memory Register Map

AUXILIARY MEMORY (A0h)									
ROW (hex)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00–7F	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE
80–FF	<5>AUX EE	EE	EE	EE	EE	EE	EE	EE	EE

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0>	<1>	<2>	<3>	<4>	<5>	<6>	<7>	<8>	<9>	<10>	<11>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1873 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Lower Memory, Register 00h–01h: TEMP ALARM HI
Lower Memory, Register 04h–05h: TEMP WARN HI

FACTORY DEFAULT	7FFFh
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
MEMORY TYPE	Nonvolatile (SEE)

00h, 04h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
01h, 05h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Temperature measurement updates above this two's complement threshold set corresponding alarm or warning bits. Temperature measurement updates equal to or below this threshold clear alarm or warning bits.

Lower Memory, Register 02h–03h: TEMP ALARM LO
Lower Memory, Register 06h–07h: TEMP WARN LO

FACTORY DEFAULT	8000h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
MEMORY TYPE	Nonvolatile (SEE)

02h, 06h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
03h, 07h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Temperature measurement updates below this two's complement threshold set corresponding alarm or warning bits. Temperature measurement updates equal to or above this threshold clear alarm or warning bits.

Lower Memory, Register 08h–09h: V_{CC} ALARM HI
Lower Memory, Register 0Ch–0Dh: V_{CC} WARN HI
Lower Memory, Register 10h–11h: MON1 ALARM HI
Lower Memory, Register 14h–15h: MON1 WARN HI
Lower Memory, Register 18h–19h: MON2 ALARM HI
Lower Memory, Register 1Ch–1Dh: MON2 WARN HI
Lower Memory, Register 20h–21h: MON3 ALARM HI
Lower Memory, Register 24h–25h: MON3 WARN HI
Lower Memory, Register 28h–29h: MON4 ALARM HI
Lower Memory, Register 2Ch–2Dh: MON4 WARN HI

FACTORY DEFAULT	FFFFh
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
MEMORY TYPE	Nonvolatile (SEE)

08h, 0Ch, 10h, 14h, 18h, 1Ch, 20h, 24h, 28h, 2Ch	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
09h, 0Dh, 11h, 15h, 19h, 1Dh, 21h, 25h, 29h, 2Dh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Voltage measurement updates above this unsigned threshold set corresponding alarm or warning bits. Voltage measurements equal to or below this threshold clear alarm or warning bits.

Lower Memory, Register 0Ah–0Bh: V_{CC} ALARM LO
Lower Memory, Register 0Eh–0Fh: V_{CC} WARN LO
Lower Memory, Register 12h–13h: MON1 ALARM LO
Lower Memory, Register 16h–17h: MON1 WARN LO
Lower Memory, Register 1Ah–1Bh: MON2 ALARM LO
Lower Memory, Register 1Eh–1Fh: MON2 WARN LO
Lower Memory, Register 22h–23h: MON3 ALARM LO
Lower Memory, Register 26h–27h: MON3 WARN LO
Lower Memory, Register 2Ah–2Bh: MON4 ALARM LO
Lower Memory, Register 2Eh–2Fh: MON4 WARN LO

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
MEMORY TYPE	Nonvolatile (SEE)

0Ah, 0Eh, 12h, 16h, 1Ah, 1Eh, 22h, 26h, 2Ah, 2Eh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
0Bh, 0Fh, 13h, 17h, 1Bh, 1Fh, 23h, 27h, 2Bh, 2Fh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

 Voltage measurement updates below this unsigned threshold set corresponding alarm or warning bits. Voltage measurements equal to or above this threshold clear alarm or warning bits.

Lower Memory, Register 30h–5Fh: EE

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
MEMORY TYPE	Nonvolatile (EE)

30h–5Fh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

PW2 level access-controlled EEPROM.

Lower Memory, Register 60h–61h: TEMP VALUE

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

60h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
61h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Signed two’s complement direct-to-temperature measurement.

Lower Memory, Register 62h–63h: V_{CC} VALUE
Lower Memory, Register 64h–65h: MON1 VALUE
Lower Memory, Register 66h–67h: MON2 VALUE
Lower Memory, Register 68h–69h: MON3 VALUE
Lower Memory, Register 6Ah–6Bh: MON4 VALUE

POWER-ON VALUE	0000h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

62h, 64h, 66h, 68h, 6Ah	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
63h, 65h, 67h, 69h, 6Bh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Left-justified unsigned voltage measurement.

Lower Memory, Register 6Ch–6Dh: RESERVED

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	

6Ch, 6Dh	0	0	0	0	0	0	0	0
	BIT 7							BIT 0

These registers are reserved. The value when read is 00h.

Lower Memory, Register 6Eh: STATUS

POWER-ON VALUE	X0XX 0XXXb
READ ACCESS	All
WRITE ACCESS	See below
MEMORY TYPE	Volatile

Write Access	N/A	All	N/A	All	All	N/A	N/A	N/A
6Eh	TXDS	TXDC	IN1S	RSELS	RSELC	TXFS	RXL	RDYB
	BIT 7							BIT 0

BIT 7	**TXDS:** TXD Status Bit. Reflects the logic state of the TXD pin (read only). 0 = TXD pin is logic-low. 1 = TXD pin is logic-high.
BIT 6	**TXDC:** TXD Software Control Bit. This bit allows for software control that is identical to the TXD pin. See the section on TXD for further information. Its value is wire-ORed with the logic value of the TXD pin (writable by all users). 0 = (Default). 1 = Forces the device into a TXD state regardless of the value of the TXD pin.
BIT 5	**IN1S:** IN1 Status Bit. Reflects the logic state of the IN1 pin (read only). 0 = IN1 pin is logic-low. 1 = IN1 pin is logic-high.
BIT 4	**RSELS:** RSEL Status Bit. Reflects the logic state of the RSEL pin (read only). 0 = RSEL pin is logic-low. 1 = RSEL pin is logic-high.
BIT 3	**RSELC:** RSEL Software Control Bit. This bit allows for software control that is identical to the RSEL pin. Its value is wire-ORed with the logic value of the RSEL pin to create the RSELOUT pin's logic value (writable by all users). 0 = (Default). 1 = Forces the device into a RSEL state regardless of the value of the RSEL pin.
BIT 2	**TXFS:** Reflects the driven state of the TXF pin (read only). 0 = TXF pin is low. 1 = TXF pin is high.
BIT 1	**RXL:** Reflects the driven state of the LOSOUT pin (read only). 0 = LOSOUT pin is driven low. 1 = LOSOUT pin is pulled high.
BIT 0	**RDYB:** Ready Bar. 0 = V_{CC} is above POA. 1 = V_{CC} is below POA and/or too low to communicate over the I^2C bus.

Lower Memory, Register 6Fh: UPDATE

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	All and DS1873 Hardware
MEMORY TYPE	Volatile

6Fh	TEMP RDY	VCC RDY	MON1 RDY	MON2 RDY	MON3 RDY	MON4 RDY	RESERVED	RSSIR
	BIT 7							BIT 0

BITS 7:2	Update of completed conversions. At power-on, these bits are cleared and are set as each conversion is completed. These bits can be cleared so that a completion of a new conversion is verified.
BIT 1	**RESERVED**
BIT 0	**RSSIR:** RSSI Range. Reports the range used for conversion update of MON3. 0 = Fine range is the reported value. 1 = Coarse range is the reported value.

Lower Memory, Register 70h: ALARM3

POWER-ON VALUE	10h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

70h	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High-alarm status for temperature measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low-alarm status for temperature measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High-alarm status for V_{CC} measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low-alarm status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (Default) Last measurement was below threshold setting.
BIT 3	**MON1 HI:** High-alarm status for MON1 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 2	**MON1 LO:** Low-alarm status for MON1 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 1	**MON2 HI:** High-alarm status for MON2 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 0	**MON2 LO:** Low-alarm status for MON2 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.

Lower Memory, Register 71h: $ALARM_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

71h	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	TXFINT
	BIT 7							BIT 0

BIT 7	**MON3 HI:** High-alarm status for MON3 measurement. A TXD event does not clear this alarm. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**MON3 LO:** Low-alarm status for MON3 measurement. A TXD event does not clear this alarm. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**MON4 HI:** High-alarm status for MON4 measurement. A TXD event does not clear this alarm. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**MON4 LO:** Low-alarm status for MON4 measurement. A TXD event does not clear this alarm. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BITS 3:1	**RESERVED**
BIT 0	**TXFINT:** TXF Interrupt. This bit is the wire-ORed logic of all alarms and warnings wire-ANDed with their corresponding enable bits in addition to nonmaskable alarms TXP HI, TXP LO, BIAS MAX, and HBAL. The enable bits are found in Table 01h/05h, Registers F8h–FFh.

Lower Memory, Register 72h: ALARM$_1$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

72h	RESERVED	RESERVED	RESERVED	RESERVED	HBAL	RESERVED	TXP HI	TXP LO
	BIT 7							BIT 0

BITS 7:4	**RESERVED**
BIT 3	**HBAL:** High-Bias Alarm Status; Fast Comparison. A TXD event clears this alarm. 0 = (Default) Last comparison was below threshold setting. 1 = Last comparison was above threshold setting.
BIT 2	**RESERVED**
BIT 1	**TXP HI:** High-Alarm Status TXP; Fast Comparison. A TXD event clears this alarm. 0 = (Default) Last comparison was below threshold setting. 1 = Last comparison was above threshold setting.
BIT 0	**TXP LO:** Low-Alarm Status TXP; Fast Comparison. A TXD event clears this alarm. 0 = (Default) Last comparison was above threshold setting. 1 = Last comparison was below threshold setting.

Lower Memory, Register 73h: ALARM$_0$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

73h	LOS HI	LOS LO	RESERVED	RESERVED	BIAS MAX	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**LOS HI:** High-Alarm Status for MON3; Fast Comparison. A TXD event does not clear this alarm. 0 = (Default) Last comparison was below threshold setting. 1 = Last comparison was above threshold setting.
BIT 6	**LOS LO:** Low-Alarm Status for MON3; Fast Comparison. A TXD event does not clear this alarm. 0 = (Default) Last comparison was above threshold setting. 1 = Last comparison was below threshold setting.
BITS 5:4	**RESERVED**
BIT 3	**BIAS MAX:** Alarm status for maximum digital setting of BIAS. A TXD event clears this alarm. 0 = (Default) The value for BIAS is equal to or below the IBIASMAX register. 1 = Requested value for BIAS is greater than the IBIASMAX register.
BITS 2:0	**RESERVED**

Lower Memory, Register 74h: $WARN_3$

POWER-ON VALUE	10h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

74h	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High-warning status for temperature measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low-warning status for temperature measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High-warning status for V_{CC} measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low-warning status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (Default) Last measurement was below threshold setting.
BIT 3	**MON1 HI:** High-warning status for MON1 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 2	**MON1 LO:** Low-warning status for MON1 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 1	**MON2 HI:** High-warning status for MON2 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 0	**MON2 LO:** Low-warning status for MON2 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.

Lower Memory, Register 75h: $WARN_2$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

75h	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**MON3 HI:** High-warning status for MON3 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**MON3 LO:** Low-warning status for MON3 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**MON4 HI:** High-warning status for MON4 measurement. 0 = (Default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**MON4 LO:** Low-warning status for MON4 measurement. 0 = (Default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BITS 3:0	**RESERVED**

Lower Memory, Register 76h–7Ah: RESERVED MEMORY

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
MEMORY TYPE	

These registers are reserved. The value when read is 00h.

Lower Memory, Register 7Bh–7Eh: Password Entry (PWE)

POWER-ON VALUE	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	All
MEMORY TYPE	Volatile

7Bh	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
7Ch	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
7Dh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
7Eh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

There are two passwords for the DS1873. Each password is 4 bytes long. The lower level password (PW1) has all the access of a normal user plus those made available with PW1. The higher level password (PW2) has all the access of PW1 plus those made available with PW2. The values of the passwords reside in EEPROM inside PW2 memory. At power-up, all PWE bits are set to 1. All reads at this location are 0.

Lower Memory, Register 7Fh: Table Select (TBL SEL)

POWER-ON VALUE	TBLSELPON (Table 02h, Register C7h)
READ ACCESS	All
WRITE ACCESS	All
MEMORY TYPE	Volatile

7Fh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The upper memory tables of the DS1873 are accessible by writing the desired table value in this register. The power-on value of this register is defined by the value written to TBLSELPON (Table 02h, Register C7h).

Table 01h, Register 80h–BFh: EEPROM

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1A) or (PW1 and RTBL1A)
WRITE ACCESS	PW2 or (PW1 and RWTBL1A)
MEMORY TYPE	Nonvolatile (EE)

80h–BFh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

EEPROM for PW1 and/or PW2 level access.

Table 01h, Register C0h–F7h: EEPROM

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1B) or (PW1 and RTBL1B)
WRITE ACCESS	PW2 or (PW1 and RWTBL1B)
MEMORY TYPE	Nonvolatile (EE)

C0h–F7h	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

EEPROM for PW1 and/or PW2 level access.

Table 01h, Register F8h: ALARM EN_3

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

F8h	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

Layout is identical to $ALARM_3$ in Lower Memory, Register 70h. Enables alarms to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (Table 02h, Register 89h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**TEMP HI:** 0 = Disables interrupt from TEMP HI alarm. 1 = Enables interrupt from TEMP HI alarm.
BIT 6	**TEMP LO:** 0 = Disables interrupt from TEMP LO alarm. 1 = Enables interrupt from TEMP LO alarm.
BIT 5	**VCC HI:** 0 = Disables interrupt from VCC HI alarm. 1 = Enables interrupt from VCC HI alarm.
BIT 4	**VCC LO:** 0 = Disables interrupt from VCC LO alarm. 1 = Enables interrupt from VCC LO alarm.
BIT 3	**MON1 HI:** 0 = Disables interrupt from MON1 HI alarm. 1 = Enables interrupt from MON1 HI alarm.
BIT 2	**MON1 LO:** 0 = Disables interrupt from MON1 LO alarm. 1 = Enables interrupt from MON1 LO alarm.
BIT 1	**MON2 HI:** 0 = Disables interrupt from MON2 HI alarm. 1 = Enables interrupt from MON2 HI alarm.
BIT 0	**MON2 LO:** 0 = Disables interrupt from MON2 LO alarm. 1 = Enables interrupt from MON2 LO alarm.

Table 01h, Register F9h: ALARM EN_2

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

F9h	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to $ALARM_2$ in Lower Memory, Register 71h. Enables alarms to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (Table 02h, Register 89h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**MON3 HI:** 0 = Disables interrupt from MON3 HI alarm. 1 = Enables interrupt from MON3 HI alarm.
BIT 6	**MON3 LO:** 0 = Disables interrupt from MON3 LO alarm. 1 = Enables interrupt from MON3 LO alarm.
BIT 5	**MON4 HI:** 0 = Disables interrupt from MON4 HI alarm. 1 = Enables interrupt from MON4 HI alarm.
BIT 4	**MON4 LO:** 0 = Disables interrupt from MON4 LO alarm. 1 = Enables interrupt from MON4 LO alarm.
BIT 3:0	**RESERVED**

Table 01h, Register FAh: ALARM EN$_1$

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

FAh	RESERVED	RESERVED	RESERVED	RESERVED	HBAL	RESERVED	TXP HI	TXP LO
	BIT 7							BIT 0

Layout is identical to ALARM$_1$ in Lower Memory, Register 72h. Enables alarms to create internal signal FETG (see Figure 12) logic. The MASK bit (Table 02h, Register 89h) determines whether this memory exists in Table 01h or 05h.

BITS 7:4	**RESERVED**
BIT 3	**HBAL:** 0 = Disables interrupt from HBAL alarm. 1 = Enables interrupt from HBAL alarm.
BIT 2	**RESERVED**
BIT 1	**TXP HI:** 0 = Disables interrupt from TXP HI alarm. 1 = Enables interrupt from TXP HI alarm.
BIT 0	**TXP LO:** 0 = Disables interrupt from TXP LO alarm. 1 = Enables interrupt from TXP LO alarm.

Table 01h, Register FBh: ALARM EN$_0$

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

FBh	LOS HI	LOS LO	RESERVED	RESERVED	BIAS MAX	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to ALARM$_1$ in Lower Memory, Register 73h. The MASK bit (Table 02h, Register 89h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**LOS HI:** Enables alarm to create TXFINT (Lower Memory, Register 71h) logic. 0 = Disables interrupt from LOS HI alarm. 1 = Enables interrupt from LOS HI alarm.
BIT 6	**LOS LO:** Enables alarm to create TXFINT (Lower Memory, Register 71h) logic. 0 = Disables interrupt from LOS LO alarm. 1 = Enables interrupt from LOS LO alarm.
BITS 5:4	**RESERVED**
BIT 3	**BIAS MAX:** Enables alarm to create internal signal FETG (see Figure 12) logic. 0 = Disables interrupt from BIAS MAX alarm. 1 = Enables interrupt from BIAS MAX alarm.
BITS 2:0	**RESERVED**

Table 01h, Register FCh: WARN EN_3

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

FCh	TEMP HI	TEMP LO	VCC HI	VCC LO	MON1 HI	MON1 LO	MON2 HI	MON2 LO
	BIT 7							BIT 0

Layout is identical to $WARN_3$ in Lower Memory, Register 74h. Enables warnings to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (Table 02h, Register 89h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**TEMP HI:** 0 = Disables interrupt from TEMP HI warning. 1 = Enables interrupt from TEMP HI warning.
BIT 6	**TEMP LO:** 0 = Disables interrupt from TEMP LO warning. 1 = Enables interrupt from TEMP LO warning.
BIT 5	**VCC HI:** 0 = Disables interrupt from VCC HI warning. 1 = Enables interrupt from VCC HI warning.
BIT 4	**VCC LO:** 0 = Disables interrupt from VCC LO warning. 1 = Enables interrupt from VCC LO warning.
BIT 3	**MON1 HI:** 0 = Disables interrupt from MON1 HI warning. 1 = Enables interrupt from MON1 HI warning.
BIT 2	**MON1 LO:** 0 = Disables interrupt from MON1 LO warning. 1 = Enables interrupt from MON1 LO warning.
BIT 1	**MON2 HI:** 0 = Disables interrupt from MON2 HI warning. 1 = Enables interrupt from MON2 HI warning.
BIT 0	**MON2 LO:** 0 = Disables interrupt from MON2 LO warning. 1 = Enables interrupt from MON2 LO warning.

Table 01h, Register FDh: WARN EN_2

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

FDh	MON3 HI	MON3 LO	MON4 HI	MON4 LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to $WARN_2$ in Lower Memory, Register 75h. Enables warnings to create TXFINT (Lower Memory, Register 71h) logic. The MASK bit (Table 02h, Register 89h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**MON3 HI:** 0 = Disables interrupt from MON3 HI warning. 1 = Enables interrupt from MON3 HI warning.
BIT 6	**MON3 LO:** 0 = Disables interrupt from MON3 LO warning. 1 = Enables interrupt from MON3 LO warning.
BIT 5	**MON4 HI:** 0 = Disables interrupt from MON4 HI warning. 1 = Enables interrupt from MON4 HI warning.
BIT 4	**MON4 LO:** 0 = Disables interrupt from MON4 LO warning. 1 = Enables interrupt from MON4 LO warning.
BITS 3:0	**RESERVED**

Table 01h, Register FEh–FFh: RESERVED

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

Table 02h Register Descriptions

Table 02h, Register 80h: MODE

POWER-ON VALUE	3Fh
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and PRTBL2)
MEMORY TYPE	Volatile

80h	SEEB	RESERVED	DAC1 EN	DAC2 EN	AEN	MOD EN	APC EN	BIAS EN
	BIT 7							BIT 0

BIT 7	**SEEB:** 0 = (Default) Enables EEPROM writes to SEE bytes. 1 = Disables EEPROM writes to SEE bytes during configuration, so that the configuration of the part is not delayed by the EE cycle time. Once the values are known, write this bit to a 0 and write the SEE locations again for data to be written to the EEPROM.
BIT 6	**RESERVED**
BIT 5	**DAC1 EN:** 0 = DAC1 VALUE is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the values for DAC1. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for DAC1 VALUE.
BIT 4	**DAC2 EN:** 0 = DAC2 VALUE is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the values for DAC2. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for DAC2 VALUE.
BIT 3	**AEN:** 0 = The temperature-calculated index value TINDEX is writable by users and the updates of calculated indexes are disabled. This allows users to interactively test their modules by controlling the indexing for the LUTs. The recalled values from the LUTs appear in the DAC registers after the next completion of a temperature conversion.
BIT 2	**MOD EN:** 0 = Modulation is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the DAC value for modulation. The output is updated with the new value at the end of the write cycle. The I^2C STOP condition is the end of the write cycle. 1 = (Default) Enables auto control of the LUT for modulation.
BIT 1	**APC EN:** 0 = APC DAC is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the DAC value for APC reference. The I^2C STOP condition is the end of the write cycle. The HBIAS DAC is also writable if recalls are disabled. 1 = (Default) Enables auto control of the LUT for APC reference.
BIT 0	**BIAS EN:** 0 = BIAS DAC is controlled by the user and the APC is in manual mode. This allows the user to interactively test their modules by writing the DAC value for bias. 1 = (Default) Enables auto control for the APC feedback.

Table 02h, Register 81h: Temperature Index (TINDEX)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and AEN = 0) or (PW1 and RWTBL2 and AEN = 0)
MEMORY TYPE	Volatile

81h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Holds the calculated index based on the temperature measurement. This index is used for the address during lookup of Tables 04h, 06h–08h. Temperature measurements below -40°C or above +102°C are clamped to 80h and C7h, respectively. The calculation of TINDEX is as follows:

$$TINDEX = \frac{Temp\_Value + 40°C}{2°C} + 80h$$

For the temperature-indexed LUTs (2°C and 4°C), the index used during the lookup function for each table is as follows:

Table 04h (MOD)	1	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$	$TINDEX_0$
Table 06h (APC)	1	0	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$
Table 07h (DAC1)	1	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$	$TINDEX_0$
Table 08h (DAC2)	1	0	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$

For the 8-position LUT tables, the following table shows the lookup function:

TINDEX	1000_0xxx	1001_0xxx	1001_1xxx	1010_0xxx	1010_1xxx	1011_0xxx	1011_1xxx	11xx_xxxx
BYTE	F8	F9	FA	FB	FC	FD	FE	FF
TEMP (°C)	< -8	-8 to +8	8 to 24	24 to 40	40 to 56	56 to 72	72 to 88	≥ 88

Table 02h, Register 82h–83h: MOD DAC

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and MOD EN = 0) or (PW1 and RWTBL2 and MOD EN = 0)
MEMORY TYPE	Volatile

82h	0	0	0	0	0	0	0	2^8
83h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for MOD DAC. It is the result of LUT4 plus MOD OFFSET times 4 recalled from Table 04h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$\text{MOD VALUE} = \text{LUT4} + \text{MOD OFFSET} \times 4$$

$$V_{MOD} = \frac{V_{REFIN}}{1024} \times \text{MOD VALUE}$$

Table 02h, Register 84h–85h: DAC1 VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RTBL246)
WRITE ACCESS	(PW2 and DAC1 EN = 0) or (PW1 and RWTBL246 and DAC1 EN = 0)
MEMORY TYPE	Volatile

84h	0	0	0	0	0	0	0	2^8
85h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for DAC1. It is the result of LUT7 plus DAC1 OFFSET times 4 recalled from Table 07h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$\text{DAC1 VALUE} = \text{LUT7} + \text{DAC1 OFFSET} \times 4$$

$$V_{DAC1} = \frac{V_{REFIN}}{1024} \times \text{DAC1 VALUE}$$

Table 02h, Register 86h–87h: DAC2 VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RTBL246)
WRITE ACCESS	(PW2 and DAC2 EN = 0) or (PW1 and RWTBL246 and DAC2 EN = 0)
MEMORY TYPE	Volatile

86h	0	0	0	0	0	0	0	2^8
87h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for DAC2. It is the result of LUT8 plus DAC2 OFFSET times 4 recalled from Table 08h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$\text{DAC2 VALUE} = \text{LUT8} + \text{DAC2 OFFSET} \times 4$$

$$V_{DAC2} = \frac{V_{REFIN}}{1024} \times \text{DAC2 VALUE}$$

Table 02h, Register 88h: UPDATE RATE

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

88h	SEE	SEE	SEE	SEE	APC_SR_3	APC_SR_2	APC_SR_1	APC_SR_0
	BIT 7							BIT 0

BITS 7:4	**SEE**
BITS 3:0	**APC_SR[3:0]:** 4-bit sample rate for comparison of APC control. Defines the sample rate for comparison of APC control.

The quick-trip comparator uses a 1.6µs window to sample each input. After an APC comparison that requires an update to the BIAS DAC, a settling time (as calculated below) is required to allow for the feedback on BMD (MON2) to stabilize. This time is dependent on the time constant of the filter pole used for the delta-to-sigma BIAS output. During the timing of the settling rate, comparisons of APC comparisons of BMD are ignored until 32 sample periods (t_{REP}) have passed.

$$\text{SettlingTime} = 51.2\mu s \times (\text{APC\_SR}[3:0] + 1)$$

Table 02h, Register 89h: CNFGA

FACTORY DEFAULT	80h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

89h	LOSC	RESERVED	INV LOS	ASEL	MASK	INVRSOUT	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**LOSC:** LOS Configuration. Defines the source for the LOSOUT pin (see Figure 14). 0 = LOS LO alarm is used as the source. 1 = (Default) LOS input pin is used as the source.
BIT 6	**RESERVED**
BIT 5	**INV LOS:** Inverts the buffered input pin LOS to output pin LOSOUT (see Figure 14). 0 = Noninverted LOS to LOSOUT pin. 1 = Inverted LOS to LOSOUT pin.
BIT 4	**ASEL:** Address Select. 0 = Device address is A2h. 1 = Byte DEVICE ADDRESS in Table 02h, Register 8Ch is used as the device address.
BIT 3	**MASK:** 0 = Alarm-enable row exists at Table 01h, Registers F8h–FFh. Table 05h, Registers F8h–FFh are empty. 1 = Alarm-enable row exists at Table 05h, Registers F8h–FFh. Table 01h, Registers F8h–FFh are empty.
BIT 2	**INVRSOUT:** Allow for inversion of RSELOUT pin (see Figure 14). 0 = RSELOUT is not inverted. 1 = RSELOUT is inverted.
BITS 1:0	**RESERVED**

Table 02h, Register 8Ah: CNFGB

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

8Ah	IN1C	INVOUT1	RESERVED	RESERVED	RESERVED	ALATCH	QTLATCH	WLATCH
	BIT 7							BIT 0

BIT 7	**IN1C:** IN1 Software Control Bit (see Figure 14). 0 = IN1 pin's logic controls OUT1 pin. 1 = OUT1 is active (bit 6 defines the polarity).
BIT 6	**INVOUT1:** Inverts the active state for OUT1 (see Figure 14). 0 = Noninverted. 1 = Inverted.
BITS 5:3	**RESERVED**
BIT 2	**ALATCH:** ADC Alarm's Comparison Latch. Table 01h, Registers 70h–71h. 0 = ADC alarm and flags reflect the status of the last comparison. 1 = ADC alarm flags remain set.
BIT 1	**QTLATCH:** Quick Trip's Comparison Latch. Table 01h, Registers 72h–73h and 76h. 0 = QT alarm and warning flags reflect the status of the last comparison. 1 = QT alarm and warning flags remain set.
BIT 0	**WLATCH:** ADC Warning's Comparison Latch. Table 01h, Registers 74h–75h. 0 = ADC warning flags reflect the status of the last comparison. 1 = ADC warning flags remain set.

Table 02h, Register 8Bh: CNFGC

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

8Bh	XOVEREN	RESERVED	TXDM34	TXDFG	TXDFLT	TXDIO	RSSI_FC	RSSI_FF
	BIT 7							BIT 0

BIT 7	**XOVEREN:** Enables RSSI conversion to use the XOVER FINE (Table 02h, Register 90h–91h) value during MON3 conversions. 0 = Uses hysteresis for linear RSSI measurements. 1 = XOVER value is enabled for nonlinear RSSI measurements.
BIT 6	**RESERVED**
BIT 5	**TXDM34:** Enables TXD to reset alarms, warnings, and quick trips associated to MON3 and MON4 during a TXD event. 0 = TXD event has no effect on the MON3 and MON4 alarms, warnings, and quick trips. 1 = MON3 and MON4 alarms, warnings, and quick trips are reset during a TXD event.
BIT 4	**TXDFG:** See Figure 13. 0 = FETG, an internal signal, has no effect on TXDOUT. 1 = FETG is enabled and ORed with other possible signals to create TXDOUT.
BIT 3	**TXDFLT:** See Figure 13. 0 = TXF pin has no effect on TXDOUT. 1 = TXF pin is enabled and ORed with other possible signals to create TXDOUT.
BIT 2	**TXDIO:** See Figure 13. 0 = (Default) TXD input signal has no effect on TXDOUT. 1 = TXD input signal is enabled and ORed with other possible signals to create TXDOUT.
BITS 1:0	**RSSI_FC and RSSI_FF:** RSSI Force Coarse and RSSI Force Fine. Control bits for RSSI mode of operation on the MON3 conversion. 00b = Normal RSSI mode of operation (default). 01b = The fine settings of scale and offset are used for MON3 conversions. 10b = The coarse settings of scale and offset are used for MON3 conversions. 11b = Normal RSSI mode of operation.

Table 02h, Register 8Ch: DEVICE ADDRESS

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

8Ch	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

This value becomes the I^2C slave address for the main memory when the ASEL (Table 02h, Register 89h) bit is set. If A0h is programmed to this register, the auxiliary memory is disabled.

Table 02h, Register 8Dh: RIGHT-SHIFT2 (RSHIFT2)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

8Dh	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	$MON3C_2$	$MON3C_1$	$MON3C_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of MON3 coarse voltage measurement. This allows for scaling the measurement to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

Table 02h, Register 8Eh: RIGHT-SHIFT$_1$ (RSHIFT$_1$)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

8Eh	RESERVED	MON1$_2$	MON1$_1$	MON1$_0$	RESERVED	MON2$_2$	MON2$_1$	MON2$_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of MON1 and MON2 voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

Table 02h, Register 8Fh: RIGHT-SHIFT$_0$ (RSHIFT$_0$)

FACTORY DEFAULT	30h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

8Fh	RESERVED	MON3F$_2$	MON3F$_1$	MON3F$_0$	RESERVED	MON4$_2$	MON4$_1$	MON4$_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of MON3 fine and MON4 voltage measurements. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB. The MON3 right-shifting is only available for the fine mode of operation. The coarse mode does not right-shift.

Table 02h, Register 90h–91h: XOVER COARSE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

90h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
91h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	0
	BIT 7							BIT 0

Defines the crossover value for RSSI measurements of nonlinear inputs when XOVEREN is set to a 1 (Table 02h, Register 8Bh). MON3 coarse conversion results (before right-shifting) less than this register are clamped to the value of this register.

Table 02h, Register 92h–93h: V_{CC} SCALE
Table 02h, Register 94h–95h: MON1 SCALE
Table 02h, Register 96h–97h: MON2 SCALE
Table 02h, Register 98h–99h: MON3 FINE SCALE
Table 02h, Register 9Ah–9Bh: MON4 SCALE
Table 02h, Register 9Ch–9Dh: MON3 COARSE SCALE

FACTORY CALIBRATED	
READ ACCESS	PW2 or (PW1 and RWTBL246) or (PW1 and RTBL246)
WRITE ACCESS	PW2 or (PW1 and RWTBL246)
MEMORY TYPE	Nonvolatile (SEE)

92h, 94h, 96h, 98h, 9Ah, 9Ch	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
93h, 95h, 97h, 99h, 9Bh, 9Dh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

Controls the scaling or gain of the FS voltage measurements. The factory-calibrated value produces an FS voltage of 6.5536V for V_{CC}; 2.5V for MON1, MON2, MON4; and 0.3125V for MON3 fine.

Table 02h, Register 9Eh–9Fh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

Table 02h, Register A0h–A1h: XOVER FINE

FACTORY DEFAULT	FFFFh
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

A0h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
A1h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	0
	BIT 7							BIT 0

Defines the crossover value for RSSI measurements of nonlinear inputs when XOVEREN is set to a 1 (Table 02h, Register 8Bh). MON3 fine conversion results (before right-shifting) greater than this register require a MON3 coarse conversion.

Table 02h, Register A2h–A3h: V_{CC} OFFSET
Table 02h, Register A4h–A5h: MON1 OFFSET
Table 02h, Register A6h–A7h: MON2 OFFSET
Table 02h, Register A8h–A9h: MON3 FINE OFFSET
Table 02h, Register AAh–ABh: MON4 OFFSET
Table 02h, Register ACh–ADh: MON3 COARSE OFFSET

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
A2h, A4h, A6h, A8h, AAh, ACh	S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}
A3h, A5h, A7h, A9h, ABh, ADh	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}

Allows for offset control of these voltage measurements if desired. This number is two's complement.

Table 02h, Register AEh–AFh: INTERNAL TEMP OFFSET

FACTORY CALIBRATED	
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

	BIT 7							BIT 0
AEh	S	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}
AFh	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}

Allows for offset control of temperature measurement if desired. The final result must be XORed with BB40h before writing to this register. Factory calibration contains the desired value for a reading in degrees Celsius.

Table 02h, Register B0h–B3h: PW1

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2 or (PW1 and WPW1)
MEMORY TYPE	Nonvolatile (SEE)

B0h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B1h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B2h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
B3h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW1 access. At power-on, the PWE value is set to all ones. Thus, writing these bytes to all ones grants PW1 access on power-on without writing the password entry. All reads of this register are 00h.

Table 02h, Register B4h–B7h: PW2

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

B4h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B5h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B6h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
B7h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW2 access. At power-on, the PWE value is set to all ones. Thus, writing these bytes to all ones grants PW2 access on power-on without writing the password entry. All reads of this register are 00h.

Table 02h, Register B8h: LOS RANGING

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

B8h	RESERVED	$HLOS_2$	$HLOS_1$	$HLOS_0$	RESERVED	$LLOS_2$	$LLOS_21$	$LLOS_0$
	BIT 7							BIT 0

This register controls the full-scale range of the quick-trip monitoring for the differential input's of MON3.

<table>
<tr><td>BIT 7</td><td>RESERVED (Default = 0)</td></tr>
<tr><td>BITS 6:4</td><td>HLOS[2:0]: HLOS Full-Scale Ranging. 3-bit value to select the FS comparison voltage for high LOS found on MON3. Default is 000b and creates an FS of 1.25V.
<table>
<tr><th>HLOS[2:0]</th><th>% of 1.25V</th><th>FS Voltage</th></tr>
<tr><td>000b</td><td>100.00</td><td>1.250</td></tr>
<tr><td>001b</td><td>80.00</td><td>1.000</td></tr>
<tr><td>010b</td><td>66.67</td><td>0.833</td></tr>
<tr><td>011b</td><td>50.00</td><td>0.625</td></tr>
<tr><td>100b</td><td>40.00</td><td>0.500</td></tr>
<tr><td>101b</td><td>33.33</td><td>0.417</td></tr>
<tr><td>110b</td><td>28.57</td><td>0.357</td></tr>
<tr><td>111b</td><td>25.00</td><td>0.313</td></tr>
</table></td></tr>
<tr><td>BIT 3</td><td>RESERVED (Default = 0)</td></tr>
<tr><td>BITS 2:0</td><td>LLOS[2:0]: LLOS Full-Scale Ranging. 3-bit value to select the FS comparison voltage for low LOS found on MON3. Default is 000b and creates an FS of 1.25V.
<table>
<tr><th>LLOS[2:0]</th><th>% of 1.25V</th><th>FS Voltage</th></tr>
<tr><td>000b</td><td>100.00</td><td>1.250</td></tr>
<tr><td>001b</td><td>80.00</td><td>1.000</td></tr>
<tr><td>010b</td><td>66.67</td><td>0.833</td></tr>
<tr><td>011b</td><td>50.00</td><td>0.625</td></tr>
<tr><td>100b</td><td>40.00</td><td>0.500</td></tr>
<tr><td>101b</td><td>33.33</td><td>0.417</td></tr>
<tr><td>110b</td><td>28.57</td><td>0.357</td></tr>
<tr><td>111b</td><td>25.00</td><td>0.313</td></tr>
</table></td></tr>
</table>

SFP+ Controller with Analog LDD Interface

Table 02h, Register B9h: COMP RANGING

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

B9h	RESERVED	$HBIAS_2$	$HBIAS_1$	$HBIAS_0$	RESERVED	APC_2	APC_1	APC_0
	BIT 7							BIT 0

The upper nibble of this byte controls the full-scale range of the quick-trip monitoring for BIAS. The lower nibble of this byte controls the full-scale range for the quick-trip monitoring of the APC reference as well as the closed-loop monitoring of APC.

<table>
<tr><td>BIT 7</td><td>RESERVED (Default = 0)</td></tr>
<tr><td>BITS 6:4</td><td>HBIAS[2:0]: HBIAS Full-Scale Ranging. 3-bit value to select the FS comparison voltage for BIAS found on MON1. Default is 000b and creates an FS of 1.25V.
<table>
<tr><th>BIAS[2:0]</th><th>% of 1.25V</th><th>FS Voltage</th></tr>
<tr><td>000b</td><td>100.00</td><td>1.250</td></tr>
<tr><td>001b</td><td>80.00</td><td>1.000</td></tr>
<tr><td>010b</td><td>66.67</td><td>0.833</td></tr>
<tr><td>011b</td><td>50.00</td><td>0.625</td></tr>
<tr><td>100b</td><td>40.00</td><td>0.500</td></tr>
<tr><td>101b</td><td>33.33</td><td>0.417</td></tr>
<tr><td>110b</td><td>28.57</td><td>0.357</td></tr>
<tr><td>111b</td><td>25.00</td><td>0.313</td></tr>
</table></td></tr>
<tr><td>BIT 3</td><td>RESERVED (Default = 0)</td></tr>
<tr><td>BITS 2:0</td><td>APC[2:0]: APC Full-Scale Ranging. 3-bit value to select the FS comparison voltage for MON2 with the APC. Default is 000b and creates an FS of 2.5V.
<table>
<tr><th>APC[2:0]</th><th>% of 2.50V</th><th>FS Voltage</th></tr>
<tr><td>000b</td><td>100.00</td><td>2.500</td></tr>
<tr><td>001b</td><td>80.00</td><td>2.000</td></tr>
<tr><td>010b</td><td>66.67</td><td>1.667</td></tr>
<tr><td>011b</td><td>50.00</td><td>1.250</td></tr>
<tr><td>100b</td><td>40.00</td><td>1.000</td></tr>
<tr><td>101b</td><td>33.33</td><td>0.833</td></tr>
<tr><td>110b</td><td>28.57</td><td>0.714</td></tr>
<tr><td>111b</td><td>25.00</td><td>0.625</td></tr>
</table></td></tr>
</table>

Table 02h, Register BAh: IBIASMAX

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

BAh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

This value defines the maximum DAC value allowed for the upper 8 bits of BIAS output during APC closed-loop operations. During the intial step and binary search, this value does not cause an alarm, but does still clamp the BIAS DAC value. After the startup sequence (or normal APC operations), if the APC loop tries to create a BIAS value greater than this setting, it is clamped and creates a MAX BIAS alarm.

Table 02h, Register BBh: ISTEP

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

BBh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

The initial step value used at power-on or after a TXD pulse to control the BIAS DAC. At startup, this value plus $2^0 = 1$ is continuously added to the BIAS DAC value until the APC feedback (MON2) is greater than its threshold. At that time, a binary search is used to complete the startup of the APC closed loop. If the resulting math operation is greater than IBIASMAX (Table 02h, Register BAh), the result is not loaded into the BIAS DAC, but the binary search is begun to complete the initial search for APC. During startup, the BIAS DAC steps causing a higher bias value than IBIASMAX do not create the BIAS MAX alarm. The BIAS MAX alarm detection is enabled at the end of the binary search.

Table 02h, Register BCh: HTXP

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
BCh	BIT 7							BIT 0

Fast-comparison DAC threshold adjust for high TXP. This value is added to the APC DAC value recalled from Table 04h. If the sum is greater than 0xFF, 0xFF is used. Comparisons greater than V_{HTXP}, compared against V_{MON2}, create a TXP HI alarm. The same ranging applied to the APC DAC should be used here.

$$V_{HTXP} = \frac{\text{Full Scale}}{255} \times (\text{HTXP} + \text{APC DAC})$$

Table 02h, Register BDh: LTXP

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
BDh	BIT 7							BIT 0

Fast-comparison DAC threshold adjust for low TXP. This value is subtracted from the APC DAC value recalled from Table 04h. If the difference is less than 0x00, 0x00 is used. Comparisons less than V_{LTXP}, compared against V_{MON2}, create a TXP LO alarm. The same ranging applied to the APC DAC should be used here.

$$V_{LTXP} = \frac{\text{Full Scale}}{255} \times (\text{APC DAC} - \text{LTXP})$$

Table 02h, Register BEh: HLOS

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

BEh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast-comparison DAC threshold adjust for high LOS. The combination of HLOS and LLOS creates a hysteresis comparator. As RSSI falls below the LLOS threshold, the LOS LO alarm bit is set to 1. The LOS alarm remains set until the RSSI input is found above the HLOS threshold setting, which clears the LOS LO alarm bit and sets the LOS HI alarm bit. At power-on, both LOS LO and LOS HI alarm bits are 0 and the hysteresis comparator uses the LLOS threshold setting.

Table 02h, Register BFh: LLOS

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

BFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast-comparison DAC threshold adjust for low LOS. See HLOS (Table 02h, Register BEh) for functional description.

Table 02h, Register C0h: PW_ENA

FACTORY DEFAULT	10h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

C0h	RWTBL78	RWTBL1C	RWTBL2	RWTBL1A	RWTBL1B	WLOWER	WAUXA	WAUXB
	BIT 7							BIT 0

BIT 7	**RWTBL78:** Tables 07h–08h 0 = (Default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 6	**RWTBL1C:** Table 01h or 05h bytes F8h–FFh. Table address is dependent on MASK bit (Table 02h, Register 89h). 0 = (Default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 5	**RWTBL2:** Tables 02h. Writing a nonvolatile value to this bit requires PW2 access. 0 = (Default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 4	**RWTBL1A:** Table 01h, Registers 80h–BFh 0 = Read and write access for PW2 only. 1 = (Default) Read and write access for both PW1 and PW2.
BIT 3	**RWTBL1B:** Table 01h, Registers C0h–F7h 0 = (Default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 2	**WLOWER:** Bytes 00h–5Fh in main memory. All users can read this area. 0 = (Default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.
BIT 1	**WAUXA:** Auxiliary Memory, Registers 00h–7Fh. All users can read this area. 0 = (Default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.
BIT 0	**WAUXB:** Auxiliary Memory, Registers 80h–FFh. All users can read this area. 0 = (Default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.

Table 02h, Register C1h: PW_ENB

FACTORY DEFAULT	03h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

C1h	RWTBL46	RTBL1C	RTBL2	RTBL1A	RTBL1B	WPW1	WAUXAU	WAUXBU
	BIT 7							BIT 0

BIT 7	**RWTBL46:** Tables 04h and 06h 0 = (Default) Read and write access for PW2 only. 1 = Read and write access for PW1.
BIT 6	**RTBL1C:** Table 01h or Table 05h, Registers F8h–FFh. Table address is dependent on MASK bit (Table 02h, Register 89h). 0 = (Default) Read and write access for PW2 only. 1 = Read access for PW1.
BIT 5	**RTBL2:** Table 02h 0 = (Default) Read and write access for PW2 only. 1 = Read access for PW1.
BIT 4	**RTBL1A:** Table 01h, Registers 80h–BFh 0 = (Default) Read and write access for PW2 only. 1 = Read access for PW1.
BIT 3	**RTBL1B:** Table 01h, Registers C0h–F7h 0 = (Default) Read and write access for PW2 only. 1 = Read access for PW1.
BIT 2	**WPW1:** Register PW1 (Table 02h, Registers B0h–B3h). For security purposes these registers are not readable. 0 = (Default) Write access for PW2 only. 1 = Write access for PW1.
BIT 1	**WAUXAU:** Auxiliary Memory, Registers 00h–7Fh. All users can read this area. 0 = Write access for PW2 only. 1 = (Default) Write access for user, PW1 and PW2.
BIT 0	**WAUXBU:** Auxiliary Memory, Registers 80h–FFh. All users can read this area. 0 = Write access for PW2 only. 1 = (Default) Write access for user, PW1 and PW2.

Table 02h, Register C2h–C5h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

These registers are reserved.

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Table 02h, Register C6h: POLARITY

FACTORY DEFAULT	0Ch
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

C6h	RESERVED	RESERVED	RESERVED	RESERVED	MODP	BIASP	DAC1P	DAC2P
	BIT 7							BIT 0

BITS 7:4	**RESERVED**
BIT 3	**MODP:** MOD DAC Polarity. The MOD DAC (Table 02h, Registers 82h–83h) range is 000h–3FFh. A setting of 000h creates a pulse density of zero and 3FFh creates a pulse density of 1023/1024. This polarity bit allows the user to use GND or V_{REFIN} as the reference. The power-on of MOD DAC is 000h, thus an application that needs V_{REFIN} to be in off state should use the inverted polarity. 0 = Normal polarity. A setting of 000h results in a pulse-density output of zero held at GND and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at V_{REFIN}. 1 = Inverted polarity. A setting of 000h results in a pulse-density output of zero held at V_{REFIN} and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at GND.
BIT 2	**BIASP:** BIAS DAC Polarity. The BIAS DAC (Table 02h, Registers CA–CBh) range is 000h–3FFh. A setting of 000h creates a pulse density of zero and 3FFh creates a pulse density of 1023/1024. This polarity bit allows the user to use GND or V_{REFIN} as the reference. The power-on of BIAS DAC is 000h, thus an application that needs V_{REFIN} to be the off state should use the inverted polarity. 0 = Normal polarity. A setting of 000h results in a pulse-density output of zero held at GND and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at V_{REFIN}. 1 = Inverted polarity. A setting of 000h results in a pulse-density output of zero held at V_{REFIN} and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at GND.
BIT 1	**DAC1P:** DAC1 VALUE Polarity. The DAC1 VALUE (Table 02h, Registers 84h–85h) range is 000h–3FFh. A setting of 000h creates a pulse density of zero and 3FFh creates a pulse density of 1023/1024. This polarity bit allows the user to use GND or V_{REFIN} as the reference. The power-on of DAC1 VALUE is 000h, thus an application that needs V_{REFIN} to be the off state should use the inverted polarity. 0 = Normal polarity. A setting of 000h results in a pulse-density output of zero held at GND and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at V_{REFIN}. 1 = Inverted polarity. A setting of 000h results in a pulse-density output of zero held at V_{REFIN} and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at GND.
BIT 0	**DAC2P:** DAC2 VALUE Polarity. The DAC2 VALUE (Table 02h, Registers 86h–87h) range is 000h–3FFh. A setting of 000h creates a pulse-density of zero and 3FFh creates a pulse density of 1023/1024. This polarity bit allows the user to use GND or V_{REFIN} as the reference. The power-on of DAC2 VALUE is 000h, thus an application that needs V_{REFIN} to be the off state should use the inverted polarity. 0 = Normal polarity. A setting of 000h results in a pulse-density output of zero held at GND and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at V_{REFIN}. 1 = Inverted polarity. A setting of 000h results in a pulse-density output of zero held at V_{REFIN} and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at GND.

Table 02h, Register C7h: TBLSELPON

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
MEMORY TYPE	Nonvolatile (SEE)

C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Chooses the initial value for the table-select byte (Lower Memory, Register 7Fh) at power-on.

Table 02h, Register C8h–C9h: MAN BIAS

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and BIAS EN = 0) or (PW1 and RWTBL2 and BIAS EN = 0)
MEMORY TYPE	Volatile

C8h	0	0	0	0	0	0	0	2^8
C9h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

When BIAS EN (Table 02h, Register 80h) is written to 0, writes to these bytes control the BIAS DAC.

Table 02h, Register CAh: MAN_CNTL

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and BIAS EN = 0) or (PW1 and RWTBL2 and BIAS EN = 0)
MEMORY TYPE	Volatile

CAh	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MAN_CLK
	BIT 7							BIT 0

When BIAS EN (Table 02h, Register 80h) is written to 0, MAN_CLK controls the updates of the MAN BIAS value to the BIAS DAC. The values of MAN BIAS must be written with a separate write command. Setting MAN_CLK to a 1 clocks the MAN BIAS value to the BIAS DAC.
1) Write the MAN BIAS value with a write command.
2) Set the MAN_CLK bit to a 1 with a separate write command.
3) Clear the MAN_CLK bit to a 0 with a separate write command.

Table 02h, Register CBh–CCh: BIAS DAC

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	N/A
MEMORY TYPE	Volatile

CBh	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	2^9	2^8
CCh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for BIAS and resolved from the APC. This register is updated after each decision of the APC loop.

Table 02h, Register CDh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	N/A
MEMORY TYPE	N/A

This register is reserved.

Table 02h, Register CEh: DEVICE ID

FACTORY DEFAULT	73h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	N/A
MEMORY TYPE	ROM

CEh	0	1	1	1	0	0	1	1
	BIT 7							BIT 0

Hardwired connections to show the device ID.

Table 02h, Register CFh: DEVICE VER

FACTORY DEFAULT	DEVICE VERSION
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	N/A
MEMORY TYPE	ROM

CFh	DEVICE VERSION	
	BIT 7	BIT 0

Hardwired connections to show the device version.

Table 02h, Register D0h: APC DAC

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and ACPEN = 0) or (PW1 and RWTBL2 and APC EN = 0)
MEMORY TYPE	Volatile

D0h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for APC reference and recalled from Table 06h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

Table 02h, Register D1h: HBIAS DAC

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and APC EN = 0) or (PW1 & RWTBL2 and APC EN = 0)
MEMORY TYPE	Volatile

D1h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for HBIAS reference and recalled from Table 06h at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

Table 02, Register D2h–D7h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	N/A
MEMORY TYPE	N/A

These registers are reserved.

Table 02h, Register D8h–F7h: EMPTY

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
MEMORY TYPE	None

These registers do not exist.

Table 04h, Register 80h–C7h: MODULATION LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL46) or (PW1 and RTBL46)
WRITE ACCESS	PW2 or (PW1 and RWTBL46)
MEMORY TYPE	Nonvolatile (EE)

80h–C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value for the modulation DAC output.

The MODULATION LUT is a set of registers assigned to hold the temperature profile for the MOD DAC. The values in this table determine the set point for the modulation voltage. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 2°C increments from -40°C to +102°C, starting at 80h in Table 04h. Register 80h defines the -40°C to -38°C MOD output, Register 81h defines the -38°C to -36°C MOD output, and so on. Values recalled from this EEPROM memory table are written into the MOD DAC (Table 02h, Register 82h–83h) location that holds the value until the next temperature conversion. The DS1873 can be placed into a manual mode (MOD EN bit, Table 02h, Register 80h), where the MOD DAC is directly controlled for calibration. If the temperature compensation functionality is not required, then program the entire Table 04h to the desired modulation setting.

Table 04h, Register F8h–FFh: MOD OFFSET LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL46) or (PW1 and RTBL46)
WRITE ACCESS	PW2 or (PW1 and RWTBL46)
MEMORY TYPE	Nonvolatile (EE)

F8h–FFh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

The digital value for the temperature offset of the MOD DAC output.

F8h	Less than or equal to -8°C
F9h	Greater than -8°C up to +8°C
FAh	Greater than +8°C up to +24°C
FBh	Greater than +24°C up to +40°C
FCh	Greater than +40°C up to +56°C
FDh	Greater than +56°C up to +72°C
FEh	Greater than +72°C up to +88°C
FFh	Greater than +88°C

The MOD DAC is a 10-bit register. The MODULATION LUT is an 8-bit LUT. The MOD OFFSET LUT times 4 plus the MODULATION LUT makes use of the entire 10-bit range.

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Table 06h Register Descriptions

Table 06h, Register 80h–A3h: APC TE LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL46) or (PW1 and RTBL46)
WRITE ACCESS	PW2 or (PW1 and RWTBL46)
MEMORY TYPE	Nonvolatile (EE)

80h–A3h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The APC TE LUT is a set of registers assigned to hold the temperature profile for the APC reference DAC. The values in this table combined with the APC bits in the COMP RANGING register (Table 02h, Register B9h) determine the set point for the APC loop. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 4°C increments from -40°C to +100°C, starting at Register 80h in Table 05h. Register 80h defines the -40°C to -36°C APC reference value, Register 81h defines the -36°C to -32°C APC reference value, and so on. Values recalled from this EEPROM memory table are written into the APC DAC (Table 02h, Register CDh) location that holds the value until the next temperature conversion. The DS1873 can be placed into a manual mode (APC EN bit, Table 02h, Register 80h), where APC DAC can be directly controlled for calibration. If TE temperature compensation is not required by the application, program the entire LUT to the desired APC set point.

Table 06h, Register A4h–A7h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL46) or (PW1 and RTBL46)
WRITE ACCESS	PW2 or (PW1 and RWTBL46)
MEMORY TYPE	Nonvolatile (EE)

These registers are reserved.

Table 06h, Register F8h–FFh: HBIAS LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL46) or (PW1 and RTBL46)
WRITE ACCESS	PW2 or (PW1 and RWTBL46)
MEMORY TYPE	Nonvolatile (EE)

F8h–FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

High bias alarm threshold (HBATH) is a digital clamp used to ensure that the DAC setting for BIAS currents does not exceed a set value. The table below shows the range of temp for each byte's location. The table shows a rising temperature; for a falling temperature there is 1°C of hysteresis.

F8h	Less than or equal to -8°C
F9h	Greater than -8°C up to +8°C
FAh	Greater than +8°C up to +24°C
FBh	Greater than +24°C up to +40°C
FCh	Greater than +40°C up to +56°C
FDh	Greater than +56°C up to +72°C
FEh	Greater than +72°C up to +88°C
FFh	Greater than +88°C

Table 07h Register Descriptions

Table 07h, Register 80h–C7h: DAC1 LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) and (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

80h–C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The DAC1 LUT is a set of registers assigned to hold the PWM profile for DAC1. The values in this table determine the set point for DAC1. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 2°C increments from -40°C to +102°C, starting at Register 80h in Table 07h. Register 80h defines the -40°C to -38°C DAC1 value, Register 81h defines -38°C to -36°C DAC1 value, and so on. Values recalled from this EEPROM memory table are written into the DAC1 VALUE (Table 02h, Registers 84h–85h) location, which holds the value until the next temperature conversion. The part can be placed into a manual mode (DAC1 EN bit, Table 02h, Register 80h), where DAC1 can be directly controlled for calibration. If temperature compensation is not required by the application, program the entire LUT to the desired DAC1 set point.

Table 07h, Register C8h–F7h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) or (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

These registers are reserved.

Table 07h, Register F8h–FFh: DAC1 OFFSET LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) or (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

F8h–FFh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

The digital value for the temperature offset of the DAC1 output.

F8h	Less than or equal to -8°C
F9h	Greater than -8°C up to +8°C
FAh	Greater than +8°C up to +24°C
FBh	Greater than +24°C up to +40°C
FCh	Greater than +40°C up to +56°C
FDh	Greater than +56°C up to +72°C
FEh	Greater than +72°C up to +88°C
FFh	Greater than +88°C

The DAC1 VALUE is a 10-bit register. The DAC1 LUT is an 8-bit LUT. The DAC1 OFFSET LUT times 4 plus the MODULATION LUT makes use of the entire 10-bit range.

Table 08h, Register 80h–A3h: DAC2 LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) or (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

80h–A3h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The DAC2 LUT is set of registers assigned to hold the PWM profile for DAC2. The values in this table determine the set point for DAC2. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 4°C increments from -40°C to +100°C, starting at Register 80h in Table 07h. Register 80h defines the -40°C to -36°C DAC2 value, Register 81h defines -36°C to -32°C DAC2 value, and so on. Values recalled from this EEPROM memory table are written into the DAC2 VALUE (Table 02h, Registers 86h–87h) location that holds the value until the next temperature conversion. The DS1873 can be placed into a manual mode (DAC2 EN bit, Table 02h, Register 80h), where DAC2 can be directly controlled for calibration. If temperature compensation is not required by the application, program the entire LUT to the desired DAC2 set point.

Table 08h, Register A4h–A7h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) or (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

These registers are reserved.

Table 08h, Register F8h–FFh: DAC2 OFFSET LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL78) or (PW1 and RTBL78)
WRITE ACCESS	PW2 or (PW1 and RWTBL78)
MEMORY TYPE	Nonvolatile (EE)

F8h–FFh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

The digital value for the temperature offset of the DAC2 output.

F8h	Less than or equal to -8°C
F9h	Greater than -8°C up to +8°C
FAh	Greater than +8°C up to +24°C
FBh	Greater than +24°C up to +40°C
FCh	Greater than +40°C up to +56°C
FDh	Greater than +56°C up to +72°C
FEh	Greater than +72°C up to +88°C
FFh	Greater than +88°C

The DAC2 VALUE is a 10-bit register. The DAC2 LUT is an 8-bit LUT. The DAC2 OFFSET LUT times 4 plus the MODULATION LUT makes use of the entire 10-bit range.

Auxiliary Memory A0h Register Descriptions

Auxiliary Memory A0h, Register 00h–7Fh: EEPROM

FACTORY DEFAULT	00h
READ ACCESS	ALL
WRITE ACCESS	PW2 or (PW1 and WAUXA) or (WAUXAU)
MEMORY TYPE	Nonvolatile (EE)

00h–7Fh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Accessible with the slave address A0h.

Auxiliary Memory A0h, Register 80h–FFh: EEPROM

FACTORY DEFAULT	00h
READ ACCESS	ALL
WRITE ACCESS	PW2 or (PW1 and RWAUXB) or (RWAUXBU)
MEMORY TYPE	Nonvolatile (EE)

80h–FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Accessible with the slave address A0h.

Applications Information

Power-Supply Decoupling

To achieve best results, it is recommended that the power supply is decoupled with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins to minimize lead inductance.

SDA and SCL Pullup Resistors

SDA is an open-collector output on the DS1873 that requires a pullup resistor to realize high logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be utilized for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I^2C AC Electrical Characteristics* table are within specification.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2855+6	21-0140

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/09	Initial release.	—
1	11/09	Changed the default state for the TXDIO bit in Table 02h, Register 8Bh: CNFGC.	60
		Corrected the factory default value for Table 02h, Register C6h: POLARITY from 00h to 0Ch.	74