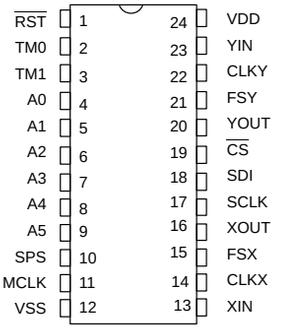
DALLAS SEMICONDUCTOR

DS2167/DS2168
ADPCM Processor

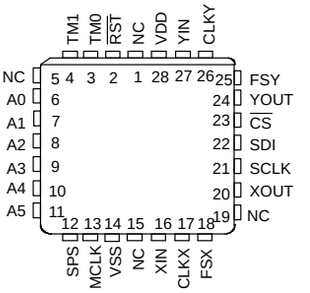
FEATURES

- Speech compression chip compatible with standard ADPCM algorithms:
  - DS2167 supports “new” T1Y1 recommendations (July 1986) and “new” CCITT G.721 recommendations
  - DS2168 supports “old” CCITT G.721 recommendations
- Dual independent channel architecture – device may be programmed to perform full duplex, 2-channel expansions, or 2-channel compressions
- Interconnects directly with μ-law or A-law codec/filter devices
- Serial PCM and control port interfaces minimize “glue logic” in multiple channel applications
  - On-chip channel counters identify input and output timeslots in TDM-based systems
  - Unique addressing scheme simplifies device control; 3-wire port shared among 64 devices
  - Bypass and idle features allow dynamic allocation of channel bandwidth, minimize system power requirements
- Hardware mode intended for stand-alone use
  - No host processor required
  - Ideal for voice mail applications
- 28-pin surface-mount package available, designated DS2167Q/DS2168Q

PIN ASSIGNMENT



24-Pin DIP (600 MIL)



28-Pin PLCC

DESCRIPTION

The DS2167 and DS2168 are dedicated digital signal processor (DSP) CMOS chips optimized for Adaptive Differential Pulse Code Modulation (ADPCM) based compression algorithms. The devices halve the transmission bandwidth of “toll quality” voice from 64K to 32K bits/second and are utilized in PCM-based telephony networks.

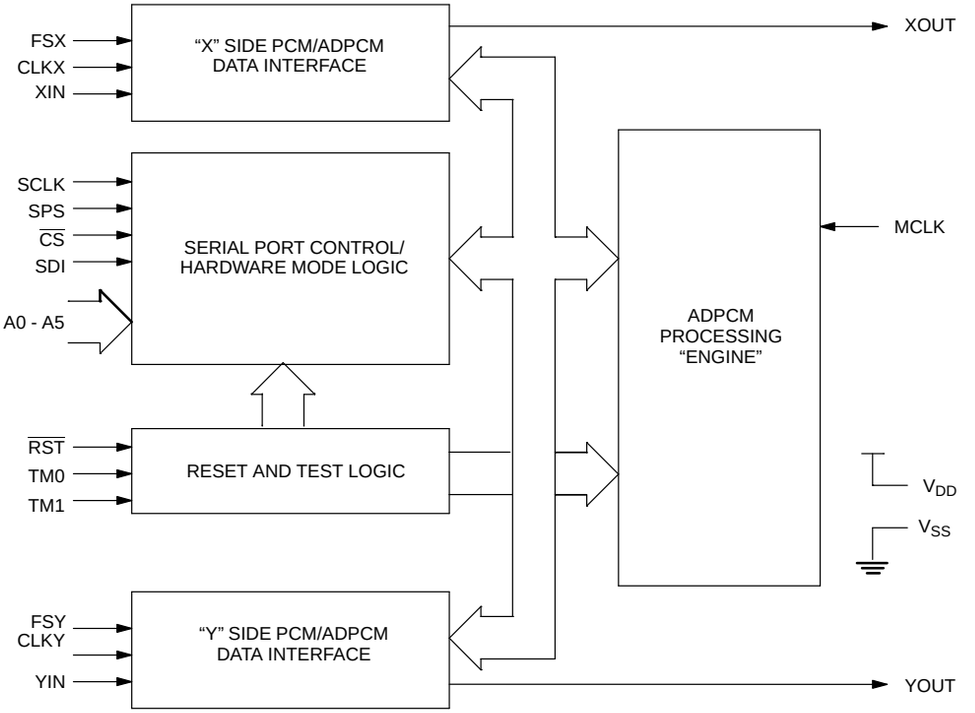
PRODUCT OVERVIEW

The DS2167 and DS2168 contain three major functional blocks: a high performance (10 MIPS) DSP “engine,” two independent PCM data interfaces (“X” and “Y”) which connect directly to serial time division multiplexed (TDM) backplanes and a microcontroller-compatible serial port for on-the-fly device configuration. A 10MHz master clock is required by the DSP engine. The devices’ dual channel architecture supports full duplex, dual compression or dual expansion operation. The PCM data interfaces support 1.544, 2.048 and 4.096 MHz data rates. Each device samples the serial PCM or ADPCM bit stream during a user-programmed input timeslot, processes the data and outputs the result during a user-programmed output timeslot.

Each PCM interface has a control register which specifies functional characteristics (compress, expand, bypass and idle), data format (μ-law or A-law) and algorithm reset control. With the SPS pin strapped high, the software mode is enabled and the serial port is used to program control and timeslot registers. In this mode, a novel addressing scheme allows multiple devices to share a common 3-wire control bus, simplifying system level interconnect.

With SPS low, the hardware mode is enabled. This mode disables the serial port and maps appropriate control register bits to address and port inputs. Under hardware mode, no host controller is required and all PCM I/O defaults to timeslot 0. This stand-alone mode is compatible with popular codecs.

DS2168 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
1	RST	I	**Reset.** A high-low-high transition clears all internal registers and reset both algorithms. The device should be reset on system power-up, and/or when changing to/from hardware mode.
2 3	TM0 TM1	I	**Test Modes 0 and 1.** Tie to V_{SS} for normal operation
4 5 6 7 8 9	A0 A1 A2 A3 A4 A5	I	**Address Select.** A0=LSB; A5=MSB. Must match address/command word to enable serial port write.
10	SPS	I	**Serial Port Select.** Tie to V_{DD} to select the serial port, to V_{SS} to select the hardware mode.
11	MCLK	I	**Master Clock.** 10 MHz clock for ADPCM processing “engine”; may asynchronous to SCLK, CLKX and CLKY.
12	VSS	–	**Signal Ground.** 0.0 volts
13	XIN	I	**X Data In.** Samples on falling edge of CLKX during selected timeslots.
14	CLKX	I	**X Data Clock.** Data clock for X side PCM interface; must be coherent and rising edge aligned with FSX.
15	FSX	I	**X Frame Sync.** 8 KHz frame sync for X side PCM interface.
16	XOUT	O	**X Data Out.** Updated on rising edge of CLKX during selected timeslots.
17	SCLK	I	**Serial Data Clock.** Used to write serial port registers.
18	SDI	I	**Serial Data In.** Data for onboard control registers. Sampled on rising edge of SCLK.
19	CS	I	**Chip Select.** Must be low to write the serial port.
20	YOUT	O	**Y Data Out.** Updated on rising edge of CLKY during selected timeslots.
21	FSY	I	**Y Frame Sync.** 8 KHz frame sync for Y side PCM interface.
22	CLKY	I	**Y Data Clock.** Data clock for Y side PCM interface; must be coherent and rising edge aligned with FSY.
23	YIN	I	**Y Data In.** Samples on falling edge of CLKY during selected timeslots.
24	VDD	–	**Positive Supply.** 5.0 volts.

HARDWARE RESET

$\overline{RST}$ allows the user to reset both channel algorithms and register contents. This input must be held low for at least 1 ms on system power-up after master clock is stable to assure proper initialization of the device. $\overline{RST}$ should also be asserted when changing to/from the hardware mode. $\overline{RST}$ clears all bits of the control register except IPD; IPD is set for both channels, powering down the device.

HARDWARE MODE

The hardware mode is intended for preliminary system prototyping or for applications which do not require the features of the serial port. Tying SPS to VSS disables the serial port, clears all internal registers and maps IPD, μ/$\overline{A}$ and CP/$\overline{EX}$ of the X and Y side interfaces to the port and address inputs. Input and output timeslots for the X and Y side interfaces are fixed at 0. Such applications include, but are not limited to: 1) systems in which timeslot and algorithm are fixed, 2) stand-alone ADPCM combo applications, 3) "hardware" oriented systems where no host controller is available.

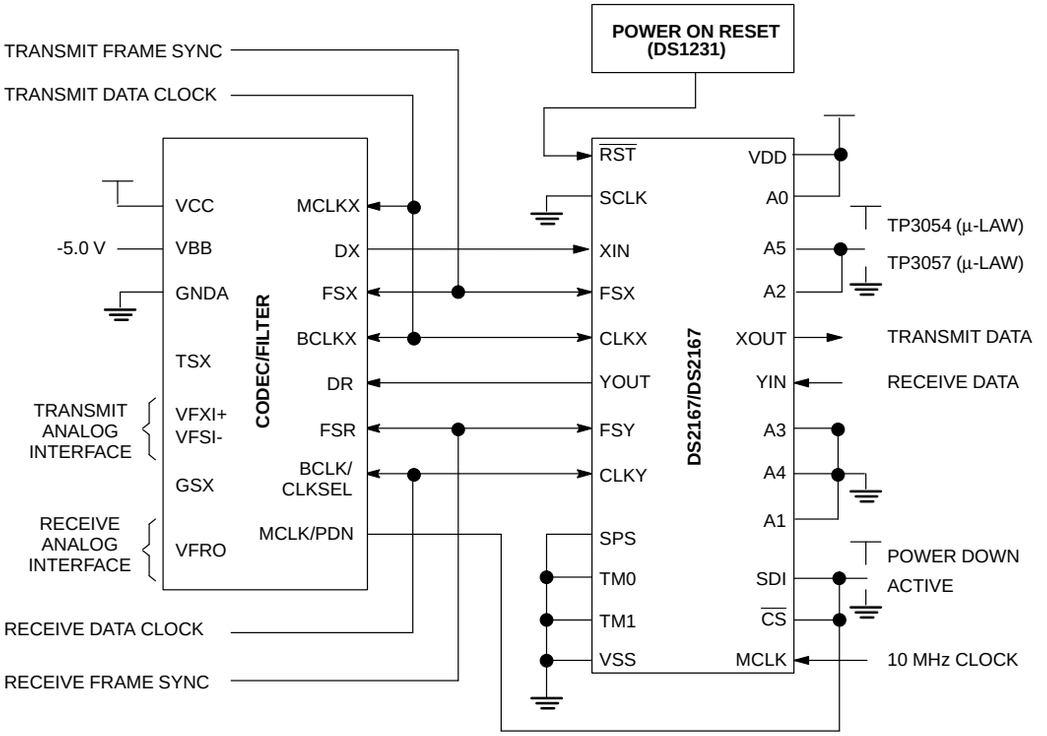
HARDWARE MODE Table 2

PIN #/NAME	REG. LOCATION	NAMES AND DESCRIPTION
4/A0	CP/$\overline{EX}$ (X)	**Channel X coding** 0 = Expand 1 = Compress
6/A2	μ/$\overline{A}$ (X)	**Channel X data format** 0 = A-law 1 = μ-law
7/A3	CP/$\overline{EX}$ (Y)	**Channel Y coding** 0 = Expand 1 = Compress
9/A5	μ/$\overline{A}$ (Y).2	**Channel Y data format** 0 = A-law 1 = μ-law
18/SDI	IPD (Y)	**Y idle select** 0 = Channel active 1 = Channel idle
19/$\overline{CS}$	IPD (X)	**X idle select** 0 = Channel active 1 = Channel idle

NOTES:

1. SCLK, A1 and A4 must be tied to VSS when the hardware mode is selected.
2. When both X and Y sides are idled, the devices enter a stand-by mode which significantly reduces power consumption.
3. The DS2167 will power-up within 200 ms after the X or Y side is reactivated (SDI and/or $\overline{CS}$ not equal to 0) from standby.
4. The DS2168 must be hardware reset when reactivated from standby. Power-up occurs immediately after the reset.

CODEC/FILTER HARDWARE MODE INTERCONNECT Figure 2



NOTE:
Suggested Codec/Filters

TP305X	National Semiconductor
ETC505X	SGS–Thomson Microelectronics
MC1455XX	Motorola
TCM29CXX	Texas Instruments
HD44238C	Hitachi

*other generic Codec/Filter devices can be substituted.

SOFTWARE MODE

Tying SPS high enabled the software mode. In this mode, a host microcontroller writes configuration data to the DS2167/DS2168 serial port via inputs SCLK, SDI, and $\overline{CS}$. Independent control and timeslot registers establish operating characteristics for the X-side and Y-side PCM interfaces.

ADDRESS/COMMAND BYTE

In the software mode, the address/command byte is the first byte written to the serial port; it identifies which of 64 possible ADPCM processors sharing the port wiring is to be updated. Address data must match that at inputs A0–A5. If no match occurs, the device ignores the following configuration data. If an address match occurs, the next three bytes written are accepted as control, input and output timeslot data. Bit ACB.6 determines which side (X or Y) of the device is to be updated.

CONTROL REGISTER

The control register establishes idle, algorithm reset, bypass, data format and channel coding for the selected PCM interface.

The X and Y side PCM interfaces may be independently disabled (output tri-stated) via IPD; when IPD is set for

both X and Y interfaces, the device enters a low-power standby mode. The DS2167 will power-up within 200 ms after the X or Y side is reactivated (IPD=0) from standby. The DS2168 requires an external hardware reset after IPD is cleared to “wake-up” from standby. The DS2168 will power-up immediately after the low-high transition on $\overline{RST}$.

ALRST resets the algorithm coefficients for the selected channel to their initial values. ALRST will be cleared by the device when the algorithm reset is complete.

The bypass feature is enabled when BYP is set and IPD is clear. During bypass, no expansion or compression of data occurs. This feature allows the user to interchange timeslots under control of the timeslot registers. Bypass operates on byte-wide slots when CP/$\overline{EX}$=1, on nibble-wide slots when CP/$\overline{EX}$=0.

A-law (μ/$\overline{A}$=0) or μ-law PCM (μ/$\overline{A}$=1) coding is independently selected for the X and Y side interfaces by bit μ/A. If BYP and IPD are clear, CP/$\overline{EX}$ determines if input data is to be compressed or expanded.

TIMESLOT ASSIGNMENT

On-chip counters establish when PCM data I/O occurs and are programmed via the timeslot registers. Timeslot size (4 or 8 bits wide) is determined by the state of CP/$\overline{EX}$. Timeslots are counted from the rising edge of FSX and FSY.

ADDRESS/COMMAND BYTE Figure 3

(MSB)							(LSB)
–	X/$\overline{Y}$	A5	A4	A3	A2	A1	a0

SYMBOL	POSITION	NAME AND DESCRIPTION
–	ACB.7	Reserved, must be 0 for proper operation.
X/$\overline{Y}$	ACB.6	**X/$\overline{Y}$ Channel Select.** 0 = Update channel Y characteristics. 1 = Update channel X characteristics.
A5	ACB.5	**MSB of Device Address.**
A4	ACB.4	
A3	ACB.3	
A2	ACB.2	
A1	ACB.1	
A0	ACB.0	**LSB of Device Address.**

CONTROL REGISTER Figure 4

(MSB)							(LSB)
–	–	IPD	ALRST	BYP	μ/$\overline{A}$	–	CP/$\overline{EX}$

SYMBOL	POSITION	NAME AND DESCRIPTION
–	CR.7	Reserved, must be 0 for proper operation.
–	CR.6	Reserved, must be 0 for proper operation.
IPD	CR.5	**Idle and Power Down.** 0 = channel enabled. 1 = channel disabled (output tri-stated).
ALRST	CR.4	**Algorithm Reset.** 0 = Normal operation. 1 = Reset algorithm for selected channel.
BYP	CR.3	**Bypass.** 0 = Normal operation. 1 = Bypass selected channel.
μ/$\overline{A}$	CR.2	**Data Format** 0 = A-law. 1 = μ-law.
–	CR.1	Reserved, must be 0 for proper operation.
CP/$\overline{EX}$	CR.0	**Channel Coding.** 0 = Expand (decode) selected channel. 1 = Compress (encode) selected channel.

INPUT TIMESLOT REGISTER Figure 5

(MSB)							(LSB)
–	–	D5	D4	D3	D2	D1	D0

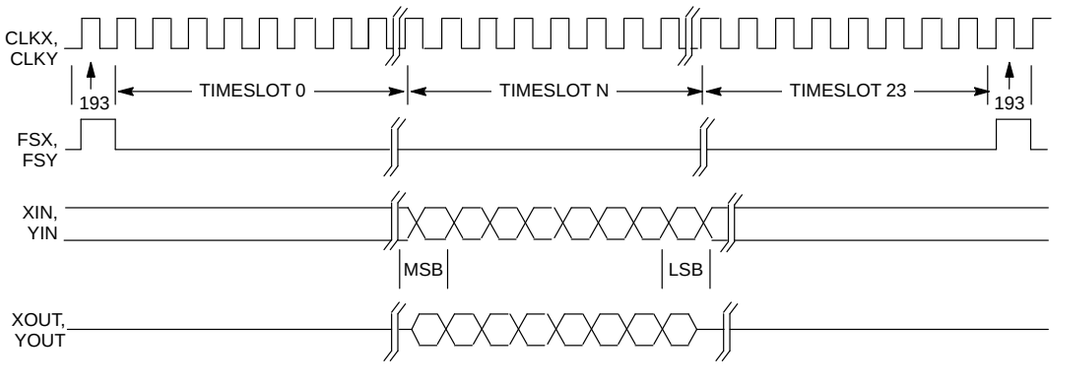
SYMBOL	POSITION	NAME AND DESCRIPTION
–	ITR.7	Reserved, must be 0 for proper operation.
–	ITR.6	Reserved, must be 0 for proper operation.
D5	ITR.5	MSB of input timeslot word.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input timeslot word.

OUTPUT TIMESLOT REGISTER Figure 6

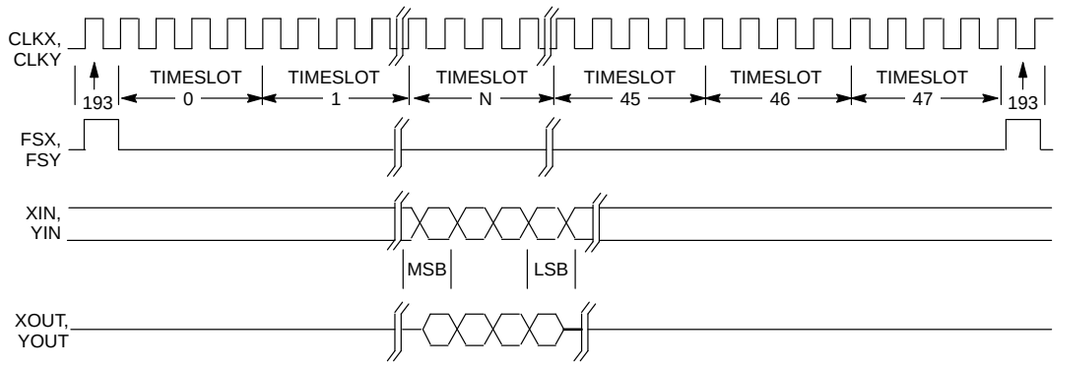
(MSB)							(LSB)
–	–	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
–	OTR.7	Reserved, must be 0 for proper operation.
–	OTR.6	Reserved, must be 0 for proper operation.
D5	OTR.5	MSB of output timeslot word.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output timeslot word.

PCM I/O TIMING (1.544 MHz BACKPLANE) Figure 7



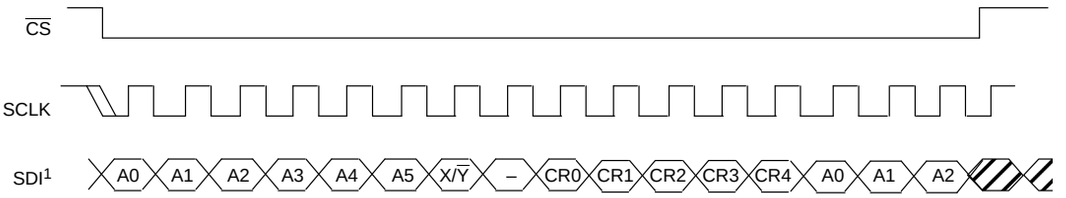
ADPCM I/O TIMING (1.544 MHz BACKPLANE) Figure 8



SERIAL PORT WRITE

All port writes are initiated by driving $\overline{CS}$ low and terminated when $\overline{CS}$ returns high. *Data is sampled on the rising edge of SCLK and must be written to the device LSB first.* Writes to the device may be two bytes (address/command and control) or four bytes (address/command, control, input timeslot and output timeslot) in length. Writes should be terminated on byte boundaries to insure data integrity. PCM and ADPCM outputs will tristate during register updates.

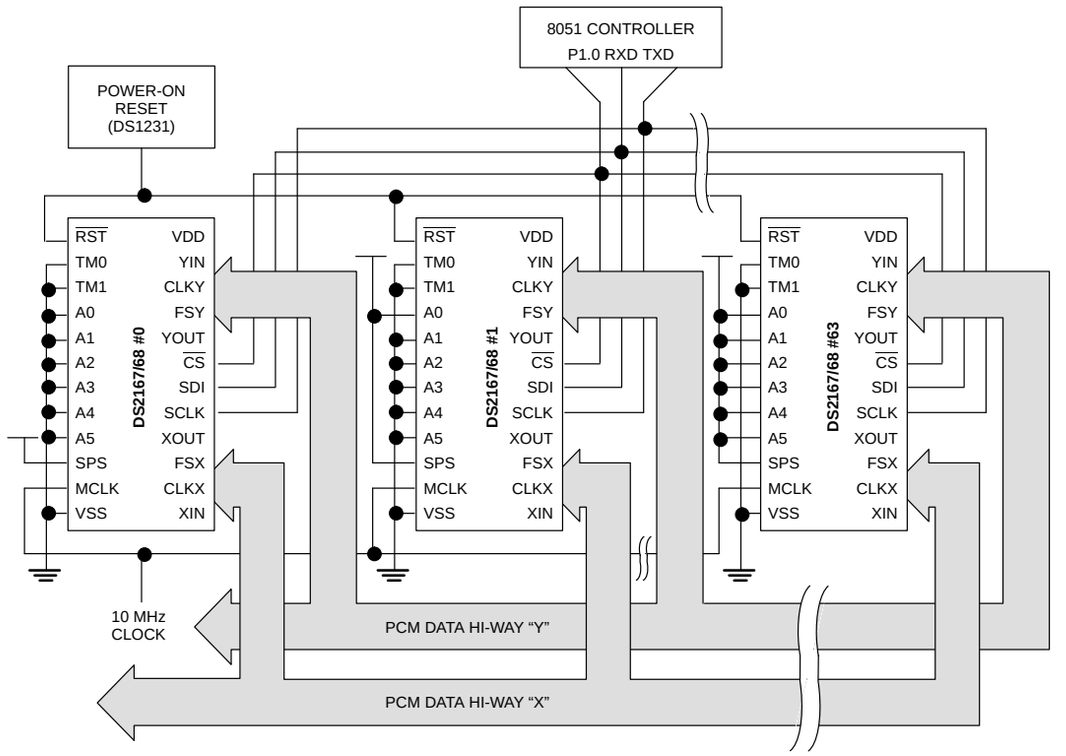
SERIAL PORT WRITE Figure 9



NOTE:

1. 2-byte write shown.

8051-BASED CONTROL SYSTEM Figure 10



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to 7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to 125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC} +0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.5		5.5	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{DD} = 5V $\pm$ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current (Active)	I_{DDA}		30		mA	1,2
Supply Current (Idle)	I_{DDPD}		1		mA	1,2,3
Input Leakage	I_{IL}	-1.0		+1.0	µA	
Output Leakage	I_{TRI}	-1.0		+1.0	µA	4
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	4.0			mA	

NOTES:

1. CLKX = CLKY = 1.544 MHz; MCLK = 10 MHz.
2. Outputs open; inputs swinging full supply levels.
3. Both channels in idle mode.
4. XOUT and YOUT when tri-stated.

PCM INTERFACE
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	5
MCLK Pulse Width	t_{WMH}, t_{WML}	45	50	55	ns	
MCLK Rise and Fall Times	t_{RM}, t_{FM}		5	10	ns	
CLKX, CLKY Period	t_{PXY}	244	488	5208	ns	4
CLKX, CLKY Pulse Width	t_{WXYH}, t_{WXYL}	100	244		ns	
CLKX, CLKY Rise and Fall Times	t_{RXY}, t_{FXY}		10	20	ns	
Hold Time from CLKX, CLKY to FSX, FSY	t_{HOLD}	0			ns	1
Setup Time from FSX, FSY to CLKX, CLKY low	t_{SF}	50			ns	1
Hold Time from CLKX, CLKY low to FSX, FSY low	t_{HF}	100			ns	1
XIN, YIN Setup to CLKX, CLKY low	t_{SD}	50			ns	1
XIN, YIN Hold to CLKX, CLKY low	t_{HD}	50			ns	1
Delay Time from CLKX, CLKY to Valid XOUT, YOUT	t_{DXYO}	10		150	ns	2
Delay Time from CLKX, CLKY to XOUT, YOUT Tri-stated	t_{DXYZ}	20		150	ns	1,2,3

NOTES:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.
2. Load = 150 pF + 2 LSTTL loads.
3. For LSB of PCM byte or ADPCM nibble.
4. Maximum width of FSX, FSY is one CLKX, CLKY period.
5. MCLK = 10 MHz ± 500 ppm.

MASTER CLOCK/RESET AC ELECTRICAL CHARACTERISTICS

(0° to 70°C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}		100		ns	5
MCLK Pulse Width	t_{WMH}, t_{WML}	45	50	55	ns	
$\overline{RST}$ Pulse Width	t_{WRL}	1			ms	

SERIAL PORT AC ELECTRICAL CHARACTERISTICS

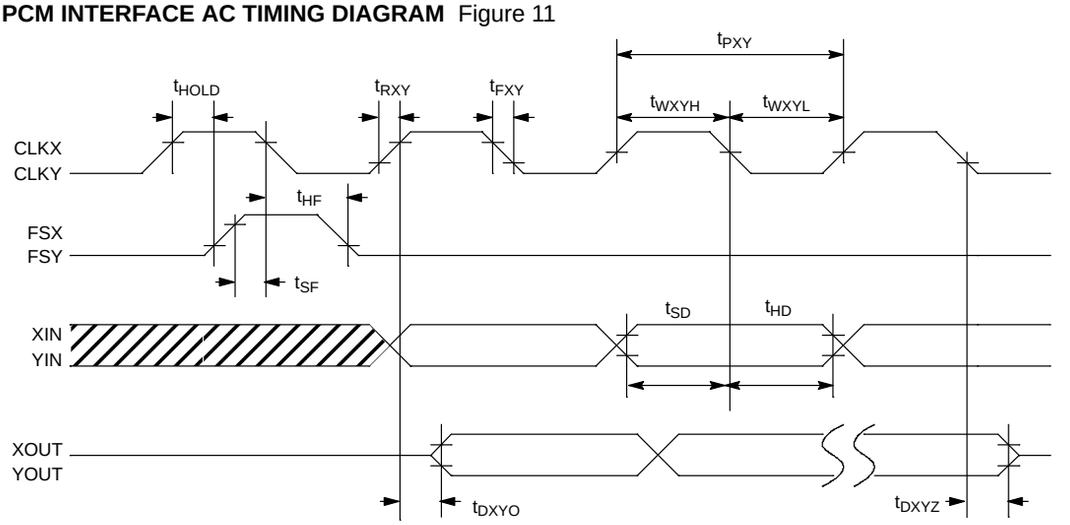
(0°C to 70°C, V_{DD} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Times	t_R, t_F			100	ns	1
$\overline{CS}$ to SCLK Setup	t_{CC}	50			ns	1
SCLK to $\overline{CS}$ Hold	t_{CCH}	250			ns	1
$\overline{CS}$ Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to $\overline{CS}$ Falling	t_{SCC}	50			ns	1

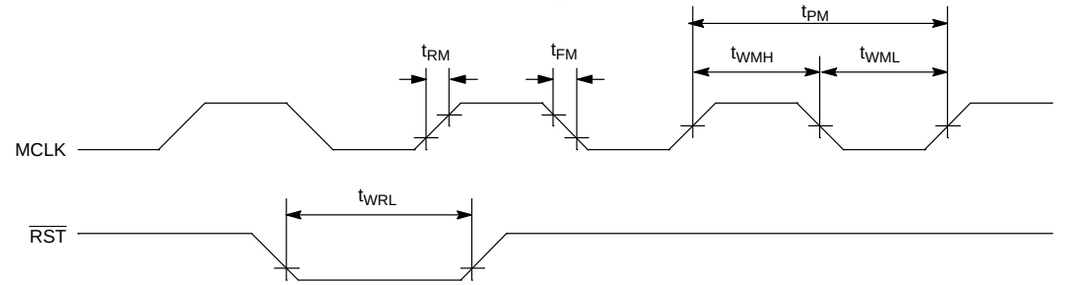
NOTES:

1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.
2. MCLK = 10 MHz ± 500 ppm.

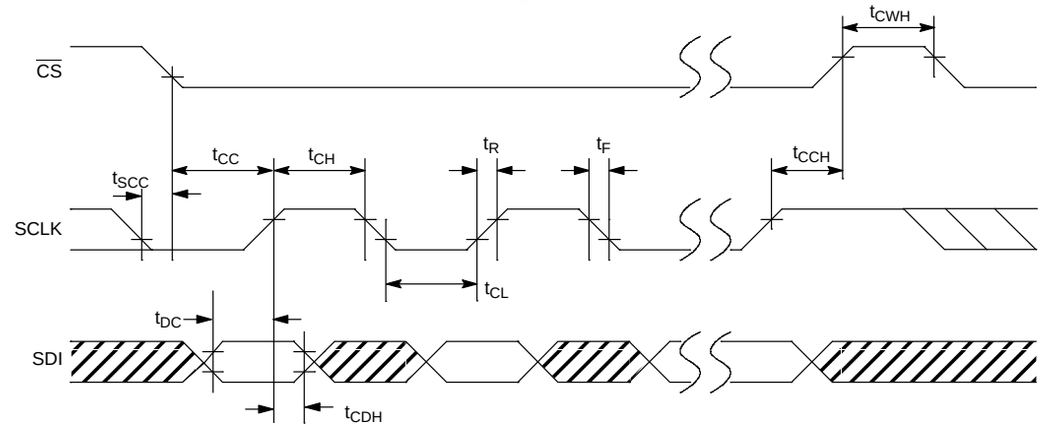
PCM INTERFACE AC TIMING DIAGRAM Figure 11



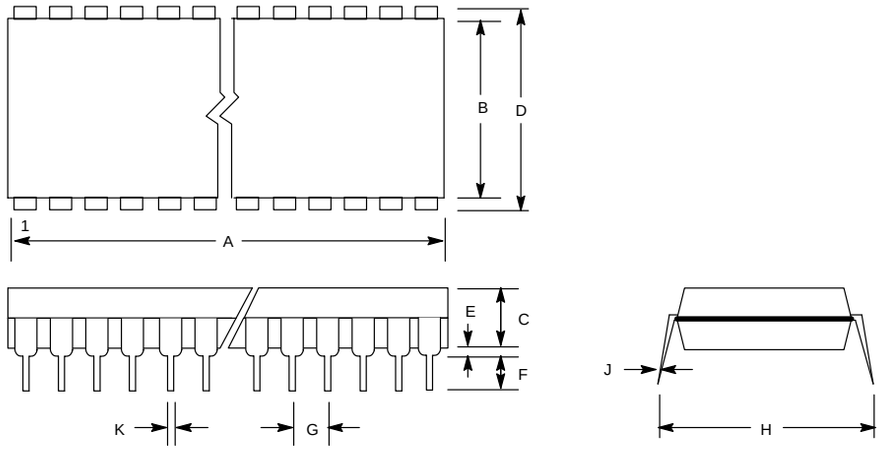
MASTER CLOCK/RESET AC TIMING DIAGRAM Figure 12



SERIAL PORT WRITE AC TIMING DIAGRAM Figure 13

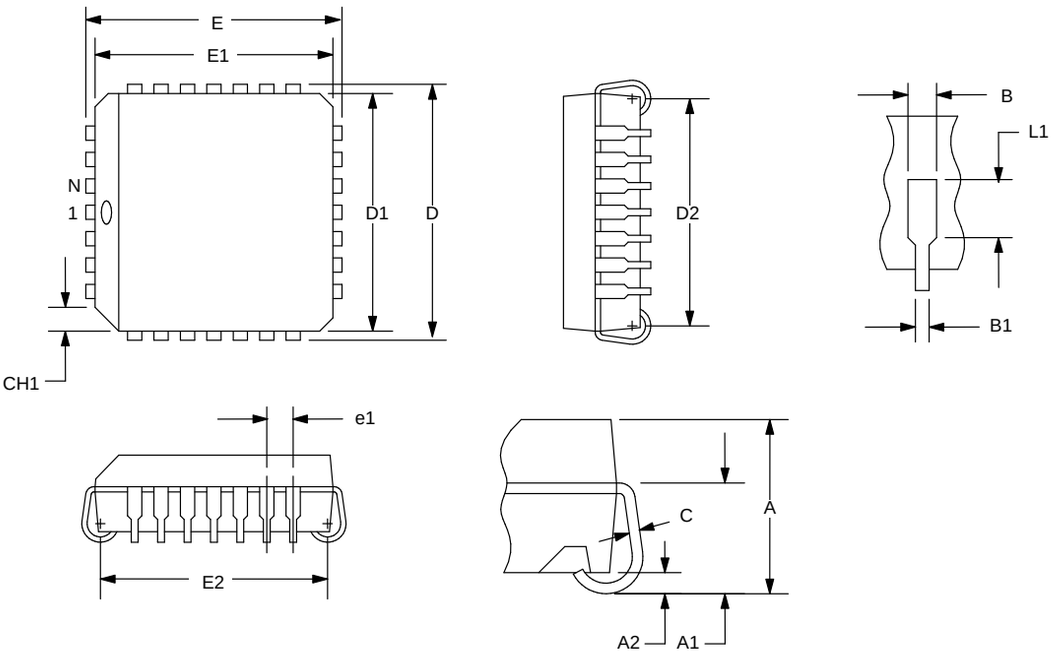


DS2167/DS2168 ADPCM PROCESSOR
24-PIN DIP



DIM	INCHES	
	MIN	MAX
A IN. MM	1.245 31.62	1.270 32.25
B IN. MM	0.530 13.46	0.550 13.97
C IN. MM	0.140 3.56	0.160 4.06
D IN. MM	0.600 15.24	0.625 15.88
E IN. MM	0.015 0.380	0.050 1.27
F IN. MM	0.120 3.05	0.145 3.68
G IN. MM	0.090 2.29	0.110 2.79
H IN. MM	0.625 15.88	0.675 17.15
J IN. MM	0.008 0.20	0.012 0.30
K IN. MM	0.015 0.38	0.022 0.56

DS2167/DS2168Q ADPCM PROCESSOR
28-PIN PLCC



DIM.	INCHES	
	MIN.	MAX.
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	–
N	28	–
e1	0.050 BSC	
CH1	0.042	0.048