National Semiconductor

May 2006

# DS25BR400
# Quad Transceiver with Input Equalization and Output De-Emphasis

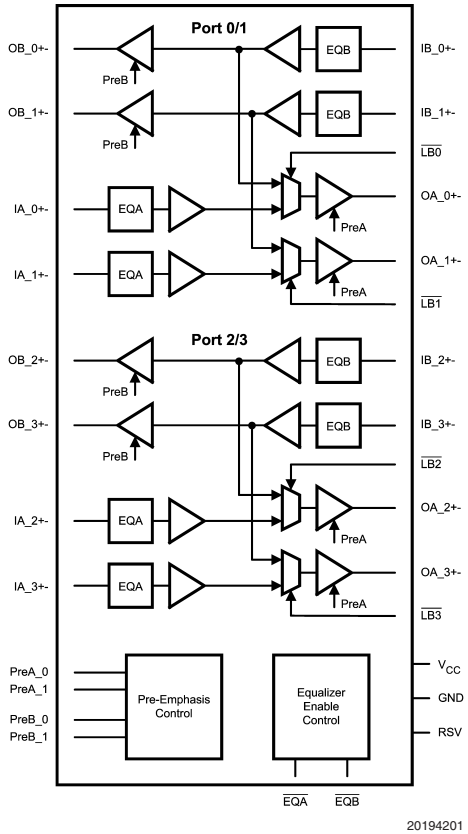
## General Description

The DS25BR400 is a quad 250 Mbps – 2.5 Gbps CML transceiver, or 8-channel buffer, for use in XAUI Fibre Channel backplane and cable applications. With operation down to 250 Mbps, the DS25BR400 can be used in applications requiring both low and high frequency data rates. Each input stage has a fixed equalizer to reduce ISI distortion from board traces. The equalizers are grouped in fours and are enabled through two control pins. These control pins provide customers flexibility in XAUI applications where ISI distortion may vary from one direction to another. All output drivers have four selectable steps of de-emphasis to compensate against transmission loss across long FR4 backplanes. The de-emphasis blocks are also grouped in fours. In addition, the DS25BR400 also has loopback control capability on four channels. All CML drivers and receivers are internally terminated with 50Ω pull-up resistors.

## Features

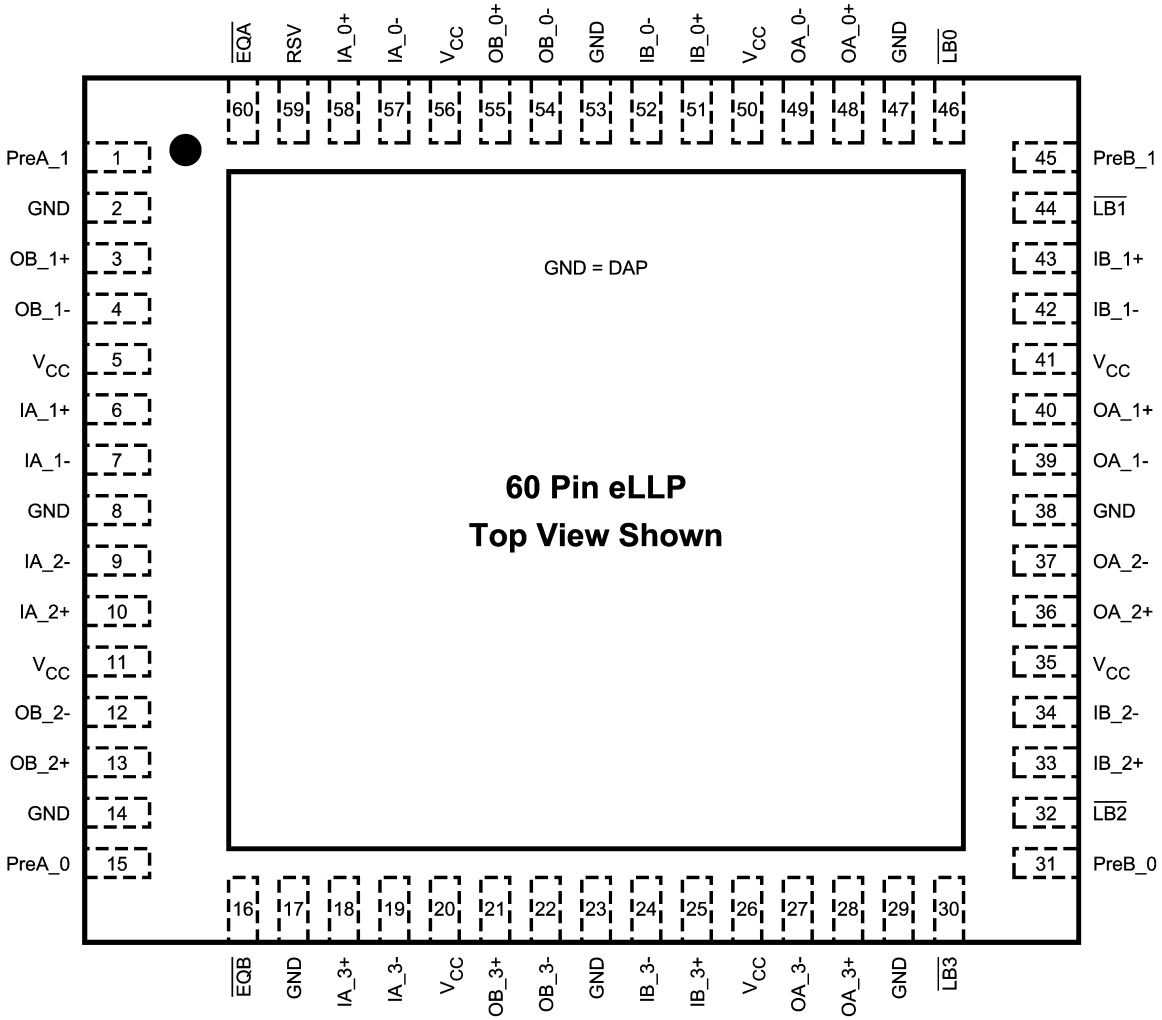
- Quad 2.5 Gbps Transceiver or 8-Channel CML Serial Buffer
- 250 Mbps – 2.5 Gbps Fully Differential Data Paths
- Optional Fixed Input Equalization
- Selectable Output De-emphasis
- Individual Loopback Controls
- On-chip Termination
- +3.3V supply
- Low Power, 1.3 Watts MAX
- Lead-less eLLP-60 pin package (9mmx9mmx0.8mm, 0.4mm pitch)
- –40˚C to +85˚C Industrial Temperature Range
- 6 kV ESD Rating, HBM

## Functional Block Diagram



## Connection Diagram

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**Leadless eLLP-60 Pin Package**
**(9mmx9mmx0.8mm, 0.4mm pitch)**
**Order number DS25BR400TSQ**
**See NS Package Number SQA060**

## Pin Descriptions

| Pin Name | Pin Number | I/O | Description |
|---|---|---|---|
| **DIFFERENTIAL I/O** | | | |
| IB_0+<br>IB_0– | 51<br>52 | I | Inverting and non-inverting differential inputs of port_0. IB_0+ and IB_0– are internally connected to a reference voltage through a 50Ω resistor. |
| OA_0+<br>OA_0– | 48<br>49 | O | Inverting and non-inverting differential outputs of port_0. OA_0+ and OA_0– are connected to $V_{CC}$ through a 50Ω resistor. |
| IB_1+<br>IB_1– | 43<br>42 | I | Inverting and non-inverting differential inputs of port_1. IB_1+ and IB_1– are internally connected to a reference through a 50Ω resistor. |
| OA_1+<br>OA_1– | 40<br>39 | O | Inverting and non-inverting differential outputs of port_1. OA_1+ and OA_1– are connected to $V_{CC}$ through a 50Ω resistor. |
| IB_2+<br>IB_2– | 33<br>34 | I | Inverting and non-inverting differential inputs of port_2. IB_2+ and IB_2– are internally connected to a reference voltage through a 50Ω resistor. |
| OA_2+<br>OA_2– | 36<br>37 | O | Inverting and non-inverting differential outputs of port_2. OA_2+ and OA_2– are connected to $V_{CC}$ through a 50Ω resistor. |
| IB_3+<br>IB_3– | 25<br>24 | I | Inverting and non-inverting differential inputs of port_3. IB_3+ and IB_3– are internally connected to a reference voltage through a 50Ω resistor. |
| OA_3+<br>OA_3– | 28<br>27 | O | Inverting and non-inverting differential outputs of port_3. OA_3+ and OA_3– are connected to $V_{CC}$ through a 50Ω resistor. |
| IA_0+<br>IA_0– | 58<br>57 | I | Inverting and non-inverting differential inputs of port_0. IA_0+ and IA_0– are internally connected to a reference voltage through a 50Ω resistor. |
| OB_0+<br>OB_0– | 55<br>54 | O | Inverting and non-inverting differential outputs of port_0. OB_0+ and OB_0– are connected to $V_{CC}$ through a 50Ω resistor. |
| IA_1+<br>IA_1– | 6<br>7 | I | Inverting and non-inverting differential inputs of port_1. IA_1+ and IA_1– are internally connected to a reference through a 50Ω resistor. |
| OB_1+<br>OB_1– | 3<br>4 | O | Inverting and non-inverting differential outputs of port_1. OB_1+ and OB_1– are connected to $V_{CC}$ through a 50Ω resistor. |
| IA_2+<br>IA_2– | 10<br>9 | I | Inverting and non-inverting differential inputs of port_2. IA_2+ and IA_2– are internally connected to a reference voltage through a 50Ω resistor. |
| OB_2+<br>OB_2– | 13<br>12 | O | Inverting and non-inverting differential outputs of port_2. OB_2+ and OB_2– are connected to $V_{CC}$ through a 50Ω resistor. |
| IA_3+<br>IA_3– | 18<br>19 | I | Inverting and non-inverting differential inputs of port_3. IA_3+ and IA_3– are internally connected to a reference voltage through a 50Ω resistor. |
| OB_3+<br>OB_3– | 21<br>28 | O | Inverting and non-inverting differential outputs of port_3. OB_3+ and OB_3– are connected to $V_{CC}$ through a 50Ω resistor. |
| **CONTROL (3.3V LVCMOS)** | | | |
| $\overline{EQA}$ | 60 | I | This pin is active LOW. A logic LOW at $\overline{EQA}$ enables equalization for input channels IA_0±, IA_1±, IA_2±, and IA_3±. By default, this pin is internally pulled high and equalization is disabled. |
| $\overline{EQB}$ | 16 | I | This pin is active LOW. A logic LOW at $\overline{EQB}$ enables equalization for input channels IB_0±, IB_1±, IB_2±, and IB_3±. By default, this pin is internally pulled high and equalization is disabled. |
| PreA_0<br>PreA_1 | 15<br>1 | I | PreA_0 and PreA_1 select the output de-emphasis levels (OA_0±, OA_1±, OA_2±, and OA_3±). PreA_0 and PreA_1 are internally pulled high. Please see *Table 2* for de-emphasis levels. |
| PreB_0<br>PreB_1 | 31<br>45 | I | PreB_0 and PreB_1 select the output de-emphasis levels (OB_0±, OB_1±, OB_2±, and OB_3±). PreB_0 and PreB_1 are internally pulled high. Please see *Table 2* for de-emphasis levels. |
| $\overline{LB0}$ | 46 | I | This pin is active LOW. A logic LOW at $\overline{LB0}$ enables the internal loopback path from IB_0± to OA_0±. $\overline{LB0}$ is internally pulled high. Please see *Table 1* for more information. |
| $\overline{LB1}$ | 44 | I | This pin is active LOW. A logic LOW at $\overline{LB1}$ enables the internal loopback path from IB_1± to OA_1±. $\overline{LB1}$ is internally pulled high. Please see *Table 1* for more information. |

## Pin Descriptions (Continued)

| Pin Name | Pin Number | I/O | Description |
|---|---|---|---|
| **CONTROL (3.3V LVCMOS)** | | | |
| $\overline{LB2}$ | 32 | I | This pin is active LOW. A logic LOW at $\overline{LB2}$ enables the internal loopback path from IB_2± to OA_2±. $\overline{LB2}$ is internally pulled high. Please see *Table 1* for more information. |
| $\overline{LB3}$ | 30 | I | This pin is active LOW. A logic LOW at $\overline{LB3}$ enables the internal loopback path from IB_3± to OA_3±. $\overline{LB3}$ is internally pulled high. Please see *Table 1* for more information. |
| RSV | 59 | I | Reserve pin to support factory testing. This pin can be left open, tied to GND, or tied to GND through an external pull-down resistor. |
| **POWER** | | | |
| $V_{CC}$ | 5, 11, 20, 26, 35, 41, 50, 56 | P | $V_{CC}$ = 3.3V ± 5%.<br>Each $V_{CC}$ pin should be connected to the $V_{CC}$ plane through a low inductance path, typically with a via located as close as possible to the landing pad of the $V_{CC}$ pin.<br>It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each $V_{CC}$ pin to ground plane. |
| GND | 8, 14, 23, 29, 38, 47, 53 | P | Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin. |
| GND | DAP | P | DAP is the metal contact at the bottom side, located at the center of the eLLP-60 pin package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package. |

**Note:** I = Input, O = Output, P = Power

# Functional Description

**TABLE 1. Logic Table for Loopback Controls**

| $\overline{\text{LB0}}$ | **Loopback Function** |
|---|---|
| 0 | Enable loopback from IB_0± to OA_0±. |
| 1 (default) | Normal mode. Loopback disabled. |
| $\overline{\text{LB1}}$ | **Loopback Function** |
| 0 | Enable loopback from IB_1± to OA_1±. |
| 1 (default) | Normal mode. Loopback disabled. |
| $\overline{\text{LB2}}$ | **Loopback Function** |
| 0 | Enable loopback from IB_2± to OA_2±. |
| 1 (default) | Normal mode. Loopback disabled. |
| $\overline{\text{LB3}}$ | **Loopback Function** |
| 0 | Enable loopback from IB_3± to OA_3±. |
| 1 (default) | Normal mode. Loopback disabled. |

**TABLE 2. De-Emphasis Controls**

| **PreA_[1:0]** | **Default VOD Level in $mV_{PP}$ (VODB)** | **De-Emphasis Level in $mV_{PP}$ (VODPE)** | **De-Emphasis in dB (VODPE/VODB)** |
|---|---|---|---|
| 0 0 | 1200 | 1200 | 0 |
| 0 1 | 1200 | 850 | –3 |
| 1 0 | 1200 | 600 | –6 |
| 1 1 (Default) | 1200 | 426 | –9 |
| **PreB_[1:0]** | **Default VOD Level in $mV_{PP}$ (VODB)** | **De-Emphasis Level in $mV_{PP}$ (VODPE)** | **De-Emphasis in dB (VODPE/VODB)** |
| 0 0 | 1200 | 1200 | 0 |
| 0 1 | 1200 | 850 | –3 |
| 1 0 | 1200 | 600 | –6 |
| 1 1 (Default) | 1200 | 426 | –9 |

De-emphasis is the primary signal conditioning function for use in compensating against backplane transmission loss. The DS25BR400 provides four steps of de-emphasis ranging from 0, –3, –6 and –9 dB, user-selectable dependent on the loss profile of the backplane. *Figure 1* shows a driver de-emphasis waveform. The de-emphasis duration is nominal 188 ps, corresponding to 0.75 bit-width at 2.5 Gbps. The de-emphasis levels of switch-side and line-side can be individually programmed.

## Input Equalization

Each differential input of the DS25BR400 has a fixed equalizer front-end stage. It is designed to provide fixed equalization for short board traces with transmission losses of approximately 5 dB between 375 MHz to 1.875 GHz. Programmable de-emphasis together with input equalization ensures an acceptable eye opening for a 40-inch FR-4 backplane.

The differential input equalizer for inputs on Channel A and inputs on Channel B can be bypassed by using $\overline{EQA}$ and $\overline{EQB}$, respectively. By default, the equalizers are internally pulled high and disabled. Therefore, $\overline{EQA}$ and $\overline{EQB}$ must be asserted LOW to enable equalization.

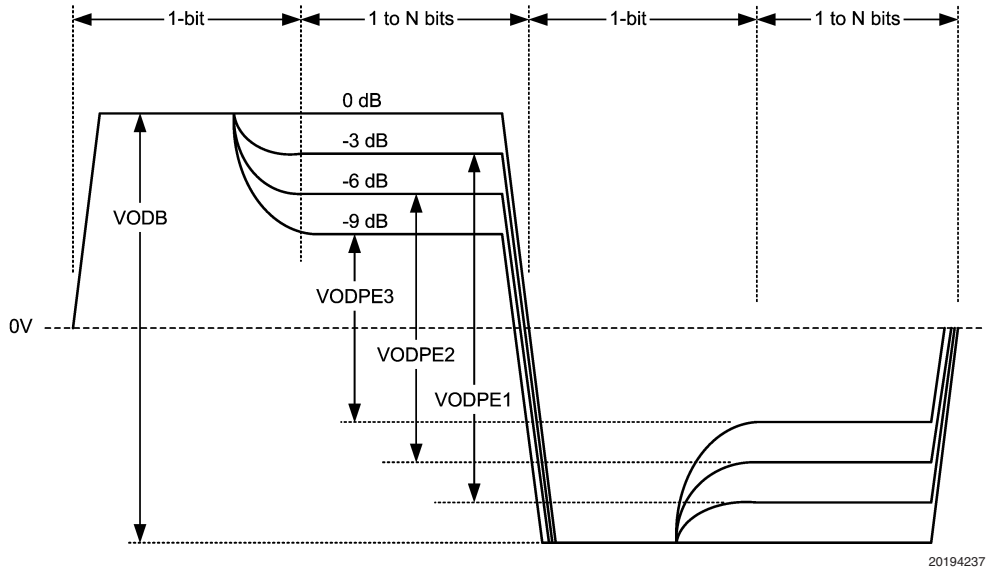



**FIGURE 1. Driver De-Emphasis Differential Waveform (showing all 4 de-emphasis steps)**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.3V to 4V |
| CMOS/TTL Input Voltage | −0.3V to ($V_{CC}$ +0.3V) |
| CML Input/Output Voltage | −0.3V to ($V_{CC}$ +0.3V) |
| Junction Temperature | +150˚C |
| Storage Temperature | −65˚C to +150˚C |
| Lead Temperature | |
| Soldering, 4 sec | +260˚C |
| Thermal Resistance, $\theta_{JA}$ | 22.3˚C/W |
| Thermal Resistance, $\theta_{JC}$ | 3.2˚C/W |
| Thermal Resistance, $\Phi_{JB}$ | 10.3˚C/W |
| (Note: assumes 26 thermal vias) | |
| ESD Ratings ((Note 9)) | |
| HBM | 6kV |
| CDM | 1kV |
| MM | 350V |

## Recommended Operating Ratings

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$-GND) | 3.135 | 3.3 | 3.465 | V |
| Supply Noise Amplitude 10 Hz to 2 GHz | | | 100 | $mV_{PP}$ |
| Ambient Temperature | −40 | | +85 | ˚C |
| Case Temperature | | | 100 | ˚C |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|
| **LVCMOS DC SPECIFICATIONS** | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | 2.0 | | $V_{CC}$ +0.3 | V |
| $V_{IL}$ | Low Level Input Voltage | | −0.3 | | 0.8 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN} = V_{CC}$ | −10 | | 10 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = GND | 75 | 94 | 124 | µA |
| $R_{PU}$ | Pull-High Resistance | | | 35 | | kΩ |
| **RECEIVER SPECIFICATIONS** | | | | | | |
| $V_{ID}$ | Differential Input Voltage Range | AC Coupled Differential Signal.<br>Below 1.25 Gb/s<br>At 1.25 Gbps–3.125 Gbps<br>Above 3.125 Gbps<br>This parameter is not production tested. | <br>100<br>100<br>100 | | <br>1750<br>1560<br>1200 | <br>$mV_{P-P}$<br>$mV_{P-P}$<br>$mV_{P-P}$ |
| $V_{ICM}$ | Common Mode Voltage at Receiver Inputs | Measured at receiver inputs reference to ground. | | 1.3 | | V |
| $R_{ITD}$ | Input Differential Termination | On-chip differential termination between IN+ or IN−. | 84 | 100 | 116 | Ω |
| $R_{ITSE}$ | Input Termination (single-end) | On-chip termination IN+ or IN− to GND for frequency > 100 MHz. | | 50 | | Ω |
| **DRIVER SPECIFICATIONS** | | | | | | |
| VODB | Output Differential Voltage Swing without De-Emphasis | $R_L$ = 100Ω ±1%<br>PreA_1 = 0; PreA_0 = 0<br>PreB_1 = 0; PreB_0 = 0<br>Driver de-emphasis disabled.<br>Running K28.7 pattern at 2.5 Gbps.<br>*(Figure 6)* | 1000 | 1200 | 1400 | $mV_{P-P}$ |

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|
| **DRIVER SPECIFICATIONS** | | | | | | |
| $V_{PE}$ | Output De-Emphasis Voltage Ratio 20*log(VODPE/VODB) | $R_L$ = 100Ω ±1%<br>Running K28.7 pattern at 2.5 Gbps<br>PreX_[1:0] = 00<br>PreX_[1:0] = 01<br>PreX_[1:0] = 10<br>PreX_[1:0] = 11<br>X = A/B channel de-emphasis drivers<br>*(Figure 1 / Figure 6)* | | <br><br>0<br>–3<br>–6<br>–9 | | <br><br>dB<br>dB<br>dB<br>dB |
| $t_{PE}$ | De-Emphasis Width | Tested at –9 dB de-emphasis level, PreX[1:0] = 11<br>X = A/B channel de-emphasis drivers<br>See *Figure 5* on measurement condition. | 125 | 200 | 250 | ps |
| $R_{OTSE}$ | Output Termination | On-chip termination from OUT+ or OUT– to $V_{CC}$ | 42 | 50 | 58 | Ω |
| $R_{OTD}$ | Output Differential Termination | On-chip differential termination between OUT+ and OUT– | | 100 | | Ω |
| $\Delta R_{OTSE}$ | Mis-Match in Output Termination Resistors | Mis-match in output termination resistors | | | 5 | % |
| $V_{OCM}$ | Output Common Mode Voltage | | | 2.7 | | V |
| **POWER DISSIPATION** | | | | | | |
| $P_D$ | Power Dissipation | $V_{DD}$ = 3.465V<br>All outputs terminated by 100Ω ±1%.<br>PreB_[1:0] = 0, PreA_[1:0] = 0<br>Running PRBS $2^7$-1 pattern at 2.5 Gbps | | | 1.3 | W |
| **AC CHARACTERISTICS** | | | | | | |
| $t_R$ | Differential Low to High Transition Time | Measured with a clock-like pattern at 2.5 Gbps, between 20% and 80% of the differential output voltage.<br>De-emphasis disabled.<br>Transition time is measured with the fixture shown in *Figure 6* adjusted to reflect the transition time at the output pins. | | 80 | | ps |
| $t_F$ | Differential High to Low Transition Time | | | 80 | | ps |
| $t_{PLH}$ | Differential Low to High Propagation Delay | Measured at 50% differential voltage from input to output. | | | 1 | ns |
| $t_{PHL}$ | Differential High to Low Propagation Delay | | | | 1 | ns |
| $t_{SKP}$ | Pulse Skew | $\lvert t_{PHL} - t_{PLH} \rvert$ | | | 20 | ps |
| $t_{SKO}$ | Output Skew (Note 7) | Difference in propagation delay between channels on the same part (Channel-to-Channel Skew) | | | 100 | ps |
| $t_{SKPP}$ | Part-to-Part Skew (Note 7) | Difference in propagation delay between devices across all channels operating under identical conditions | | | 165 | ps |
| $t_{LB}$ | Loopback Delay Time | Delay from enabling loopback mode to signals appearing at the differential outputs<br>*Figure 4* | | | 4 | ns |

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | |
| RJ | Device Random Jitter (Note 5) | At 0.25 Gbps<br>At 1.5 Gbps<br>At 2.5 Gbps<br>Alternating-10 pattern.<br>De-emphasis disabled.<br>*(Figure 6*) | | | 2<br>2<br>2 | ps rms<br>ps rms<br>ps rms |
| DJ | Device Deterministic Jitter (Note 6) | At 0.25 Mbps, PRBS7 pattern<br>At 1.5 Gbps, K28.5 pattern<br>At 2.5 Gbps, K28.5 pattern<br>At 2.5 Gbps, PRBS7 pattern<br>De-emphasis disabled.<br>*(Figure 6*) | | | 25<br>25<br>25<br>25 | ps pp<br>ps pp<br>ps pp<br>ps pp |
| DR | Data Rate (Note 8) | Alternating-10 pattern | 0.25 | | 2.5 | Gbps |

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables. Operation of the device beyond the maximum Operating Ratings is not recommended.

**Note 2:** Typical specifications are at TA=25 C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not guaranteed.

**Note 3:** IN+ and IN– are generic names that refer to one of the many pairs of complementary inputs of the DS25BR400. OUT+ and OUT– are generic names that refer to one of the many pairs of the complementary outputs of the DS25BR400. Differential input voltage $V_{ID}$ is defined as |IN+ – IN–|. Differential output voltage $V_{OD}$ is defined as |OUT+ – OUT–|.

**Note 4:** K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000}

K28.5 pattern is a 20-bit repeating pattern of +K28.5 and –K28.5 code groups {110000 0101 001111 1010}

**Note 5:** Device output random jitter is a measurement of random jitter contributed by the device. It is derived by the equation $SQRT[(RJ_{OUT})^2 – (RJ_{IN})^2]$, where $RJ_{OUT}$ is the total random jitter measured at the output of the device in ps(rms), $RJ_{IN}$ is the random jitter of the pattern generator driving the device. Below 400 Mbps, system jitter and device jitter could not be separated. The 250 Mbps specification includes system random jitter. Please see *Figure 6* for the AC test circuit.

**Note 6:** Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation ($DJ_{OUT}$ - $DJ_{IN}$), where $DJ_{OUT}$ is the total peak-to-peak deterministic jitter measured at the output of the device in ps(p-p). $DJ_{IN}$ is the peak-to-peak deterministic jitter at the input of the test board. Please see *Figure 6* for the AC test circuit.

**Note 7:** $t_{SKO}$ is the magnitude difference in propagation delays between all data paths on one device. This is channel-to-channel skew. $t_{SKPP}$ is the worst case difference in propagation delay across multiple devices on all channels and operating under identical conditions. For example, for two devices operating under the same conditions, $t_{SKPP}$ is the magnitude difference between the shortest propagation delay measurement on one device to the longest propagation delay measurement on another device.

**Note 8:** This parameter is guaranteed by design and/or characterization and is not tested in production.

**Note 9:** ESD tests conform to the following standards:

Human Body Model (HBM) applicable standard: MIL-STD-883, Method 3015.7

Machine Model (MM) applicable standard: JESD22-A115-A (ESD MM std. of JEDEC)

Field -Induced Charge Device Model (CDM) applicable standard: JESD22-C101-C (ESD FICDM std. of JEDEC)

## Timing Diagrams

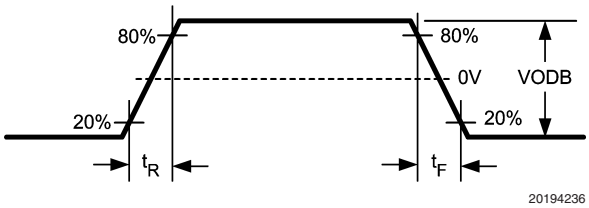



**FIGURE 2. Driver Output Transition Time**

## Timing Diagrams (Continued)

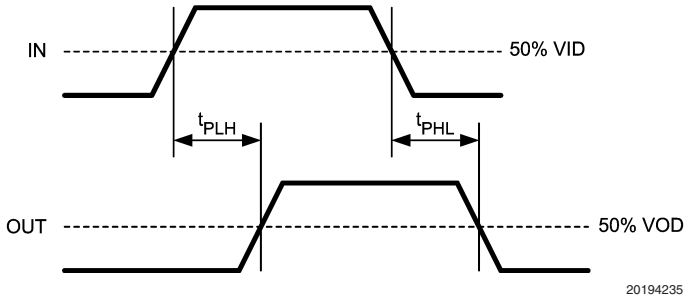



**FIGURE 3. Propagation Delay**

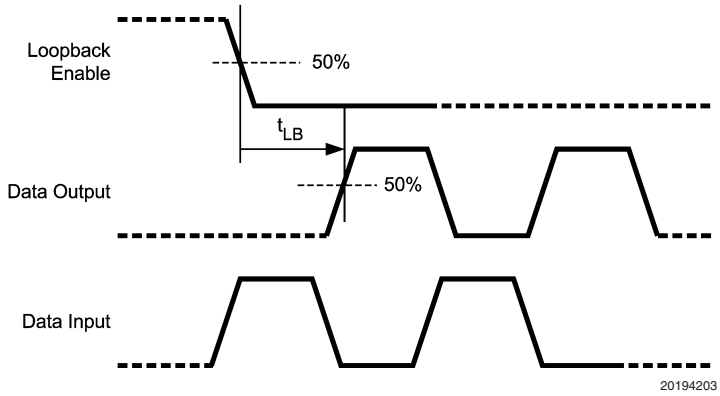



**FIGURE 4. Loopback Delay Timing**

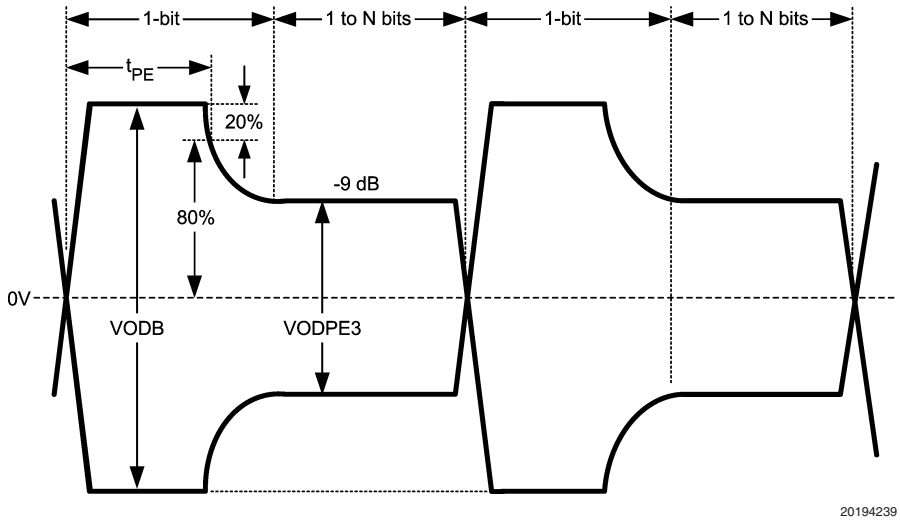



**FIGURE 5. Output De-Emphasis Duration**

## Timing Diagrams (Continued)

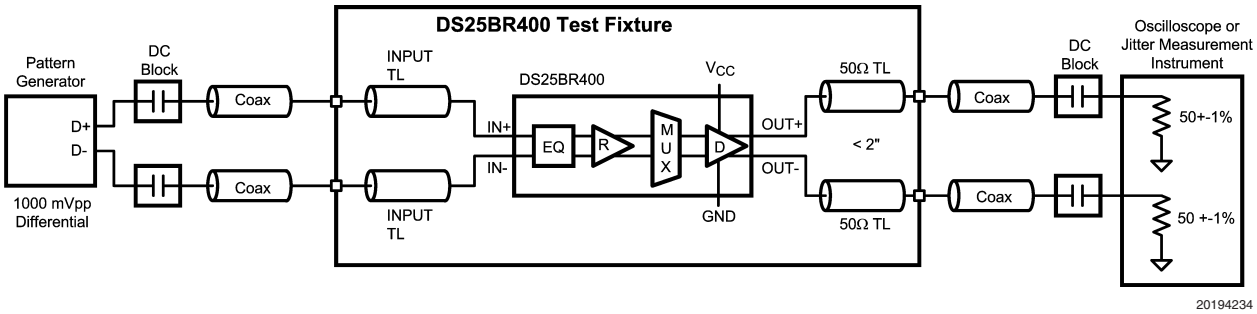
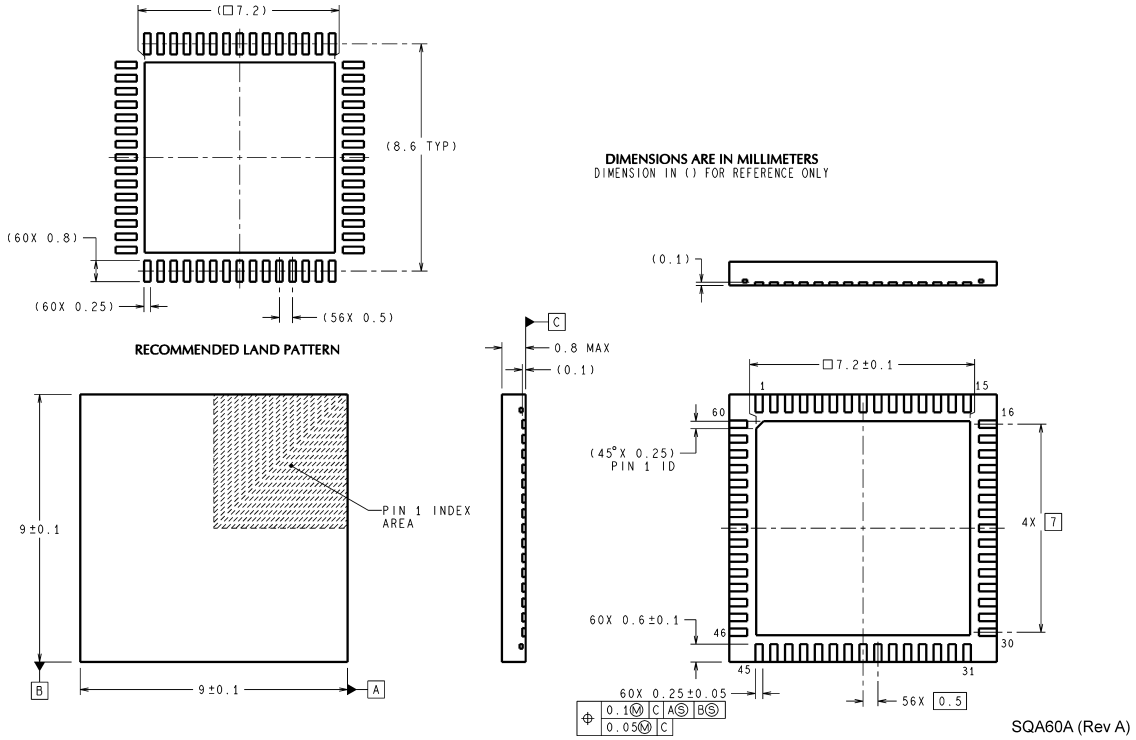



**FIGURE 6. AC Test Circuit**

## Physical Dimensions inches (millimeters) unless otherwise noted




**eLLP-60 Package**
**Order Number DS25BR400TSQ**
**NS Package Number SQA060**



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