National Semiconductor

PRELIMINARY
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DS25C400
Quad 2.5 Gbps Serializer/Deserializer

General Description

The DS25C400 is a four-channel serializer/deserializer (SERDES) for high-speed serial data transmission over controlled impedance transmission media such as a printed circuit board backplane or twin-axial cable. It is capable of transmitting and receiving serial data of 2.125 - 2.5 Gbps or 1.0625 - 1.25 Gbps per channel.

Each transmit section of the DS25C400 contains a low-jitter clock synthesizer, an 8-bit or 10-bit parallel to serial converter with built in 8b/10b encoder, and a CML output driver with selectable pre-emphasis optimized for backplane applications. Its receive section contains an input limiting amplifier with on-chip terminations and selectable equalization levels, a clock/data recovery PLL, a comma detector and a serial to parallel converter with built-in 8b/10b decoder.

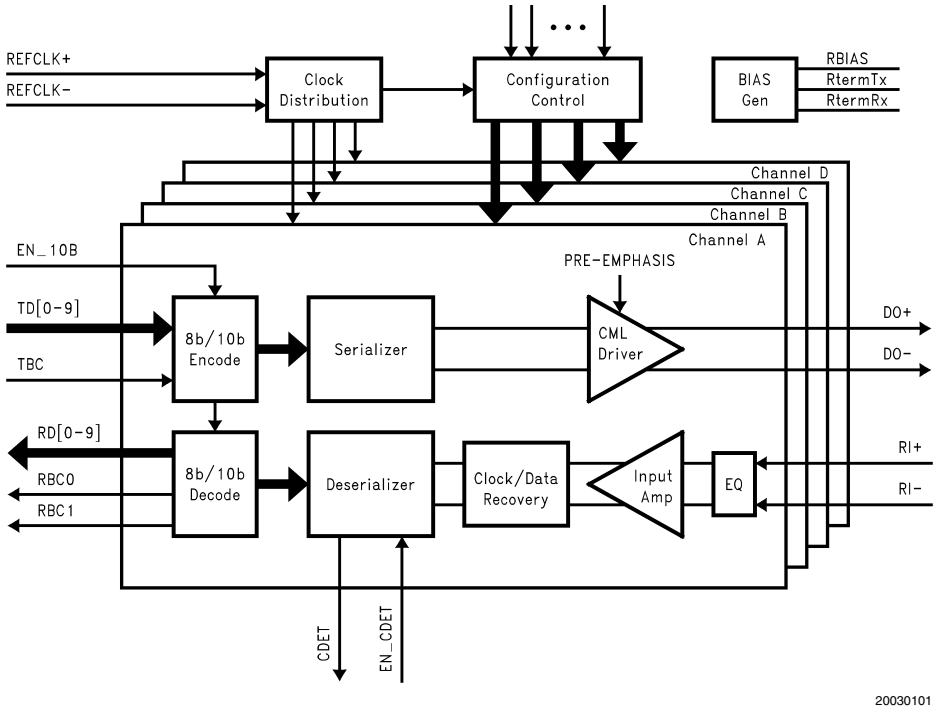
The DS25C400 has built-in local loopback test mode, pseudo-random pattern generator and error detector to support self-testing.

The DS25C400 requires no external components for its clock synthesizers and clock recovery PLL's. Three external resistors are needed to set the proper bias currents and compensate for process variations to achieve tight tolerance on-chip terminations.

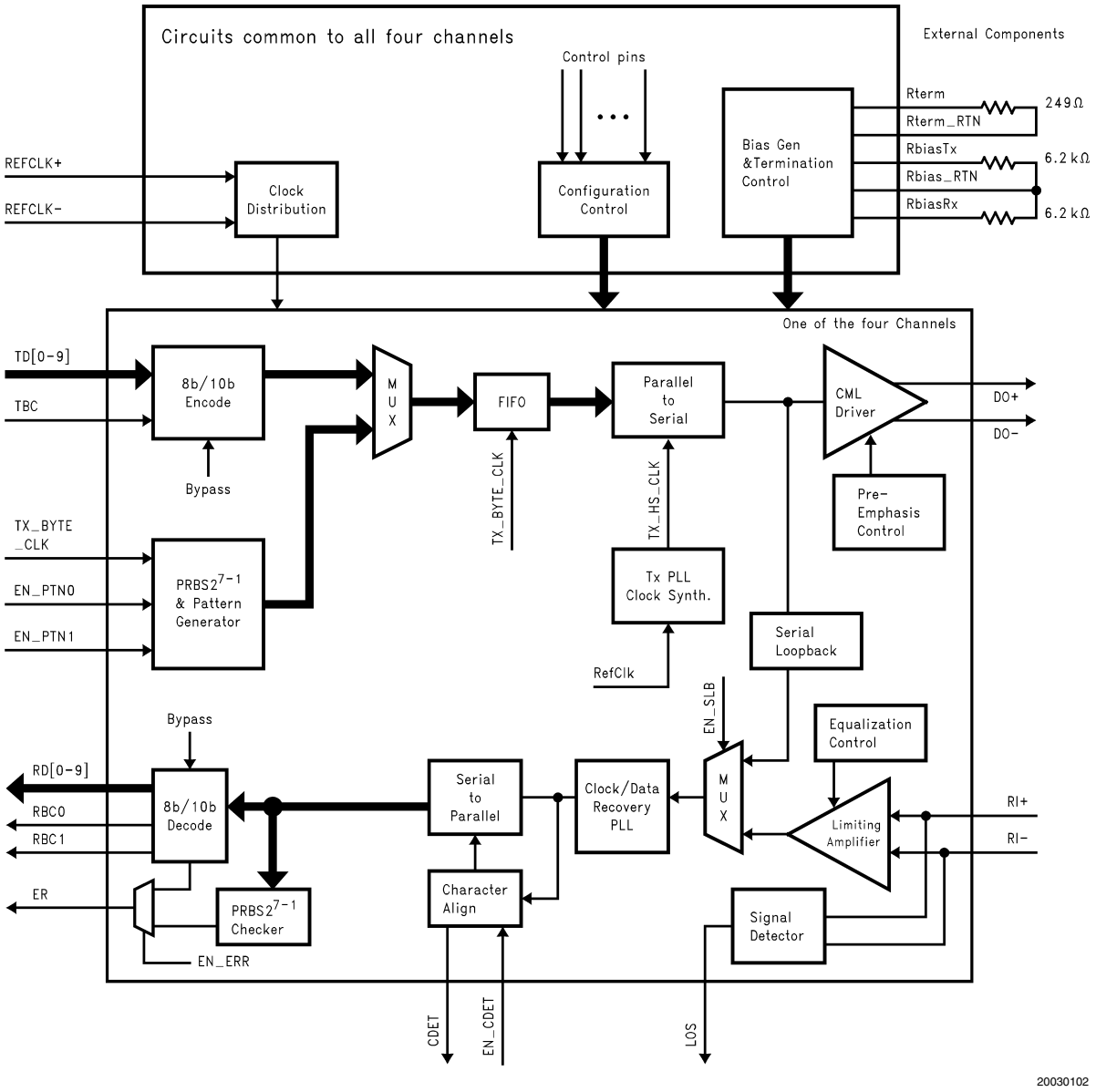
Features

- Quad Serializer/Deserializer
- Data rate per channel: 2.125 - 2.5 Gbps or 1.0625 - 1.25 Gbps
- Supports 106.25 - 125 MHz differential reference input clock
- Low jitter clock synthesizers for clock distribution
- 8-bit or 10-bit parallel I/O Interface conforms to SSTL_18 Class 1 (also interfaces to 1.8V HSTL or 1.8V LVCMOS)
- On-chip 8b/10b encoder and decoder
- High speed serial CML drivers
- High speed serial CML on-chip terminations
- Selectable pre-emphasis and equalization
- On-chip Comma Detect for character alignment
- On-chip local loopback test mode
- On-chip pattern generator and error checker to support BIST
- Hot plug protection
- Low power, 420 mW (typ) per channel
- 324-ball TE-PBGA package
- Operating temperature –40˚C to +85˚C

General Function Diagram



Functional Block Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DDQ}, DV_{DD})	−0.3V to +2.3V
Supply Voltage (V_{DDIO}, V_{DDHS}, V_{DDB})	−0.3V to +3.0V
SSTL Input Voltage	−0.3V to (V_{DDQ} + 0.3V)
LVCMOS Input Voltage	−0.3V to (DV_{DD} + 0.3V)
LVCMOS Output Voltage	−0.3V to (DV_{DD} + 0.3V)
CML Receiver Input Voltage	−0.3V to (V_{DDHS} + 0.3V)
CML Driver Output Voltage	−0.3V to (V_{DDHS} + 0.3V)
Junction Temperature	+125˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature Soldering, 4 Seconds	+260˚C
Maximum Package Power Dissipation at 25˚C DS25C400TUT	5.68 W
Derating above 25˚C	45.45 mW/˚C
Thermal Resistance, θ_{JA}	22 ˚C/W
Junction-to-case Conductive Thermal Resistance, θ_{JC}	6.5 ˚C/W
ESD Rating HBM, 1.5 kΩ, 100 pF	>2 kV
EIAJ, 0Ω, 200 pF	>200 V

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage V_{DDQ} and DV_{DD} to DGND	1.7	1.8	1.9	V
V_{DDIO}, V_{DDHS} and V_{DDB} to DGND or AGND	2.35	2.5	2.65	V
Temperature	−40	25	85	˚C
Supply Noise Amplitude			<100	mV_{P-P}
Supply Noise Frequency			<1	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
SSTL_18 DC SPECIFICATIONS—Parallel I/O, Class I						
V_{REF}	Reference Voltage		0.83	0.90	0.97	V
V_{TT}	Termination Voltage		V_{REF} − 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (dc)	High Level Input Voltage		V_{REF} +0.125		V_{DDQ} +0.300	V
V_{IH} (ac)	AC Input Logic High		V_{REF} +0.250			V
V_{IL} (dc)	Low Level Input Voltage		−0.300		V_{REF} −0.125	V
V_{IL} (ac)	AC Input Logic Low				V_{REF} −0.250	V
I_{IH}	High Level Input Current	V_{IN} = V_{DDQ} = 1.9 V	−10		+50	µA
I_{IL}	Low Level Input Current	V_{IN} = GND, V_{DDQ} = 1.9 V	−10		+10	µA
V_{OH} (dc)	High Level Output Voltage	I_{OH} = −6.3 mA, Unterminated, C_L = 8pF	V_{DDQ} −0.400			V
		Terminated, R = 50 Ω to V_{TT}	V_{DDQ} −0.550			V
V_{OL} (dc)	Low Level Output Voltage	I_{OL} = 6.3 mA, Unterminated, C_L = 8pF			0.400	V
		Terminated, R = 50 Ω to V_{TT}			0.550	V
LVCMOS DC SPECIFICATIONS—Control Pins EIA/JESD8-7 Compliant						
V_{IH}	High Level Input Voltage		0.65* DV_{DD}		DV_{DD}	V
V_{IL}	Low Level Input Voltage		0		0.35* DV_{DD}	V

Electrical Characteristics Over recommended operating supply and temperature ranges unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
LVCMOS DC SPECIFICATIONS—Control Pins EIA/JESD8-7 Compliant						
I_{IH}	High Level Input Current	$V_{IN} = DV_{DD} = 1.9$ V (input and pull-low)		0.1		mA
I_{IH}	High Level Input Current	$V_{IN} = DV_{DD} = 1.9$ V (input with pull-high)	−10		+10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND, $DV_{DD} = 1.9$ V (input with pull-low)	−10		+10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND, $DV_{DD} = 1.9$ V (input with pull-high)		−0.1		mA
V_{OH}	High Level Output Voltage	$I_{OH} = -2$ mA	DV_{DD} −0.45			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2$ mA			0.45	V
SUPPLY CURRENT						
I_{DD}	Total Supply Current	K28.5 pattern at 2.5 Gbps with no pre-emphasis. SSTL outputs no load termination resistors, Tx high speed serial outputs driving 100Ω differential, no high speed Rx input data.				
		$V_{DDHS} + V_{DDIO} + V_{DDB}$		572	600	mA
		$DV_{DD} + V_{DDQ}$		130	136.5	mA
P_D	Total Power Consumption	K28.5 pattern at 2.5 Gbps with no pre-emphasis. SSTL outputs no load termination resistors, Tx high speed serial outputs driving 100Ω differential, no high speed Rx input data.				
		SERDES and SSTL I/O		1708	1940	mW
RECOMMENDED INPUT REFERENCE CLOCK (REFCLK±) AC coupled differential signal						
$VIDS_{RCLK}$	Differential Input Voltage *Figure 1*	Terminated by 50Ω parallel termination	600		1500	mV_{p-p}
V_{ICM}	Common Mode Voltage	Terminated by 50Ω Parallel Termination	1.0		V_{DDHS} −0.5	V
R_{REFCLK}	Input Termination to GND	Equivalent Parallel Input Termination at REFCLK+ or REFCLK− to GND		100		Ω
f_{REF}	REFCLK Frequency Range		106.25		125	MHz
df_{REF}	REFCLK Frequency Variation	Variation from Nominal Frequency	−100		+100	ppm
t_{REF-DC}	REFCLK Duty Cycle (Note 3)	Between 50% of the differential voltage across REFCLK+ and REFCLK−	40	50	60	%
t_{REF-RJ}	REFCLK Input Random (rms) Jitter			3	5	ps
t_{REF-RJ}	REFCLK Input Peak-to-Peak Jitter			25	40	ps
t_{REF-X}	REFCLK Transition Time *Figure 1*	Transition time between 20% and 80% of the differential voltage across REFCLK+ and REFCLK−	0.2		1	ns

Electrical Characteristics Over recommended operating supply and temperature ranges unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
SERIALIZER						
DR_{DO}	Transmit Data Rate	Data Rate at DO±				
		High Data Rate Mode (EN_HDR = 1)	2.125		2.5	Gbps
		Low Data Rate Mode (EN_HDR = 0)	1.0625		1.25	Gbps
V_{ODS}	Output Differential Voltage Swing (DO+ – DO–) WITHOUT Pre-emphasis	DO+, DO– are terminated by external 50Ω to V_{DDHS} PSEL1 = 0, PSEL0 = 0	850	1065	1280	mV_{p-p}
	Output Differential Voltage Swing (DO+ – DO–) WITH Pre-emphasis	DO+, DO– are terminated by external 50Ω to V_{DDHS}				
		PSEL1 = 0, PSEL0 = 1	TBD	1330	TBD	mV_{p-p}
		PSEL1 = 1, PSEL0 = 0	TBD	1600	TBD	
		PSEL1 = 1, PSEL0 = 1	TBD	1850	TBD	
V_{CM}	Output Common Mode Offset Voltage WITHOUT Pre-emphasis	DO+, DO– are terminated by external 50Ω to V_{DDHS} PSEL1 = 0, PSEL0 = 0	–10%	V_{DDHS} –0.3	+10%	V
	Output Common Mode Offset Voltage WITH Pre-emphasis	DO+, DO– are terminated by external 50Ω to V_{DDHS}				
		PSEL1 = 0, PSEL0 = 1	–10%	V_{DDHS} –0.37	+10%	V
		PSEL1 = 1, PSEL0 = 0		V_{DDHS} –0.43		
		PSEL1 = 1, PSEL0 = 1		V_{DDHS} –0.50		
R_{DO}	Output Resistance	On-chip termination DO+ or DO– to V_{DDHS}, RTERM = 249Ω	45	50	55	Ω
C_{DO}	Capacitance to GND	DO+ or DO– to GND		1		pF
t_{DO-X}	Serial Data Output Transition Time	Measured between 20% and 80% of V_{ODS}	100	120	160	ps
JIT_{DO-DJ}	Serial Data Output Deterministic Jitter (Peak-to-Peak), (Notes 4, 5)	Output K28.5 at 2.5 Gbps		0.1	0.13	UI
JIT_{DO-RJ}	Serial Data Output Random Jitter (Peak-to-Peak), (Notes 4, 5)	Output D21.5 at 2.5 Gbps		0.13	0.15	UI
JIT_{DO-TJ}	Serial Data Output Total Jitter, (Notes 4, 5)	Output K28.5 pattern at 2.5 Gbps at BER of 10^{-12}		0.2	0.25	UI
t_{LAT-TX}	Transmit Latency *Figure 2*	Transmit K28.5 from TD[0–9] to DO± at 2.5 Gbps, EN_10B = 1	35		48	Bits
		Transmit K28.5 from TD[0–9] to DO± at 2.5 Gbps, EN_10B = 0	45		58	Bits
$t_{DO-LOCK}$	Lock Time	Time to achieve frequency lock to REFCLK. Output K28.5 at 2.5 Gbps.			0.5	ms
DESERIALIZER						
DR_{RI}	Receive Data Rate	High Data Rate (EN_HDR = 1)	2.125		2.5	Gbps
		Low Data Rate (EN_HDR = 0)	1.0625		1.25	Gbps
$VIDS_{RI}$	Differential Input Voltage	RI+ – RI–	200		1500	mV_{p-p}
R_{RI}	Input Termination to V_{DDHS}	On-chip termination RI+ to RI– to V_{DDHS} EN_RAC = 0, RTERM = 249Ω:	45	50	55	Ω

Electrical Characteristics Over recommended operating supply and temperature ranges unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
DESERIALIZER						
C_{RI}	Input Capacitance to GND	RI+ or RI– to GND		1		pF
$V_{RI-BIAS}$	Input Bias Voltage	DC bias at RI+ or RI– when configure for AC couple (EN_RAC = 1)	0.9* V_{DDHS}	0.91* V_{DDHS}	0.92* V_{DDHS}	V
R_{RIAC}	Equivalent Parallel Input Termination	Equivalent parallel termination at RI+ or RI– to GND EN_RAC = 1, RTERM = 249Ω:	45	50	55	Ω
t_{LAT-RX}	Receive Latency *Figure 3*	Receive K28.5 from RI± to RD[0–9] at 2.5 Gbps, EN_10B = 1	76		95	Bits
		Receive K28.5 from RI± to RD[0–9] at 2.5 Gbps, EN_10B = 0	86		105	Bits
JIT_{RI-TL}	Input Jitter Tolerance Without Equalizer, (Notes 4, 5)	Receiving RPAT pattern at 2.5Gbps at BER of 10^{-12} of random jitter (1.5MHz to 1.25GHz)	0.22			UI
		Receiving RPAT pattern at 2.5Gbps at BER of 10^{-12} of non-sinusoidal deterministic jitter (1.5MHz to 1.25GHz)	0.5			UI
$F_{FRI-LOCK}$	Receiver Lock Range	Input data rate reference to local transmit data rate	–200		+200	ppm
$t_{RI-LOCK}$	Maximum Lock Time				500	µs
LOS_{TH}	Loss of Signal Detect Thresholds	Loss of Signal OFF			200	mV_{p-p}
		Loss of Signal ON	80			mV_{p-p}
T_{LOSOFF}	Loss of Signal Detect Off Timing	Loss of signal OFF time. VIDS = 200 mV_{p-p}			100	µs
T_{LOSON}	Loss of Signal Detect on Timing	Loss of signal ON time. VIDS = 80 mV_{p-p}			100	µs
TIMING SPECIFICATIONS—Serializer, Low-Data-Rate Mode at 1.25 Gbps, EN_HDR = 0						
t_S	Setup Time *Figure 4*	TBC Falling Edge to TD[0–9] Valid	1.4			ns
t_H	Hold Time *Figure 4*	TBC Falling Edge to TD[0–9] Invalid	1.4			ns
f_{TBC}	TBC Frequency	At Line Date Rate of 1.0625 Gbps		106.25		MHz
		At Line Date Rate of 1.25 Gbps		125		MHz
TIMING SPECIFICATIONS—Serializer, High-Data-Rate Mode at 2.5 Gbps, EN_HDR = 1						
t_{VALID}	Valid Time *Figure 5*	TBC and TD[0–9] Valid	1.0			ns
t_{SK}	Edge Skew *Figure 5*	TBC and TD[0–9] Valid			1.5	ns
t_{TXCT}	Transition Time *Figure 5*	TBC or TD[0–9] Transition Time			3.0	ns
f_{TBC}	TBC Frequency	At Line Data Rate of 2.125 Gbps		106.25		MHz
		At Line Data Rate of 2.5 Gbps		125		MHz
TIMING SPECIFICATIONS—Deserializer, High-Data-Rate Mode at 2.5 Gbps, EN_RBC = 0						
t_S	Setup Time *Figure 6*	RBC1 or RBC0 Rising Edge to the Corresponding Data Word at RD[0–9] Valid	1.4			ns
t_H	Hold Time *Figure 6*	RBC1 or RBC0 Rising Edge to the Corresponding Data Word at RD[0–9] Invalid	1.4			ns
t_{DC}	Duty Cycle	RBC1 or RBC0 Duty Cycle	40		60	%
t_{A-B}	RBC Clock Skew *Figure 6*	Rising Edge of RBC1 to Rising Edge of RBC0	3.8		4.2	ns

Electrical Characteristics Over recommended operating supply and temperature ranges unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
TIMING SPECIFICATIONS — Deserializer, High-Data-Rate Mode at 2.5 Gbps, EN_RBC = 0						
f_{RBC}	RBC Frequency	At Line Date Rate of 2.125 Gbps		106.25		MHz
		At Line Date Rate of 2.5 Gbps		125		MHz
TIMING SPECIFICATIONS — Deserializer, Low-Data-Rate Mode at 1.25 Gbps, EN_RBC = 0						
t_S	Setup Time *Figure 6*	RBC1 Rising Edge to RD[0–9] Valid	3.0			ns
t_H	Hold Time *Figure 6*	RBC1 Rising Edge to RD[0–9] Invalid	3.0			ns
t_{DC}	Duty Cycle	RBC1 Duty Cycle	40		60	%
t_{A-B}	RBC Clock Skew *Figure 6*	Rising Edge of RBC1 to Rising Edge of RBC0	7.6		8.4	ns
f_{RBC}	RBC Frequency	At Line Date Rate of 1.0625 Gbps		53.125		MHz
		At Line Date Rate of 1.25 Gbps		62.5		MHz
TIMING SPECIFICATIONS — Deserializer, High-Data-Rate Mode at 2.5 Gbps, EN_RBC = 1						
t_S	Setup Time *Figure 7*	RBC1 Rising Edge to RD[0–9] Valid	1.4			ns
t_H	Hold Time *Figure 7*	RBC1 Rising Edge to RD[0–9] Invalid	1.4			ns
f_{RBC}	RBC Frequency	At High Data Rate (EN_HDR = 1) 2.125 Gbps		212.5		MHz
		At High Data Rate (EN_HDR = 1) 2.5 Gbps		250		MHz
t_{XRBC}	RBC Transition Time	V_{REF} – 0.25 V to V_{REF} + 0.25V	0.4	0.6	0.8	ns
t_X	Output Data Transition Time	For RD[0–9], CDET, LOS and ER pins. Measured between 20% and 80% Levels	0.6	1.0	1.5	ns
TIMING SPECIFICATIONS — Deserializer, Low-Data-Rate Mode at 1.25 Gbps, EN_RBC = 1						
t_S	Setup Time *Figure 7*	RBC1 Rising Edge to RD[0–9] Valid	3.0			ns
t_H	Hold Time *Figure 7*	RBC1 Rising Edge to RD[0–9] Invalid	3.0			ns
f_{RBC}	RBC Frequency	At Low Data Rate (EN_HDR = 0) 1.0625 Gbps		106.25		MHz
		At Low Data Rate (EN_HDR = 0) 1.25 Gbps		125		MHz

Note 1: "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Typical parameters are measured at V_{DDQ} = 1.8 V, DV_{DD} = 1.8 V, V_{DDHS} = 2.5 V, V_{DDIO} = 2.5 V,V_{DDB} = 2.5 V, T_A = 25˚C. They are for reference purposes, and are not production-tested.

Note 3: Duty cycle is defined as high period (t_{WH}) or low period (t_{WL}) ratio to clock period (t_{WH} + t_{WL}), measured at 50% of the differential voltage across REFCLK+ and REFCLK–.

Note 4: K28.5 is a repeating periodic pattern (hex: 283, 17C - bin: 110000 0101, 001111 1010). D21.5 is a repeating periodic pattern (hex: 155 - bin: 1010101010).

RPAT is a random data pattern with valid 8b/10b data codes of K28.5, K28.5, D3.1, D7.2, D11.3, D15.4, D19.5, D23.6, D27.7, D20.0, D21.1, D25.2 (hex: 283, 283, 263, 2B8, 30B, 2C5, 153, 197, 1E4, 0B4, 255, 299).

Note 5: Output Jitter and Jitter Tolerance are measured through characterization on sample basis. They are not production-tested. Output jitter is measured at a sample size of TBD. REFCLK± differential amplitude is 1.2 V_{p-p} with jitter of 3 ps (rms) or 25 ps (pk-pk) for Tx output jitter testing.

AC Timing Diagrams

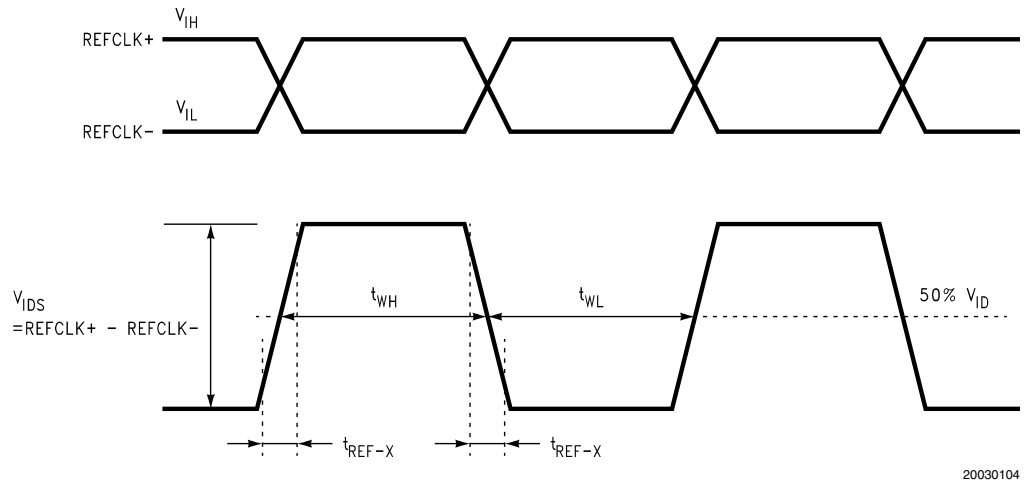


FIGURE 1. REFCLK Timing

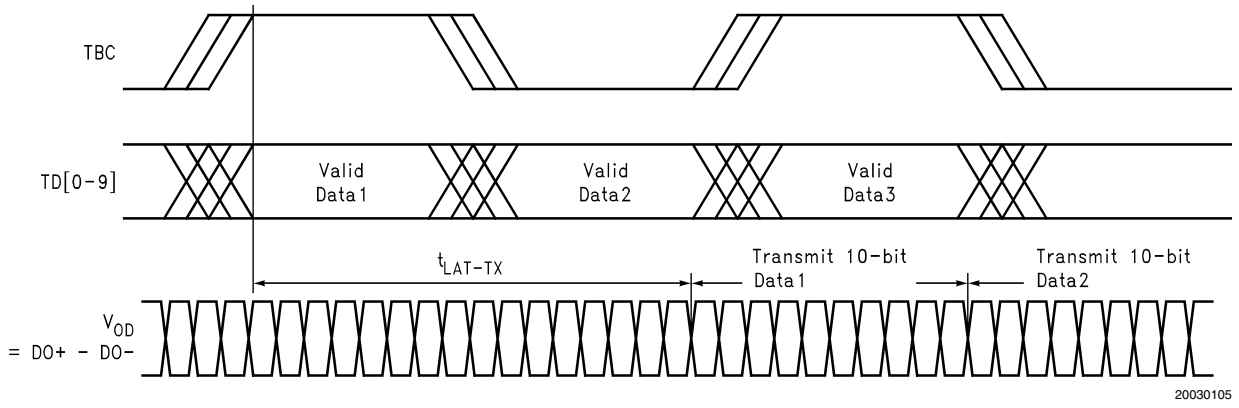


FIGURE 2. Transmit Latency (High Data Rate Mode)

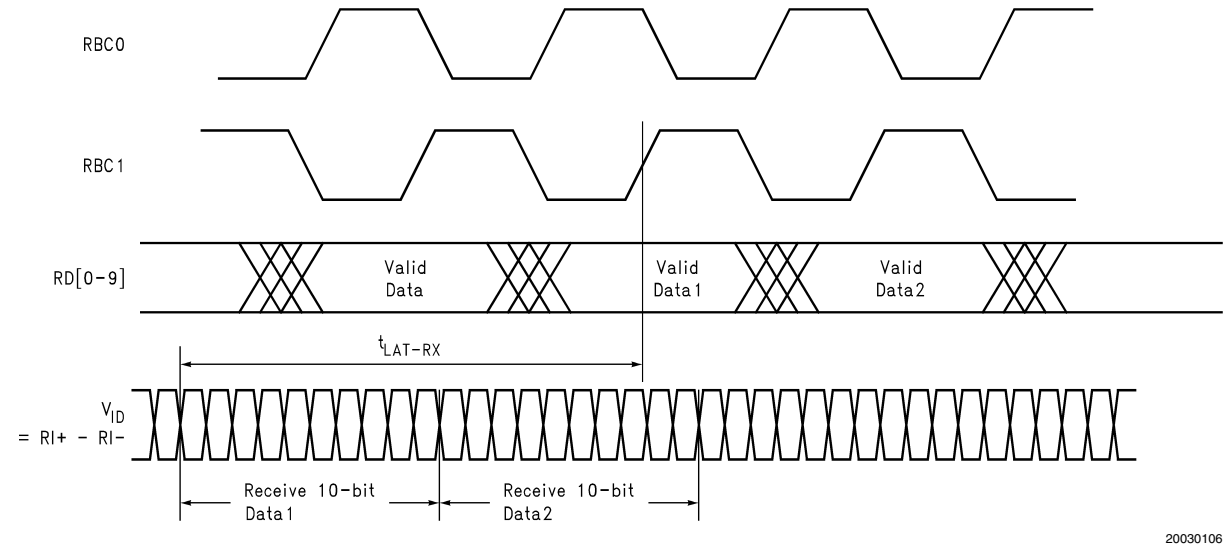


FIGURE 3. Receive Latency (EN_RBC = 1)

AC Timing Diagrams (Continued)

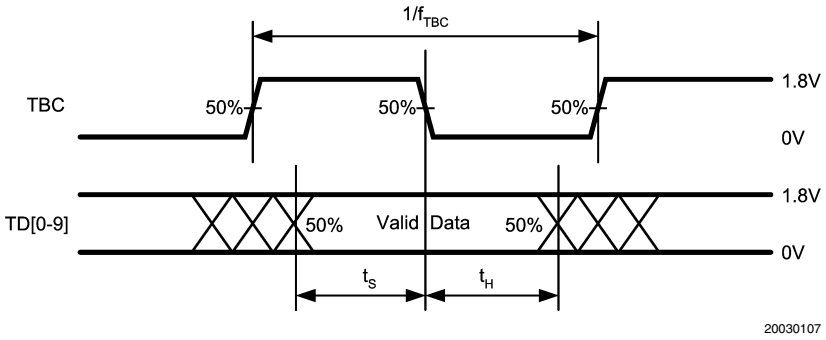


FIGURE 4. Transmit Input Data Bus Timing — Low Data Rate Mode

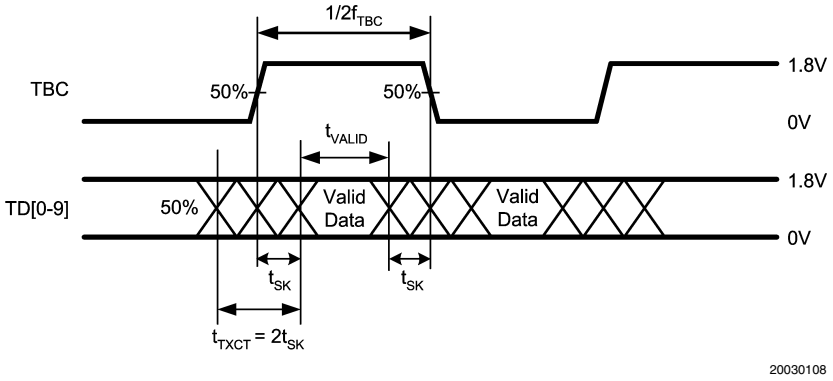


FIGURE 5. Transmit Input Data Timing — High Data Rate Mode

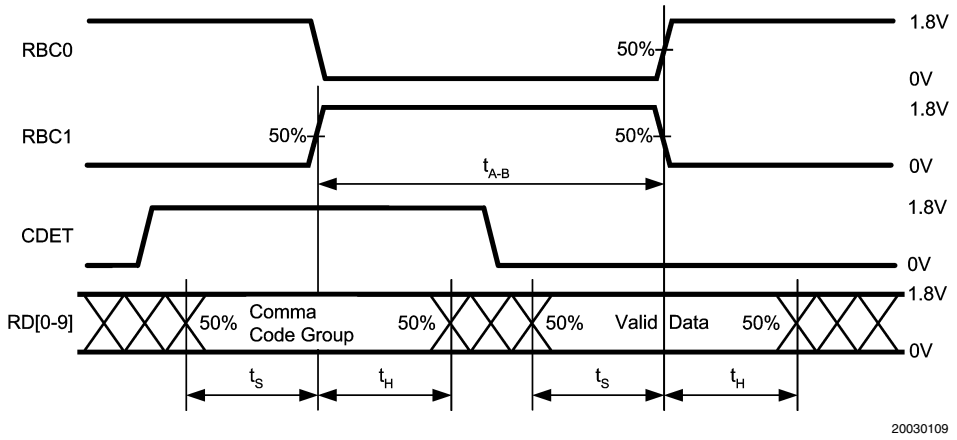


FIGURE 6. Receive Output Data Bus Timing — Low Data Rate or High Data Rate Mode (EN_RBC = 0)

AC Timing Diagrams (Continued)

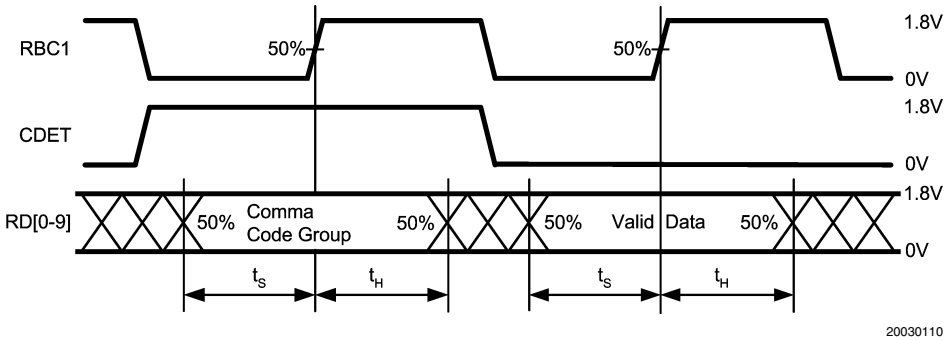


FIGURE 7. Receive Output Data Bus Timing—Low Data Rate or High Data Rate Mode (EN_RBC = 1)

Termination at the High Speed Interface

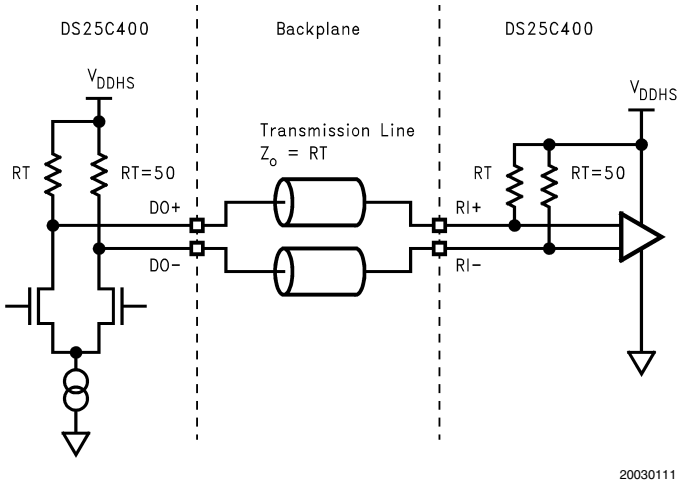


FIGURE 8. High Speed Interface — Direct-Coupled Mode (EN_RAC = 0)

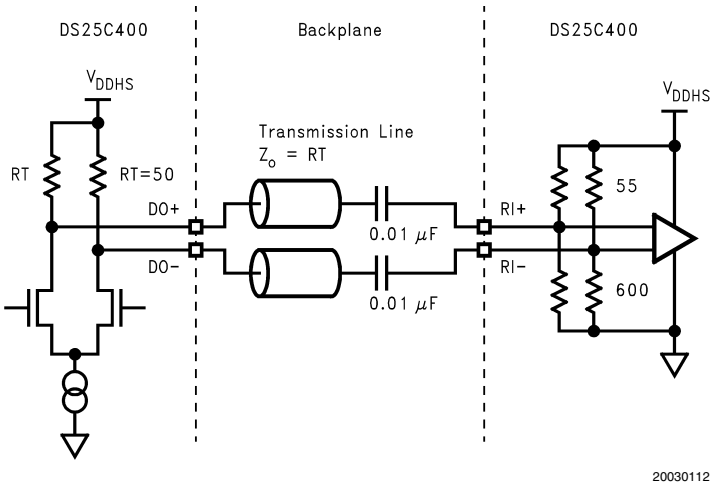


FIGURE 9. High Speed Interface — AC-Coupled Mode (EN_RAC = 1)

Termination at REFCLK

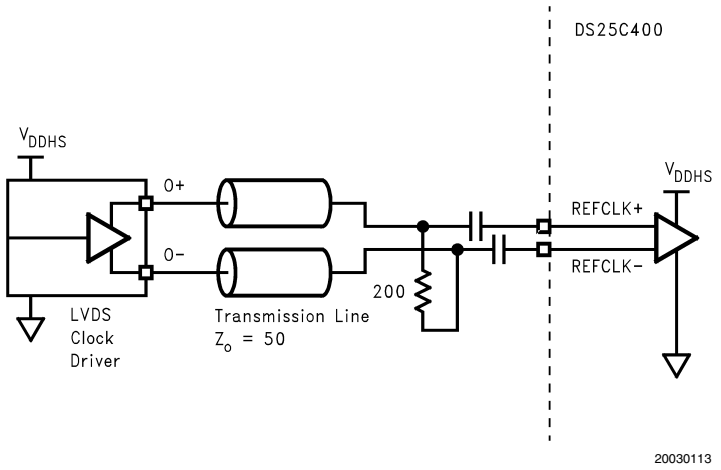


FIGURE 10. LVDS Terminations at REFCLK±

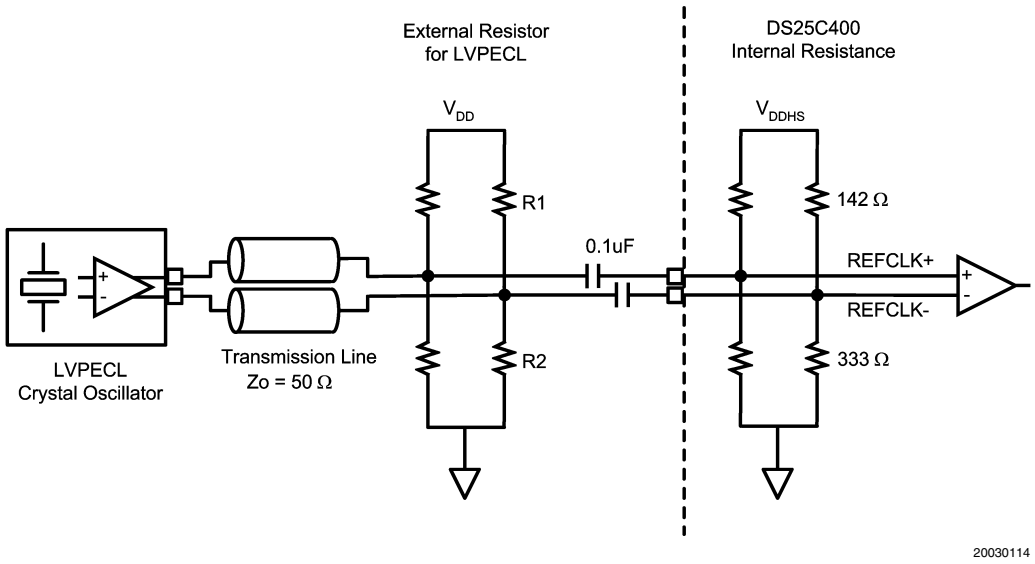


FIGURE 11. LVPECL Terminations at REFCLK±

The inputs to the DS25C400 have parallel termination resistors, thevenin equivalent to 100Ω single-ended. The value of R1 and R2 must be selected such that $V_T = V_{DD} - 2V$ and that the equivalent resistance is also 100Ω single-ended.

Termination values for different V_{DD} supply voltages:

For V_{DD} = 2.5V; R1 = 500 Ω; R2 = 125.5 Ω

For V_{DD} = 3.3V; R1 = 253 Ω; R2 = 165 Ω

For V_{DD} = 5.0V; R1 = 167 Ω; R2 = 250 Ω

Termination at the Parallel I/O Interface

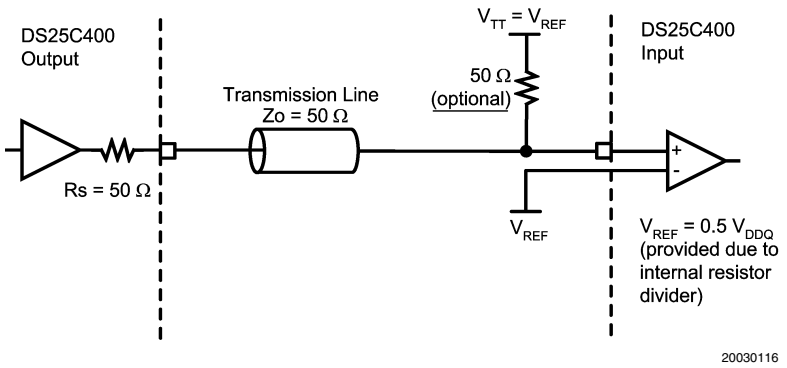


FIGURE 12. SSTL_18 Class 1, 1.8V HSTL or 1.8V LVCMOS I/O Termination

Pin Diagram

DS25C400TUT: 324-ball TE-PBGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	DGND	DGND	RD_A(9)	DGND	V_{DDQ}	RD_A[2]	RBC0_A	TBC_A	DGND	V_{DDQ}	TD_A(3)	AGND	V_{DDHS}	REFCLK−	REFCLK+	EN_RAC	RES3	LOS_C	EQ0_C	V_{DDHS}	EQ1_A	EQ0_A	A
B	DGND	V_{DDQ}	V_{REF1}	RD_A[8]	RD_A[5]	RD_A[1]	CDET_A	TD_A(9)	TD_A(6)	TD_A(4)	TD_A(2)	RES13	RES12	AGND	EN_PTN0	V_{DDHS}	AGND	LOS_B	EQ0_D	EQ1_B	EQ0_B	AGND	B
C	RD_B[9]	RD_B[8]	V_{DDQ}	RD_A[7]	RD_A[4]	DGND	V_{DDQ}	TD_A(8)	DGND	DGND	TD_A(1)	EN_LOS	EN_SLB	EN_PLB	EN_PTN1	EN_HDR	EN_CDET	LOS_A	EQ1_C	AGND	AGND	V_{DDHS}	C
D	V_{DDQ}	RD_B[7]	RD_B[6]	RD_A[6]	RD_A[3]	RD_A[0]	RBC1_A	TD_A(7)	TD_A(5)	V_{DDIO}	TD_A(0)	AGND	RES2	EN_10B	EN_ERR	EN_RBC	LOS_D	EQ1_D	RES4	DO_A+	V_{DDHS}	V_{DDHS}	D
E	RD_B[5]	DGND	RD_B[4]	RD_B[3]															AGND	DO_A−	DGND	RI_A+	E
F	RD_B[2]	V_{DDQ}	RD_B[1]	RD_B[0]															DGND	DV_{DD}	DV_{DD}	RI_A−	F
G	RBC0_B	TBC_B	CDET_B	RBC1_B															V_{DDHS}	RES8	V_{DDHS}	V_{DDHS}	G
H	TD_B[9]	TD_B[8]	DGND	TD_B[7]															AGND	RES9	AGND	RI_B−	H
J	TD_B[6]	TD_B[5]	V_{DDQ}	DGND					DGND	DGND	DGND	AGND	AGND	AGND					DGND	DV_{DD}	DV_{DD}	RI_B+	J
K	V_{DDIO}	TD_B[4]	TD_B[3]	TD_B[2]					DGND	DGND	DGND	AGND	AGND	AGND					DGND	DO_B−	V_{DDHS}	AGND	K
L	V_{DDQ}	TD_B[1]	TD_B[0]	DGND					DGND	DGND	DGND	AGND	AGND	AGND					AGND	DO_B+	AGND	RES5	L
M	DGND	TD_C[1]	TD_C[0]	V_{DDQ}					DGND	DGND	DGND	AGND	AGND	AGND					V_{DDHS}	DO_C+	AGND	RES6	M
N	TD_C[4]	TD_C[3]	TD_C[2]	V_{DDIO}					DGND	DGND	DGND	AGND	AGND	AGND					DGND	DO_C−	V_{DDHS}	AGND	N
P	TD_C[6]	TD_C[5]	V_{DDQ}	DGND					DGND	DGND	DGND	AGND	AGND	AGND					DGND	DV_{DD}	DV_{DD}	RI_C+	P
R	TD_C[9]	TD_C[8]	DGND	TD_C[7]															AGND	RES10	AGND	RI_C−	R
T	V_{DDQ}	TBC_C	CDET_C	RBC1_C															V_{DDHS}	RES11	V_{DDHS}	V_{DDHS}	T
U	DGND	RBC0_C	RD_C[1]	RD_C[0]															DGND	DV_{DD}	DV_{DD}	RI_D−	U
V	RD_C[4]	RD_C[3]	V_{DDQ}	RD_C[2]															AGND	DO_D−	DGND	RI_D+	V
W	DGND	RD_C[6]	DGND	RD_C[5]	RD_D[2]	RD_D[0]	TBC_D	TD_D[6]	DGND	TD_D[2]	PD1	RTERM	RBIASRX	ER_B	PSEL0_A	PSEL1_B	PSEL0_C	RES21	RES7	DO_D+	V_{DDHS}	V_{DDHS}	W
Y	RD_C[9]	RD_C[8]	RD_C[7]	RD_D[5]	RD_D[3]	V_{DDQ}	DGND	TD_D[7]	V_{DDIO}	TD_D[3]	V_{DDQ}	DGND	V_{DDB}	RBIASTX	ER_C	DGND	V_{DDQ}	RES23	RES17	AGND	AGND	V_{DDHS}	Y
AA	V_{DDQ}	RD_D[9]	RD_D[7]	RD_D[6]	RD_D[4]	RBC0_D	CDET_D	TD_D[8]	TD_D[5]	TD_D[4]	TD_D[0]	PD0	V_{DDQ}	DGND	ER_A	PSEL1_A	PSEL1_C	PSEL0_D	RES16	RES19	RES20	AGND	AA
AB	DGND	V_{REF2}	RD_D[8]	V_{DDQ}	DGND	RD_D[1]	RBC1_D	TD_D[9]	V_{DDQ}	DGND	TD_D[1]	DGND	RTERM_RTN	RBIAS_RTN	RES1	ER_D	PSEL0_B	PSEL1_D	RES15	RES18	RES22	DGND	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

20030103

Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
DO_A+ DO_A–	D20 E20	O, CML	Inverting and non-inverting high speed CML differential outputs of the serializer, channel A. On-chip termination resistors connect from DO_A+ and DO_A– to V_{DDHS}.
DO_B+ DO_B–	L20 K20	O, CML	Inverting and non-inverting high speed CML differential outputs of the serializer, channel B. On-chip termination resistors connect from DO_B+ and DO_B– to V_{DDHS}.
DO_C+ DO_C–	M20 N20	O, CML	Inverting and non-inverting high speed CML differential outputs of the serializer, channel C. On-chip termination resistors connect from DO_C+ and DO_C– to V_{DDHS}.
DO_D+ DO_D–	W20 V20	O, CML	Inverting and non-inverting high speed CML differential outputs of the serializer, channel D. On-chip termination resistors connect from DO_D+ and DO_D– to V_{DDHS}.
RI_A+ RI_A–	E22 F22	I, CML	Inverting and non-inverting high speed differential inputs of the deserializer, channel A. On-chip termination resistors connect from RI_A+ and RI_A– to V_{DDHS}.
RI_B+ RI_B–	J22 H22	I, CML	Inverting and non-inverting high speed differential inputs of the deserializer, channel B. On-chip termination resistors connect from RI_B+ and RI_B– to V_{DDHS}.
RI_C+ RI_C–	P22 R22	I, CML	Inverting and non-inverting high speed differential inputs of the deserializer, channel C. On-chip termination resistors connect from RI_C+ and RI_C– to V_{DDHS}.
RI_D+ RI_D–	V22 U22	I, CML	Inverting and non-inverting high speed differential inputs of the deserializer, channel D. On-chip termination resistors connect from RI_D+ and RI_D– to V_{DDHS}.
DIFFERENTIAL REFERENCE CLOCK			
REFCLK+ REFCLK–	A15 A14	I, CML or AC coupled inputs	Inverting and non-inverting differential reference clock to the clock synthesizers for clock generation. A low jitter clock source should be connected to REFCLK±. The REFCLK± is shared by all four channels.
PARALLEL I/O DATA			
TD_A[0] TD_A[1] TD_A[2] TD_A[3] TD_A[4] TD_A[5] TD_A[6] TD_A[7] TD_A[8] TD_A[9]	D11 C11 B11 A11 B10 D9 B9 D8 C8 B8	I, SSTL_18, Pull-Low	Transmit data word for channel A. In the 10-bit mode, the 10-bit code-group at TD_A[0–9] is serialized with the internal 8b/10b encoder disabled. Bit 9 is the MSB. In the 8-bit mode, TD_A[0–7] is first converted into 10-bit code-group by the internal 8b/10b encoder before it is serialized. Bit 7 is the MSB. TD_A[8] is used as K-code select pin. When TD_A[8] is low, TD_A[0–7] is mapped to the corresponding 10-bit D-group. When TD_A[8] is high, TD_A[0–7] is mapped to the corresponding 10-bit K-group. The 8b/10b code group conversion is implemented in according to 802.3z standard.
TD_B[0] TD_B[1] TD_B[2] TD_B[3] TD_B[4] TD_B[5] TD_B[6] TD_B[7] TD_B[8] TD_B[9]	L3 L2 K4 K3 K2 J2 J1 H4 H2 H1	I, SSTL_18, Pull-Low	Transmit data word for channel B. In the 10-bit mode, the 10-bit code-group at TD_B[0–9] is serialized with the internal 8b/10b encoder disabled. Bit 9 is the MSB. In the 8-bit mode, TD_B[0–7] is first converted into 10-bit code-group by the internal 8b/10b encoder before it is serialized. Bit 7 is the MSB. TD_B[8] is used as K-code select pin. When TD_B[8] is low, TD_B[0–7] is mapped to the corresponding 10-bit D-group. When TD_B[8] is high, TD_B[0–7] is mapped to the corresponding 10-bit K-group.

Pin Descriptions (Continued)

Pin Name	Pin #	I/O, Type	Description
PARALLEL I/O DATA			
TD_C[0] TD_C[1] TD_C[2] TD_C[3] TD_C[4] TD_C[5] TD_C[6] TD_C[7] TD_C[8] TD_C[9]	M3 M2 N3 N2 N1 P2 P1 R4 R2 R1	I, SSTL_18, Pull-Low	Transmit data word for channel C. In the 10-bit mode, the 10-bit code-group at TD_C[0–9] is serialized with the internal 8b/10b encoder disabled. Bit 9 is the MSB. In the 8-bit mode, TD_C[0–7] is first converted into 10-bit code-group by the internal 8b/10b encoder before it is serialized. Bit 7 is the MSB. TD_C[8] is used as K-code select pin. When TD_C[8] is low, TD_C[0–7] is mapped to the corresponding 10-bit D-group. When TD_C[8] is high, TD_C[0–7] is mapped to the corresponding 10-bit K-group.
TD_D[0] TD_D[1] TD_D[2] TD_D[3] TD_D[4] TD_D[5] TD_D[6] TD_D[7] TD_D[8] TD_D[9]	AA11 AB11 W10 Y10 AA10 AA9 W8 Y8 AA8 AB8	I, SSTL_18, Pull-Low	Transmit data word for channel D. In the 10-bit mode, the 10-bit code-group at TD_D[0–9] is serialized with the internal 8b/10b encoder disabled. Bit 9 is the MSB. In the 8-bit mode, TD_D[0–7] is first converted into 10-bit code-group by the internal 8b/10b encoder before it is serialized. Bit 7 is the MSB. TD_D[8] is used as K-code select pin. When TD_D[8] is low, TD_D[0–7] is mapped to the corresponding 10-bit D-group. When TD_D[8] is high, TD_D[0–7] is mapped to the corresponding 10-bit K-group.
TBC_A	A8	I, SSTL_18, Pull-Low	Transmit byte clock for channel A.
TBC_B	G2	I, SSTL_18, Pull-Low	Transmit byte clock for channel B.
TBC_C	T2	I, SSTL_18, Pull-Low	Transmit byte clock for channel C.
TBC_D	W7	I, SSTL_18, Pull-Low	Transmit byte clock for channel D.
RD_A[0] RD_A[1] RD_A[2] RD_A[3] RD_A[4] RD_A[5] RD_A[6] RD_A[7] RD_A[8] RD_A[9]	D6 B6 A6 D5 C5 B5 D4 C4 B4 A3	O, SSTL_18	Deserialized receive data word for channel A. In the 10-bit mode, RD_A[0–9] is the deserialized received data word in 10-bit code group. Bit 9 is the MSB. In the 8-bit mode, RD_A[0–7] is the deserialized received data byte. Bit 7 is the MSB. RD_A[9] is the 8b/10b error monitor. RD_A[8] is the K-group indicator. A low at RD_A[8] indicates RD_A[0–7] belongs to the D-group, while a high indicates it belongs to the K-group.
RD_B[0] RD_B[1] RD_B[2] RD_B[3] RD_B[4] RD_B[5] RD_B[6] RD_B[7] RD_B[8] RD_B[9]	F4 F3 F1 E4 E3 E1 D3 D2 C2 C1	O, SSTL_18	Deserialized receive data word for channel B. In the 10-bit mode, RD_B[0–9] is the deserialized received data word in 10-bit code group. Bit 9 is the MSB. In the 8-bit mode, RD_B[0–7] is the deserialized received data byte. Bit 7 is the MSB. RD_B[9] is the 8b/10b error monitor. RD_B[8] is the K-group indicator. A low at RD_B[8] indicates RD_B[0–7] belongs to the D-group, while a high indicates it belongs to the K-group.

Pin Descriptions (Continued)

Pin Name	Pin #	I/O, Type	Description
PARALLEL I/O DATA			
RD_C[0] RD_C[1] RD_C[2] RD_C[3] RD_C[4] RD_C[5] RD_C[6] RD_C[7] RD_C[8] RD_C[9]	U4 U3 V4 V2 V1 W4 W2 Y3 Y2 Y1	O, SSTL_18	Deserialized receive data word for channel C. In the 10-bit mode, RD_C[0–9] is the deserialized received data word in 10-bit code group. Bit 9 is the MSB. In the 8-bit mode, RD_C[0–7] is the deserialized received data byte. Bit 7 is the MSB. RD_C[9] is the 8b/10b error monitor. RD_C[8] is the K-group indicator. A low at RD_C[8] indicates RD_C[0–7] belongs to the D-group, while a high indicates it belongs to the K-group.
RD_D[0] RD_D[1] RD_D[2] RD_D[3] RD_D[4] RD_D[5] RD_D[6] RD_D[7] RD_D[8] RD_D[9]	W6 AB6 W5 Y5 AA5 Y4 AA4 AA3 AB3 AA2	O, SSTL_18	Deserialized receive data word for channel D. In the 10-bit mode, RD_D[0–9] is the deserialized received data word in 10-bit code group. Bit 9 is the MSB. In the 8-bit mode, RD_D[0–7] is the deserialized received data byte. Bit 7 is the MSB. RD_D[9] is the 8b/10b error monitor. RD_D[8] is the K-group indicator. A low at RD_D[8] indicates RD_D[0–7] belongs to the D-group, while a high indicates it belongs to the K-group.
RBC0_A RBC1_A	A7 D7	O, SSTL_18	Complementary receive byte clocks for channel A.
RBC0_B RBC1_B	G1 G4	O, SSTL_18	Complementary receive byte clocks for channel B.
RBC0_C RBC1_C	U2 T4	O, SSTL_18	Complementary receive byte clocks for channel C.
RBC0_D RBC1_D	AA6 AB7	O, SSTL_18	Complementary receive byte clocks for channel D.
V_{REF1} V_{REF2}	B3 AB2	O, Analog	SSTL_18 reference voltages. Generated internally by a resistive divider from V_{DDQ} to DGND. A X7R 0.01 µF bypass capacitor should be connected from each V_{REF} pin to GND plane.
LINE STATUS			
LOS_A LOS_B LOS_C LOS_D	C18 B18 A18 D17	O, LVCMOS O, LVCMOS O, LVCMOS O, LVCMOS	Signal detector output. 0 = Signal level at RI± above signal detector's ON threshold. 1 = Signal level at RI± below signal detector's OFF threshold.
CDET_A CDET_B CDET_C CDET_D	B7 G3 T3 AA7	O, SSTL_18 O, SSTL_18 O, SSTL_18 O, SSTL_18	Comma Detected. Logic high at CDET indicates that the internal Comma Detector detects a Comma bit sequence from the incoming bit stream. The serial to parallel converter is aligned to the proper 10-bit word boundary.
ER_A ER_B ER_C ER_D	AA15 W14 Y15 AB16	O, SSTL_18 O, SSTL_18 O, SSTL_18 O, SSTL_18	PRBS Error when EN_ERR is low, 8b/10b disparity or code violation error when EN_ERR is high. Upon detection of an error, ER will go high for one word period.
BIAS REFERENCE			
RTERM RTERM_RTN	W12 AB13	I, Analog I, Analog	An external resistor is connected from RTERM to RTERM_RTN for use as reference to control process variation of the internal on-chip terminations. An external resistor of 249Ω ±1% provides an on-chip termination of 50Ω ±10%.

Pin Descriptions (Continued)

Pin Name	Pin #	I/O, Type	Description
BIAS REFERENCE			
RbiasTx RbiasRx RBIAS_RTN	Y14 W13 AB14	I, Analog I, Analog I, Analog	An external resistor is connected from RbiaxTx to RBIAS_RTN to set up the proper internal bias Tx current. An external resistor is connected from RbiasRx to RBIAS_RTN to set up the proper internal bias Rx current. The external resistor should be 6.3 kΩ ±1%.
CONFIGURATION CONTROL—AFFECT ALL FOUR CHANNELS			
EN_CDET	C17	I, CMOS, Pull-High	Enable Comma Detector to align the correct bit boundary of the 10-bit word. 1 = Enables Comma Detector. 0 = Disable Comma Detector.
EN_10B	D14	I, CMOS, Pull-High	Enable 10-bit mode. 1 = Selects 10-bit mode. Disables internal 8b/10b encoder and decoder. 0 = Selects 8-bit mode. Enables the internal 8b/10b encoder and decoder.
EN_HDR	C16	I, CMOS, Pull-High	0 = Selects low-data-rate mode for the serdes. 1 = Selects high-data-rate mode for the serdes.
EN_RBC	D16	I, CMOS, Pull-Low	0 = RBC1 and RBC0 strobe even and odd data word at RD[0–9]. 1 = Data words at RD[0–9] are strobed by RBC1.
EN_RAC	A16	I, CMOS, Pull-High	0 = Connects internal CML input 50Ω terminations from RI+ and RI− to V_{DDHS}. 1 = Configure internal termination resistors to form an internal bias network for RI+ and RI− when AC coupling is used. The divider forms a parallel termination of 50Ω. Please refer to *Figures 8, 9*.
EN_PLB	C14	I, CMOS, Pull-Low	Local parallel loopback from TD[0–9] to RD[0–9] have been removed and only serial local loopback is functional. User should tie this pin to DGND or leave open.
EN_SLB	C13	I, CMOS, Pull-Low	Local serial loopback. 1 = Enables internal local serial loopback. 0 = Disables internal local serial loopback.
EN_LOS	C12	I, CMOS, Pull-Low	Loss Of Signal Output Control 0 = enables the LOS output control of RD[0-9] (output will be pull-high when LOS is detected) 1 = disable the LOS output control of RD[0-9] (output will not be pull-high).
EN_PTN1 EN_PTN0	C15 B15	I, CMOS, Pull-Low	Select internal test pattern generator. EN_PTN1 EN_PTN0 0 0: Disable internal test pattern generator for normal operation. 0 1: Enable internal PRBS = 2^7–1 pattern generator. 1 0: Enable D21.5 - Alterating 1_0 pattern. 1 1: Enable repeating K28.5 pattern.
EN_ERR	D15	I, CMOS, Pull-Low	Enable and synchronize the internal PRBS error checker in the receivers, and select types of errors detected. 0 = Enables internal PRBS error checker. Receiver expects pseudo-random pattern (2^7 – 1) bit stream. ER_n pin only reports any PRBS error detected. EN_ERR must be pulsed high then low with a minimum pulse period of 10 µs to synchronize the internal PRBS checker. 1 = Disable internal PRBS error checker for normal operation. ER_n pin only reports 8b/10b code error or disparity error detected.

Pin Descriptions (Continued)

Pin Name	Pin #	I/O, Type	Description
CONFIGURATION CONTROL—AFFECT INDIVIDUAL CHANNEL			
PSEL0_A PSEL1_A	W15 AA16	I, CMOS, Pull-Low	Pre-emphasis select for channel A CML driver. Select one of the three pre-emphasis current-drive settings for output drivers. See Functional Description. PSEL0_A and PSEL1_A should be tied to DGND if no pre-emphasis is needed.
PSEL0_B PSEL1_B	AB17 W16	I, CMOS, Pull-Low	Pre-emphasis select for channel B CML driver. Select one of the three pre-emphasis current-drive settings for output drivers. See Functional Description. PSEL0_B and PSEL1_B should be tied to DGND if no pre-emphasis is needed.
PSEL0_C PSEL1_C	W17 AA17	I, CMOS, Pull-Low	Pre-emphasis select for channel C CML driver. Select one of the three pre-emphasis current-drive settings for output drivers. See Functional Description. PSEL0_C and PSEL1_C should be tied to DGND if no pre-emphasis is needed.
PSEL0_D PSEL1_D	AA18 AB18	I, CMOS, Pull-Low	Pre-emphasis select for channel D CML driver. Select one of the three pre-emphasis current-drive settings for output drivers. See Functional Description. PSEL0_D and PSEL1_D should be tied to DGND if no pre-emphasis is needed.
EQ0_A EQ1_A	A22 A21	I, CMOS, Pull-Low	Receive equalization select for channel A. Select one of the three equalization filters to compensate for transmission medium's frequency response. See Functional Description. EQ0_A and EQ1_A should be tied to DGND if no equalization is needed.
EQ0_B EQ1_B	B21 B20	I, CMOS, Pull-Low	Receive equalization select for channel B. Select one of the three equalization filters to compensate for transmission medium's frequency response. See Functional Description. EQ0_B and EQ1_B should be tied to DGND if no equalization is needed.
EQ0_C EQ1_C	A19 C19	I, CMOS, Pull-Low	Receive equalization select for channel C. Select one of the three equalization filters to compensate for transmission medium's frequency response. See Functional Description. EQ0_C and EQ1_C should be tied to DGND if no equalization is needed.
EQ0_D EQ1_D	B19 D18	I, CMOS, Pull-Low	Receive equalization select for channel D. Select one of the three equalization filters to compensate for transmission medium's frequency response. See Functional Description. EQ0_D and EQ1_D should be tied to DGND if no equalization is needed.
PD0 PD1	AA12 W11	I, CMOS, Pull-Low	Power down control signals. PD1 PD0 0 0 All 4 channels powered down 0 1 Only Channel A powered up 1 0 Channels A and B powered up 1 1 All 4 channels powered up
RESERVED TEST PINS			
RES1	AB15	I, CMOS, Pull-Low	Loop filter test points. User should tie this pin to DGND or leave open.
RES2	D13	I, CMOS, Pull-Low	Termination resistor calibration. User should tie this pin to DGND or leave open.
RES3	A17	I, CMOS, Pull-Low	REFCLK rate select. User should tie this pin to DGND or leave open.

Pin Descriptions (Continued)

Pin Name	Pin #	I/O, Type	Description
RESERVED TEST PINS			
RES4 RES5 RES6 RES7 RES8 RES9 RES10 RES11	D19 L22 M22 W19 G20 H20 R20 T20	O, Analog	Loop filter test points. Leave open (no connection).
RES12	B13	I, CMOS, Pull-Low	User should tie this pin to DGND or leave open.
RES13	B12	I, CMOS, Pull-Low	User should tie this pin to DGND or leave open.
RES15	AB19	I, CMOS, Pull-Low	Leave open (no connection).
RES16	AA19	I, CMOS, Pull-Low	Leave open (no connection).
RES17	Y19	I, CMOS, Pull-Low	Leave open (no connection).
RES18	AB20	I, CMOS, Pull-Low	Leave open (no connection).
RES19	AA20	I, CMOS, Pull-Low	Leave open (no connection).
RES20	AA21	I, Power/ I, CMOS, Pull-High	User should tie this pin to D_{VDD} or leave open.
RES21	W18	I, Power/ I, CMOS, Pull-High	User should tie this pin to D_{VDD} or leave open.
RES22	AB21	I, Power/ I, CMOS, Pull-High	Leave open (no connection).
RES23	Y18	I, Power/ I, CMOS, Pull-High	Leave open (no connection).
POWER			
V_{DDQ}	B2, C3, D1, F2, J3, L1, M4, P3, T1, V3, AA1, AB4, Y6, AB9, Y11, AA13, Y17, A10, C7, A5	I, Power	V_{DDQ} = 1.8V ±5%. It powers the SSTL interface. A X7R 0.01 µF bypass capacitor should be connected from each V_{DDQ} pin to DGND plane.
D_{VDD}	U20, U21, P20, P21, J20, J21, F20, F21	I, Power	D_{VDD} = 1.8V ±5%. Power to internal logic. A X7R 0.01 µF bypass capacitor should be connected from each D_{VDD} pin to DGND plane.

Pin Descriptions (Continued)

Pin Name	Pin #	I/O, Type	Description
POWER			
V_{DDHS}	Y22, W21, W22, T19, T21, T22, N21, M19, K21, G19, G21, G22, D21, D22, C22, A20, B16, A13	I, Power	V_{DDHS} = 2.5V ±5%. It powers the high speed CML I/O circuitry, the analog PLL circuitry, and reference clock buffer. A X7R 0.01 µF bypass capacitor should be connected from each V_{DDHS} pin to AGND plane.
V_{DDIO}	K1, N4, Y9, D10	I, Power	V_{DDIO} = 2.5V ±5%. Power to Parallel I/O input buffers. A X7R 0.01 µF bypass capacitor should be connected from each V_{DDIO} pin to DGND plane.
V_{DDB}	Y13	I, Power	V_{DDB} = 2.5V ±5%. Power to BIAS circuit. A X7R 0.01 µF bypass capacitor should be connected from each V_{DDB} pin to DGND plane.
GROUND			
DGND	C10, J4, P4, W9, A1, B1, A2, E2, H3, L4, M1, R3, U1, W1, W3, AB1, AB5, Y7, AB10, Y12, AA14, Y16, AB22, A4, A9, C9, C6, AB12, V21, U19, P19, N19, K19, J19, F19, E21, J[9–11], K[9–11], L[9–11], M[9–11], N[9–11], P[9–11]	I, Ground	Digital ground pins. DGND should be tied to a solid ground plane through a low inductive path.

Pin Descriptions (Continued)

Pin Name	Pin #	I/O, Type	Description
GROUND			
AGND	A12, B14, B17, B22, C20, C21, D12, E19, H19, H21, K22, L19, L21, M21, N22, R19, R21, V19, Y20, Y21, AA22, J[12–14], K[12–14], L[12–14], M[12–14], N[12–14], P[12–14]	I, Ground	Analog ground pins. AGND should be tied to a solid ground plane through a low inductive path.

Note:
I = Input
O = Output
Pull-Low = input pin is pulled-low by an internal resistor.
Pull-High = input pin is pulled-high by an internal resistor.

Functional Descriptions

The serial interface is optimized for backplane applications with user selectable pre-emphasis at driver and/or equalization filters at receivers. A typical point-to-point backplane link consists of two high-speed connectors (such as Teradyne HSD family) and 20 inches 100Ω coupled differential traces usually implemented with strip-lines on FR4 or Getek board material.

REFERENCE CLOCK

Each of the four serializers is clocked by a high speed clock derived from its own internal low jitter clock synthesizer, which is phase-locked to the input clock at REFCLK±. No external components are required for the clock synthesizing PLL's. REFCLK± should be a differential CML, or AC coupled differential clock. Any termination resistors should be located close to the REFCLK± input pins. REFCLK± should be connected to a balanced differential clock from a crystal source or clock driver.

The clock synthesizers are low pass in nature. REFCLK jitter above 10 MHz will be attenuated by the Tx PLL. Any low frequency jitter component at REFCLK± will be transferred directly to DO±. The Tx output jitter specification is relaxed below a frequency of bit rate/1,667 because the Rx PLL can track very low frequency jitter. To ensure good output jitter performance, REFCLK should be free from excessive low frequency jitter and have random jitter less than 30–40 ps p-p. The REFCLK± input amplitude should be a minimum of 1 V_{p-p} differential for the best Tx output jitter performance.

The reference clock input has an internal bias network that sets its common mode voltage to 1.75V. The REFCLK differential input impedance is 200Ω. To terminate into 100Ω differential, an additional external 200Ω termination impedance is required. If the common mode voltage of the driver does not match the REFCLK common mode voltage coupling capacitors can be used to remove the driver DC voltage. This AC coupled mode allows the REFCLK to be interfaced to LVDS, PECL, LVPECL, LVEP, PECL, and other differential logic levels. See *Figures 10, 11*.

The frequency range of REFCLK± is 106.25 - 125 MHz to support data rate of 1.0625 - 1.25 Gbps or 2.125 - 2.5 Gbps at high data rate mode. The frequency accuracy should be better than ±100 ppm.

REFCLK (RES3=0)	Transmit and Receive Data Rate (Low Data Rate Mode, EN_HDR=0)	Transmit and Receive Data Rate (High Data Rate Mode, EN_HDR=1)
106.25 MHz	1.0625 Gbps	2.125 Gbps
125.00 MHz	1.25 Gbps	2.500 Gbps

TRANSMIT PARALLEL INPUT DATA

Each serializer accepts parallel transmit data at TD[0–9], clocked in by an input clock TBC. TBC must be synchronized to REFCLK ±100 ppm. An input FIFO is used to compensate for the phase difference between TBC and the internal byte clock that samples TD[0–9].

When the 8-bit mode is enabled (EN_10B=0), an internal 8b/10b encoder is activated to convert TD[0–8] into the corresponding 10-bit code group. TD[0–7] is the data byte, while TD[8] is used as the D-group or K-group qualifier.

Functional Descriptions (Continued)

When 10-bit mode is used (EN_10B=1), the serializer expects coded 10-bit data at TD[0–9], with its internal 8b/10b encoder disabled.

The serializer can be configured in the high-data-rate mode or low-data-rate mode determined by EN_HDR pin. In the high-data-rate mode (EN_HDR=1), source-synchronous switching is used. TD[0–9] transitions are synchronous to both the rising and falling edges of TBC. The frequency of TBC is thus half the transfer rate frequency at TD[0–9]. See *Figure 5*.

In the low-data-rate mode, (EN_HDR=0), the serializer runs at half data rate. TD[0–9] is clocked in at the falling strobe edge of TBC. See *Figure 4*.

REFCLK (RES3=0)	TBC at Low-Data-Rate Mode (EN_TDR=0)	Transfer Rate at TD[0–9] = Line Rate / 10	Line Rate at DO±
106.25 MHz	106.25 MHz	106.25 Mword/s	1.0625 Gbps
125.0 MHz	125 MHz	125 Mword/s	1.25 Gbps

REFCLK (RES3=0)	TBC at High-Data-Rate Mode (EN_HDR=1)	Transfer Rate at TD[0–9] = Line Rate / 10	Line Rate at DO±
106.25 MHz	106.25 MHz	212.5 Mword/s	2.125 Gbps
125.0 MHz	125 MHz	250 Mword/s	2.50 Gbps

The internal 10-bit coded data word is serialized and clocked out at DO±. Bit 0 (LSB) of the 10-bit code-group is shifted out first.

TD[0–9] and TBC are single-ended SSTL logic. They expect input signal swing of 1.8V, and switch at approximately 0.9V.

TRANSMIT SERIAL DATA OUTPUT

The serialized data bit stream is output at DO±, driven by a differential current mode logic (CML) driver. Both DO+ and DO– are terminated with on-chip resistors to V_{DDHS}. The values of the internal termination resistors are tightly controlled to 50Ω ±10%.

With an external load of 50Ω to V_{DDHS} or AC coupled to GND, the driver provides single-ended voltage swing of 533 mV nominal, with a common mode voltage of about (V_{DDHS} –0.27V). To compensate against edge degradation due to bandwidth-limited transmission medium, the driver has 3 selectable steps of pre-emphasis providing additional current drive for one bit period following a data level transition. The pre-emphasis improves signal quality at the receiving end of the transmission medium and enhances error rate performance of the downstream receiver.

PSEL1	PSEL0	Descriptions
0	0	Pre-emphasis disabled. Drive current = 24 mA.
0	1	Pre-emphasis enabled. Drive current = 29.3 mA at first bit after data transition.
1	0	Pre-emphasis enabled. Drive current = 34.7 mA at first bit after data transition.
1	1	Pre-emphasis enabled. Drive current = 39.7 mA at first bit after data transition.

Note: The Pre-emphasis current is only applied to the load termination for the first bit after a data transition. However, the pre-emphasis current increases the power supply DC current by the same amount. For power and thermal calculations consideration must be paid to on chip vs. off chip power dissipation.

RECEIVE SERIAL DATA INPUT

The receiver front-end is a limiting amplifier with on-chip CML terminations from RI+ and RI– to V_{DDHS}. The values of the internal termination resistors are tightly controlled to 50Ω ±10%. The limiting amplifier is capable to work with minimum input differential voltage of 200 mV_{p-p} across RI+ and RI–.

When serial bit stream is AC coupled to RI±, the internal termination resistors can be configured as a divider to provide DC bias to RI+ and RI–, and form an equivalent 50Ω parallel termination. EN_RAC is set to logic high to enable the receiver's bias network.

SIGNAL DETECT

The signal detect circuit generates a Loss of Signal (LOS) to indicate the amplitude of incoming serial data is less than minimum level allowed by the link budget. Its purpose is to indicate a complete loss of signal such as a disconnected or broken cable. A poor quality link may provide enough signal for LOS to remain off, even though the signal level is non-compliant and the BER objective is not met. Hysteresis is used to so that the LOS output does not rapidly change state with small variations in received power. The lower bound is set high enough so that Near End Cross Talk (NEXT) will not cause a false signal detect. When the input differential voltage at RI± falls below 80 mV_{p-p} max, Loss of Signal Detect Indicator is turned on (LOS=1) to signal for invalid data transmission. RD[0–9] are forced high during loss of signal. Once LOS has gone high the input signal must reach the higher differential voltage of 200 mV (max) to indicate that the incoming signal is above the minimum level. Common control pin EN_LOS is a LOS output control pin. When EN_LOS = 1, the LOS circuit which control the RD[0-9] outputs are disabled. The RD[0-9] will not be forced high upon LOS detection.

EQUALIZATION

The receiver front-end provides 3 steps of equalization filter to improve the eye opening of the input data at RI±. The equalization filter is a first order, designed to equalize transmission loss and reduce ISI for long board traces in a backplane.

EQ1	EQ0	Descriptions
0	0	Equalization disabled
0	1	Equalization filter's zero location set at about 800 MHz
1	0	Equalization filter's zero location set at about 500 MHz

Functional Descriptions (Continued)

EQ1	EQ0	Descriptions
1	1	Equalization filter's zero location set at about 400 MHz

DESERIALIZER

The clock and data recovery PLL accepts serial NRZ re-shaped bit stream from the receiver front-end. It recovers clock from the incoming bit stream, and re-times the data. It is optimized to work with 10-bit coded bit stream to maintain DC balance and ensure enough edge transitions to maintain synchronization. The data rate of the PLL can be 2.125 - 2.5 Gbps or 1.0625 - 1.25 Gbps determined by REFCLK± and EN_HDR. In the absence of input bit stream, the PLL is centered to the internal local transmit clock. It is capable to re-time data with maximum frequency tolerance of ±200 ppm from its local transmit clock. No external component is needed for the PLL.

The re-timed bit stream is deserialized into 10-bit word clocked by the recovered clock. In the 10-bit mode (EN_10B=1), the parallel recovered data code-group is output at RD[0–9]. In the 8-bit mode (EN_10B=0), the internal 8b/10b decoder is enabled to convert the 10-bit code-group into the corresponding 8-bit data byte and output at RD[0–7]. RD[8] is used as qualifier to indicate if RD[0–7] belongs to the D-group (RD8=0), or K-group (RD8=1). RD[9] is used as a second error pin that is only used to flag 8b/10b code and disparity errors.

Two recovered byte clock RBC0 and RBC1 are available for clocking the parallel data bus RD[0–9]. RBC0 and RBC1 are 180˚ out of phase. Users can latch even- and odd-numbered data word at RD[0–9] with the rising edge of successive RBC1 and RBC0. RBC0 and RBC1 have half the transfer rate frequency. In the low-data-rate mode (EN_HDR=0), the deserializer runs at half data rate.

When EN_RBC=1, RBC frequency is same as the bus transfer rate. Each rising edge of RBC1 strobes data word at RD[0–9]. See *Figure 7*.

RBC1 (EN_RBC=1) See *Figure 7*	RBC0, RBC1 (EN_RBC=0) See *Figure 6*	Transfer Rate at RD[0–9] = Line Rate / 10	Line Rate at RI± (High Data Rate Mode)
212.5 MHz	106.25 MHz	212.5 Mword/s	2.125 Gbps
250.0 MHz	125 MHz	250 Mword/s	2.50 Gbps

RBC1 (EN_RBC=1)	RBC0, RBC1 (EN_RBC=0)	Transfer Rate at RD[0–9] = Line Rate / 10	Line Rate at DO± (Low Data Rate Mode)
106.25 MHz	53.125 MHz	106.25 Mword/s	1.0625 Gbps
125 MHz	62.5 MHz	125 Mword/s	1.25 Gbps

When parallel data is serialized, the character alignment is lost. The Deserializer uses Comma character detection to establish the correct bit boundary of the 10-bit word. This process is called "code-group alignment". When a Comma character is detected, the CDET indicator is pulsed high, the corresponding Comma character is output at RD[0–9] (10-bit mode), or RD[0–8] (8-bit mode). During the alignment, RBC1 is stretched and the rising edge of RBC1 is aligned with the Comma character. The code-group alignment is enabled by EN_CDET active. When EN_CDET is low, the CDET indicator still functions, but no alignment is initiated when a comma character is detected.

DS25C400 detects both the +K28.5 and –K28.5 comma characters. These are unique binary patterns that cannot occur in valid data. A bit error could produce a misaligned comma character. This would cause an improper word re-alignment, if comma detect is enabled. Any higher order comma detect function that required the detection of multiple misaligned comma characters before initiating word realignment must be added externally by the user.

SERIAL LOCAL LOOPBACK

DS25C400 provides an internal loopback of the serial transmit data to the receiver's limiting amplifier of each channel. EN_SLB = 1 activates serial local loopback path for all four channels. DO± are disabled with output current = 0, and incoming data at RI± are ignored. Self test can be performed by comparing the parallel recovered output data at RD[0–9] to the parallel transmit input data at TD[0–9]. EN_LOS pin must be tied high (disabled LOS control of RD[0-9]) during serial local loopback testing. For normal data transmission operation using cable or PCB trace, set EN_SLB = 0 and EN_LOS can be tied low.

BIST

DS25C400 has a built-in 2^7–1 PRBS (pseudo-random bit sequence) generator, an alternating 1_0 generator, and a repeating ±K28.5 pattern, selected by EN_PTN0 and EN_PTN1. When internal pattern generator is enabled, the parallel input data at TD[0–9] are ignored. The Serializer converts the test pattern into serial bit stream at DO±. When the internal PRBS pattern is selected (EN_PTN1=0, EN_PTN0=1), an external bit error rate tester can be used to measure the error rate of the Serializer.

The DS25C400 has a built-in 2^7–1 PRBS checker in the Deserializer data path. It is initialized when EN_ERR is pulsed high then low with a minimum period of 10 µs. This will allow the internal error checker to achieve synchronization with the incoming (2^7–1) bit stream. With EN_ERR=0, ER_n pulses high for 10-bit period if the PRBS checker detects an error in the receive data word. It provides a simple mechanism to monitor the Deserializer's error rate performance by measuring the number of pulses at ER_n pin over a period of time. When EN_ERR is left high, ER_n will flag 8b/10b disparity and code violation errors instead of PRBS errors. When the 8b/10b mode is activated, RD[9] becomes a second error pin that flags 8b/10b errors.

The built-in PRBS generator and error checker, together with the internal loopback offer very powerful high speed self-test capability for the DS25C400.

POR

Upon application of power, the DS25C400 generates a power-on reset. During reset, RD[0–9] are set to logic low, and the LOS outputs are put into inactive state. RBC0 and RBC1 are at unknown state. The POR circuit monitors both

Functional Descriptions (Continued)

the 2.5V supply and the 1.8V supply. The 2.5V POR threshold voltage is approzimately 2.0V. There is about 50mV of hysteresis for this threshold. The 1.8V POR threshold is about 1.1V with 50mV of hysteresis. When the POR circuit is active, the PLL VCO capacitors are discharged to allow correct operation when a good power level is again established. Futhermore, the POR resets the internal digital counters to correct settings to be in a ready condition when supplies have been corrected. A termination resistor calibration sequence will also be executed.

RTERM

During power-on reset, the on-chip input termination resistors at RI± and the termination resistors at DO± are adjusted at power up and compared to the current through an external resistor connected from RTERM pin to RTERM-_RTN. The on-chip termination resistors can be maintained to within a ±10%. The external resistor at RTERM should be 249Ω ±1% for 50Ω on-chip terminations.

POWER DOWN

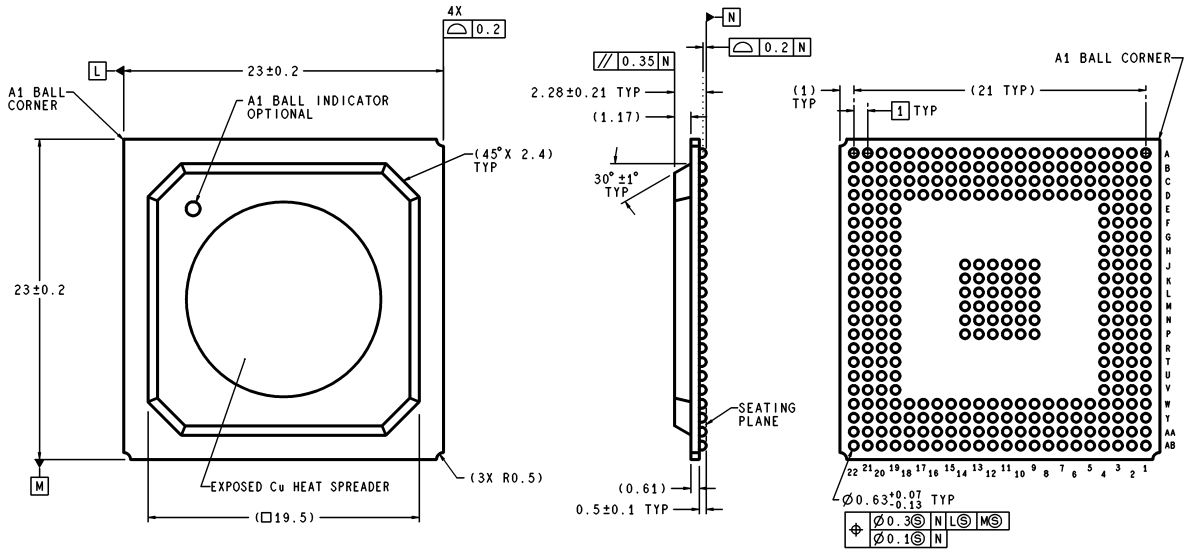
There are two control lines that control the power down modes, PD0 and PD1. With PD0=0 and PD1=0 all four channels are powered down, which subsequently power down the reference clock buffers as well as the bias circuits. This mode will allow measuring an I_{DDQ} or leakage current test. To properly measure the I_{DDQ}, the following sequence must be followed: first power up the device, then apply the reference clock and finally set the device to power down mode (PD0=0, PD1=0) and remove the reference clock. The other three states allow one, two, or four channels to be powered up. The reference clock buffers and bias circuits are powered up in these states.

PD1	PD0	$IDD_{2.5}$	$IDD_{1.8}$	Description
0	0	TBD	TBD	All 4 channels powered down
0	1	TBD	TBD	Only Channel A powered up
1	0	TBD	TBD	Channels A and B powered up
1	1	TBD	TBD	All 4 channels powered up

POWER SEQUENCE REQUIREMENT

The 2.5 V supplies (V_{DDHS}, V_{DDIO} and V_{DDB}) should be supplied, followed by the 1.8 V supplies. All the 2.5 V supplies should be tied to a common power plane.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

UFJ324A (Rev A)

Order Number DS25C400TUT
See NS Package Number UFJ324

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