National Semiconductor

March 2006

DS26F32MQML
Quad Differential Line Receivers

General Description

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input common mode range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and TRI-STATE ® outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

Features

- Input voltage range of ±7.0V (differential or common mode) ±0.2V sensitivity over the input voltage range
- High input impedance
- Operation from single +5.0V supply
- Input pull-down resistor prevents output oscillation on unused channels
- TRI-STATE outputs, with choice of complementary enables, for receiving directly onto a data bus

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS26F32ME/883	5962–7802005M2A	E20A	20LD Leadless Chip Carrier
DS26F32MJ/883	5962–7802005MEA	J16A	16LD Ceramic DIP
DS26F32MW/883	5962–7802005MFA	W16A	16LD Ceramic FLatpack
DS26F32MWG/883	5962–7802005MZA	WG16A	16LD Ceramic SOIC
DS26F32MER-QML	5962R7802005M2A	E20A	20LD Leadless Chip Carrier
DS26F32MJR-QML	5962R7802005QEA	J16A	16LD Ceramic DIP
DS26F32MWR-QML	5962R7802005QFA	W16A	16LD Ceramic FLatpack
DS26F32MJ-QMLV	5962–7802005VEA	J16A	16LD Ceramic DIP
DS26F32MW-QMLV	5962–7802005VFA	W16A	16LD Ceramic FLatpack
DS26F32MWG-QMLV	5962–7802005VZA	WG16A	16LD Ceramic SOIC
DS26F32MJRQMLV	5962R7802005VEA 100k rd(Si)	J16A	16LD Ceramic DIP
DS26F32MWRQMLV	5962R7802005VFA 100k rd(Si)	W16A	16LD Ceramic FLatpack
DS26F32MWGRQMLV	5962R7802005VZA 100k rd(Si)	WG16A	16LD Ceramic SOIC

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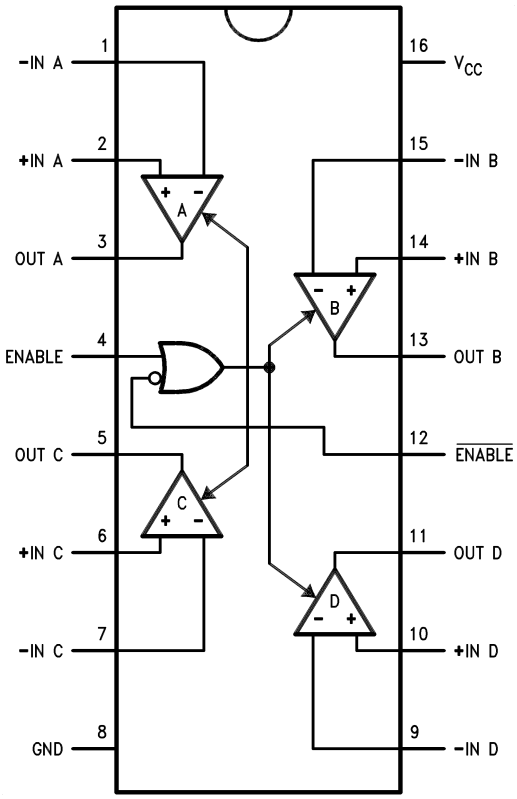
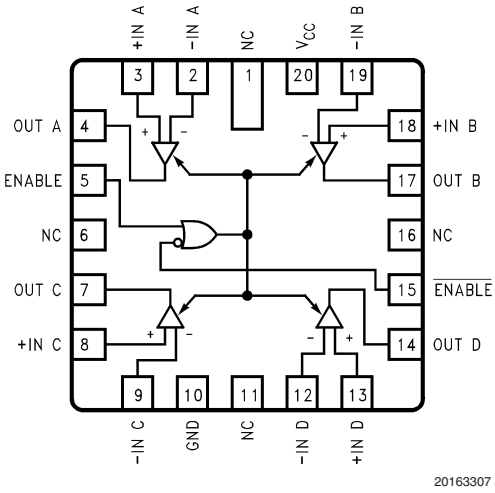
Connection Diagrams



Top View
16-Lead Ceramic DIP Pictured
See NS Package Number WG16A, J16A or W16A



20-Lead Ceramic Leadless Chip Carrier
See NS Package Number E20A

Function Table

(Each Receiver)

Differential Inputs	Enables		Outputs
$V_{ID} = (V_I+) - (V_I-)$	E	$\overline{E}$	OUT
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
X = Immaterial

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Absolute Maximum Ratings (Note 1)

Storage Temperature Range	$-65^{\circ}C \le T_A \le +150^{\circ}C$
Operating Temperature Range	$-55^{\circ}C \le T_A \le +125^{\circ}C$
Lead Temperature (soldering, 60 sec)	300˚C
Supply Voltage	7.0V
Common Mode Voltage Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50 mA
Maximum Power Dissipation ($P_{D\ max}$ at 25˚C (Note 2), (Note 3)	500 mW
Thermal Resistance	
θ_{JA}	
Ceramic DIP	100˚C/W
Ceramic Flatpack	142˚C/W
Leadless Chip Carrier	87˚C/W
θ_{JC}	
Junction-to- case	See MIL-STD-1835

Recommended Operating Range

Operating Temperature	$-55^{\circ}C \le T_A \le +125^{\circ}C$
Supply Voltage	4.5V to 5.5V

Radiation Features

DS26F32MJRQMLV	100 krads (Si)
DS26F32MWRQMLV	100 krads (Si)
DS26F32MWGRQMLV	100 krads (Si)

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp ˚C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

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DS26F32 Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified.

DC: V_{CC} = 5V (Note 7)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{In}	Input Current	Pin under test V_{CC} = 4.5V, V_I = 15V Other inputs -15V ≤ V_I ≤ +15V			2.3	mA	1, 2, 3
		Pin under test V_{CC} = 5.5V, V_I = -15V Other inputs -15V ≤ V_I ≤ +15V			-2.8	mA	1, 2, 3
I_{IL}	Logical "0" Enable Current	V_{CC} = 5.5V, V_{En} = 0.4V			-360	µA	1, 2, 3
I_{IH}	Logical "1" Enable Current	V_{CC} = 5.5V, V_I = 2.7V			10	µA	1, 2, 3
I_I	Logical "1" Enable Current	V_{CC} = 5.5V, V_I = 5.5V			50	µA	1, 2, 3
V_{IK}	Input Clamp Voltage (Enable)	V_{CC} = 4.5V, I_I = -18mA			-1.5	V	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, I_{OH} = -440µA, ΔV_I = 1V, $V\overline{En}$ = .8 = V_{En}		2.5		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 4.5V, $V\overline{En}$ =0.8V = V_{En}, I_{OL} = 4mA, ΔV_I = -1V			0.4	V	1, 2, 3
		V_{CC} = 4.5V, $V\overline{En}$ = 8V = V_{En}, I_{OL} = 8mA, ΔV_I = -1V			.45	V	1, 2, 3
I_{CC}	Supply Current	V_{CC} = 5.5V, All V_I = Gnd, V_{En} = 0V, $\overline{V_{En}}$ = 2V			50	mA	1, 2, 3
I_{OZ}	Off-State Output Current	V_{CC} = 5.5V, V_O = 0.4V, V_{En} = 0.8V, $\overline{V_{En}}$ = 2V			-20	µA	1, 2, 3
		V_{CC} = 5.5V, V_O = 2.4V, V_{En} = 0.8V, $\overline{V_{En}}$ = 2V			20	µA	1, 2, 3
R_I	Input Resistance	-15 ≤ V_{CM} ≤ 15V		14		KΩ	1, 2, 3
V_{Th}	Differential Input Voltage	V_{CC} = 4.5V, V_{OUT} = V_{OL} or V_{OH} -7V ≤ V_{CM} ≤ 7V, V_{En} = $\overline{V_{En}}$ = 2.5V	(Note 4)	-0.2	0.2	V	1, 2, 3
		V_{CC} = 5.5V, V_{OUT} = V_{OL} or V_{OH} -7V ≤ V_{CM} ≤ 7V, V_{En} = $\overline{V_{En}}$ = 2.5V	(Note 4)	-0.2	0.2	V	1, 2, 3
V_{IL}	Logical "0" Input Voltage (Enable)	V_{CC} = 5.5V	(Note 4)		0.8	V	1, 2, 3
V_{IH}	Logical "1" Input Voltage (Enable)	V_{CC} = 4.5V	(Note 4)	2.0		V	1, 2, 3
$I_{SC\ Min}$	Output Short Circuit Current	V_{CC} = 4.5V, V_O = 0V, ΔV_I = 1V		-15		mA	1, 2, 3
$I_{SC\ Max}$	Output Short Circuit Current	V_{CC} = 5.5V, V_O = 0V, ΔV_I = 1V			-85	mA	1, 2, 3

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DS26F32 Electrical Characteristics (Continued)

AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = 5V (Note 7)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PLH}		C_L = 50pF	(Note 6)		23	nS	9
			(Note 6)		31	nS	10, 11
		C_L = 15pF	(Note 5)		22	nS	9
			(Note 5)		30	nS	10, 11
t_{PHL}		C_L = 50pF	(Note 6)		23	nS	9
			(Note 6)		31	nS	10, 11
		C_L = 15pF	(Note 5)		22	nS	9
			(Note 5)		30	nS	10, 11
t_{PZH}	Enable Time	C_L = 50pF	(Note 6)		18	nS	9
			(Note 6)		29	nS	10, 11
		C_L = 15pF	(Note 5)		16	nS	9
			(Note 5)		27	nS	10, 11
t_{PZL}	Enable Time	C_L = 50pF	(Note 6)		20	nS	9
			(Note 6)		29	nS	10, 11
		C_L = 15pF	(Note 5)		18	nS	9
			(Note 5)		27	nS	10, 11
t_{PHZ}	Disable Time	C_L = 50pF	(Note 6)		55	nS	9
			(Note 6)		62	nS	10, 11
		C_L = 5pF	(Note 5)		20	nS	9
			(Note 5)		27	nS	10, 11
t_{PLZ}	Disable Time	C_L = 50pF	(Note 6)		30	nS	9
			(Note 6)		42	nS	10, 11
		C_L = 5pF	(Note 5)		18	nS	9
			(Note 5)		30	nS	10, 11

DC Drift Parameters

This section applies to -QMLV devices only. Devices shall be read & recorded at T_A = 25˚C before and after each burn-in and shall not change by more than the limits indicated. The delta rejects shall be included in the PDA calculation.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, I_{OH} = -440µA, ΔV_I = 1V, $V\overline{En}$ = 0.8V = V_{En}		-250	250	mV	1
V_{OL}	Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OL} = 4mA, ΔV_I = -1V, $V\overline{En}$ = 0.8V = V_{En}		-45	45	mV	1
		V_{CC} = 4.5V, I_{OL} = 8mA, Δ V_I = -1V, $V\overline{En}$ = 0.8V = V_{En}		-45	45	mV	1
I_I	Input Current	Pin under test V_{CC} = 4.5V, V_I = 15V Other inputs -15V ≤ V_I ≤ +15V		-0.28	0.28	mA	1
		Pin under test V_{CC} = 5.5V, V_I = -15V Other inputs -15V ≤ V_I ≤ +15V		-0.28	0.28	mA	1

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Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Derate J package 10.0mW/˚C above +25˚C, derate W package 7.1mW/˚C above +25˚C, derate E package 11.5mW/˚C above +25˚C.

Note 3: Power dissipation must be externally controlled at elevated temperatures.

Note 4: Parameter tested go-no-go only.

Note 5: Tested at 50pF guarantees limit at 15pF & 5pF.

Note 6: Tested at 50pF, system capacitance exceeds 5pF to 15pF.

Note 7: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A

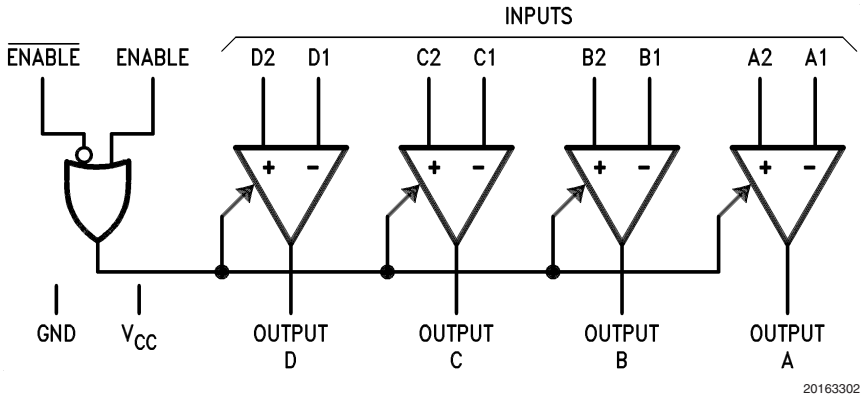

FIGURE 1. Logic Symbol

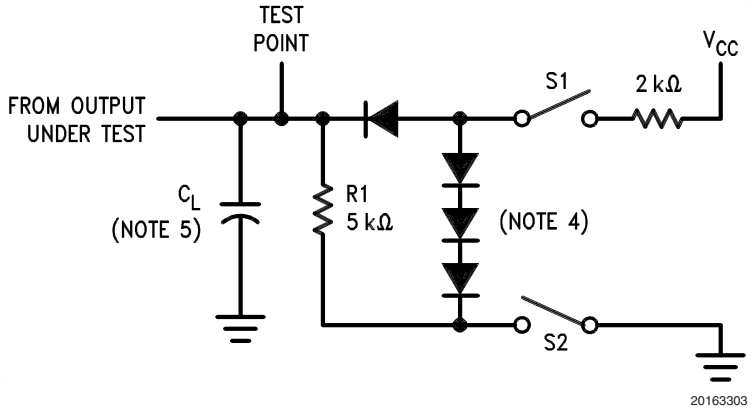

FIGURE 2. Load Test Circuit for Three-State Outputs

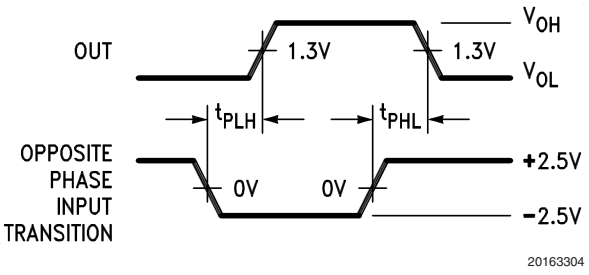

FIGURE 3. Propagation Delay (Notes 8, 9, 10)

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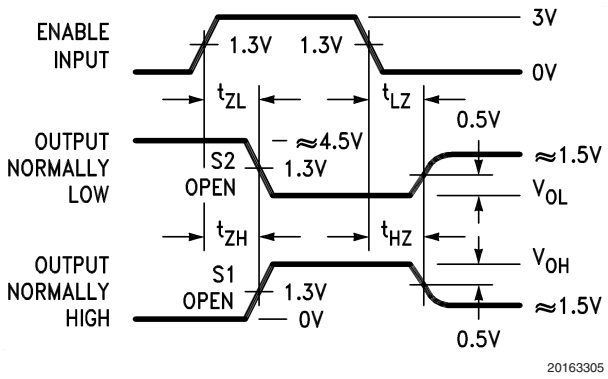

Note 8: Diagram shown for $\overline{\text{ENABLE}}$ Low.

Note 9: S1 and S2 of Load Circuit are closed except where shown.

Note 10: Pulse Generator of all Pulses: Rate ≤ 1.0 MHz, $Z_O = 50\Omega$, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns.

Note 11: All diodes are IN916 or IN3064.

Note 12: C_L includes probe and jig capacitance.

FIGURE 4. Enable and Disable Times (Notes 8, 9, 10)

Typical Application

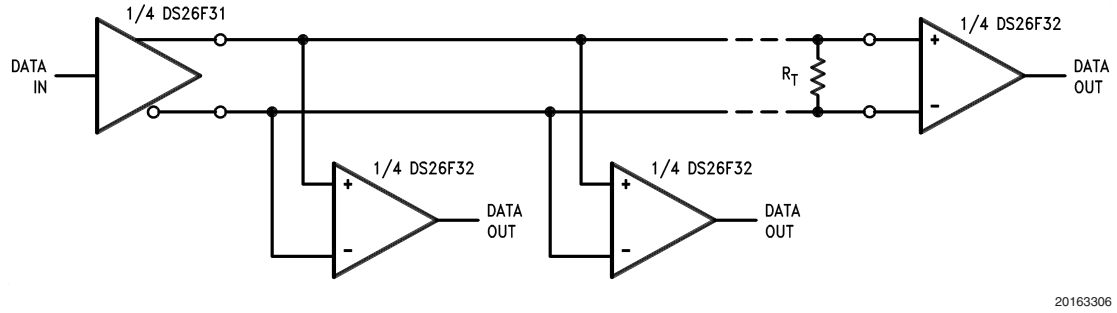

FIGURE 5.

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Revision History

Released	Revision	Section	Originator	Changes
03/01/06	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MNDS26F32M-X-RH Rev 0C0 will be archived.

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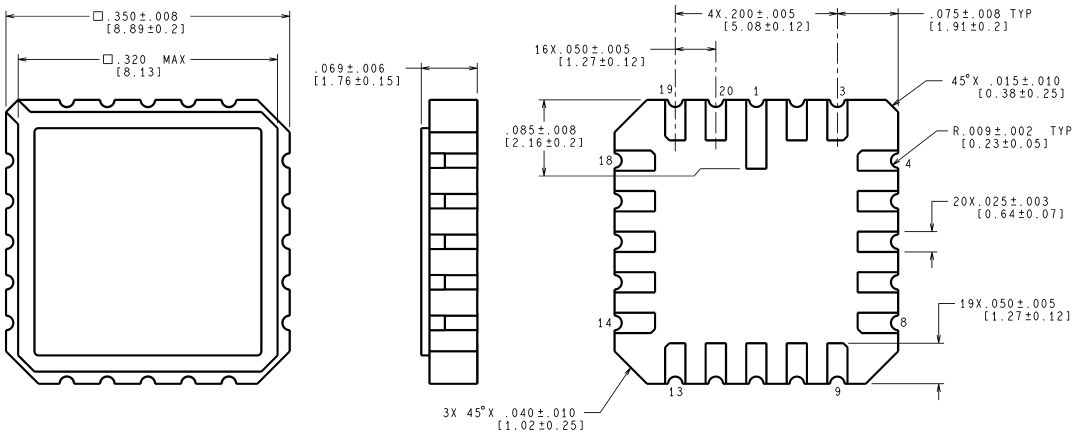
Physical Dimensions inches (millimeters) unless otherwise noted



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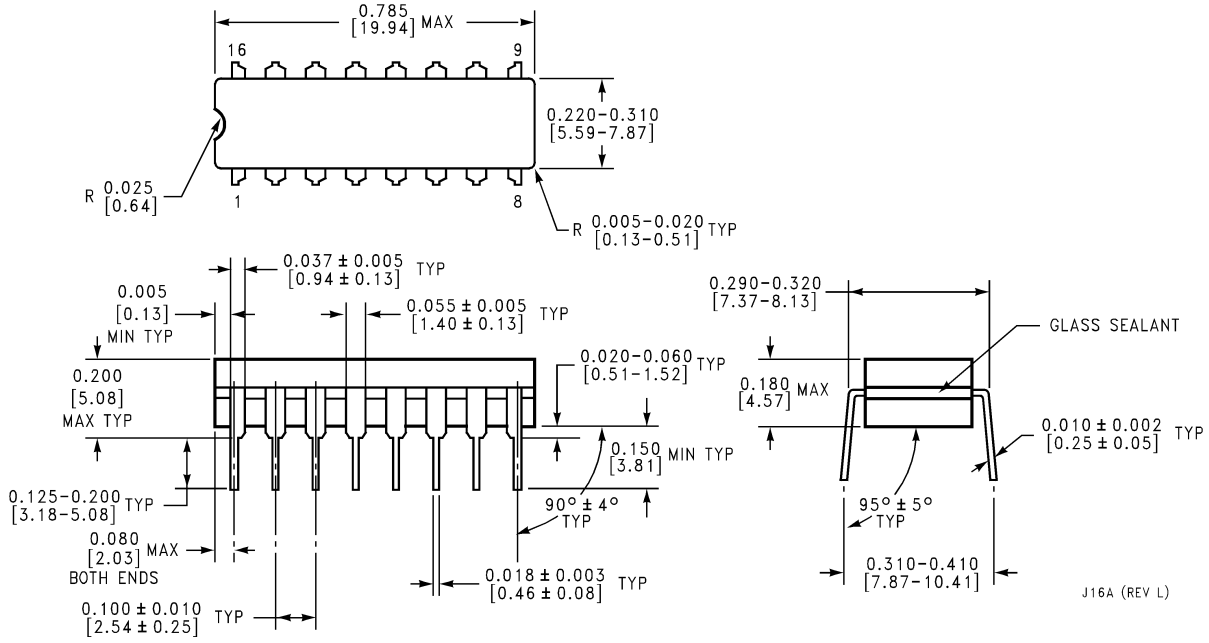
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

20LD Leadless Chip Carrier (E)
NS Package Number E20A



Ceramic Dual-In-Line Package (J)
NS Package Number J16A

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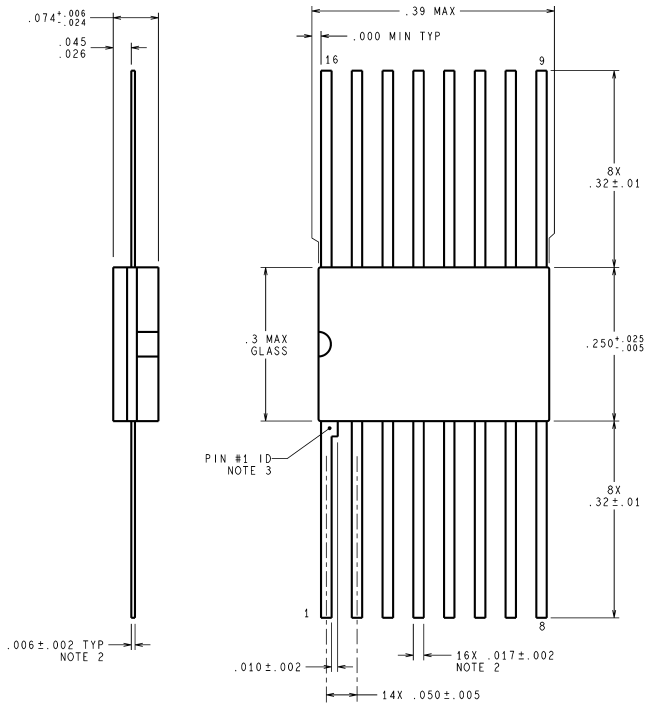
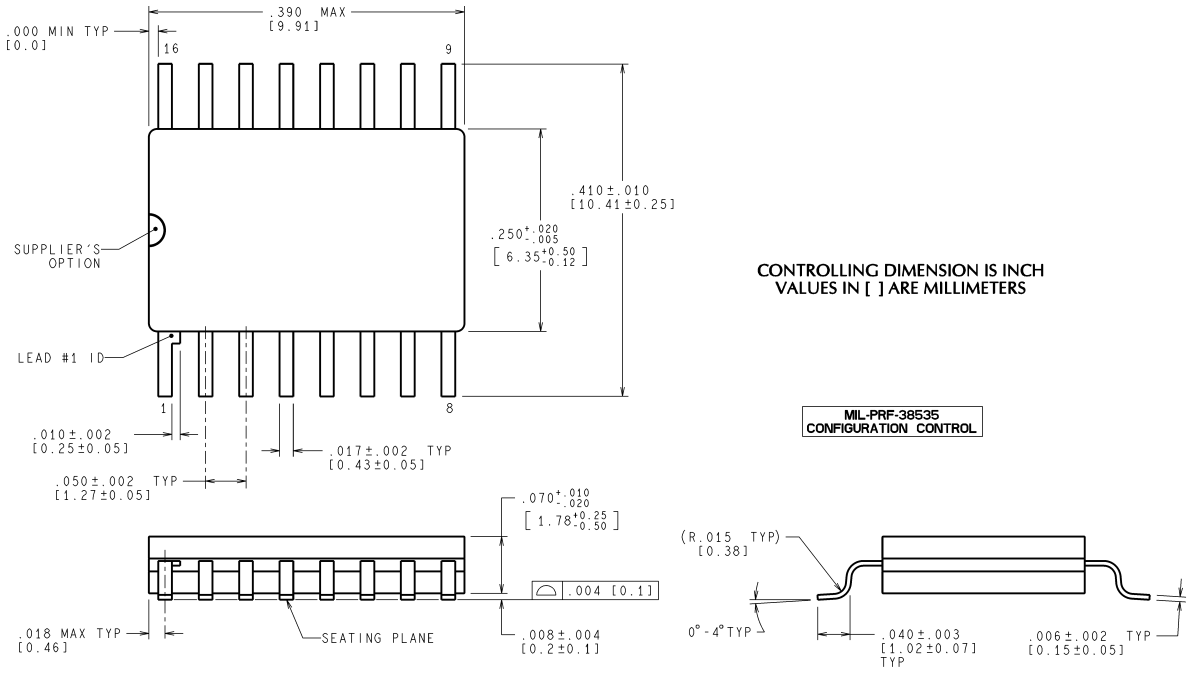
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN INCHES

W16A (Rev T)

16LD Ceramic Flatpack (W)
NS Package Number W16A



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MIL-PRF-38535
CONFIGURATION CONTROL

WG16A (Rev D)

16LD Ceramic SOIC (WG)
NS Package Number WG16A

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Notes

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