

SNOSAM6B-OCTOBER 2005-REVISED APRIL 2013

DS26LS32MQML Quad Differential Line Receivers

Check for Samples: DS26LS32MQML

FEATURES

- High Differential or Common-Mode Input Voltage Ranges of ±7V on the DS26LS32.
- ±0.2V Sensitivity Over the Input Voltage Range on the DS26LS32.
- DS26LS32 Meet All Requirements of RS-422
 and RS-423
- 6k Minimum Input Impedance
- 100 mV Input Hysteresis on the DS26LS32
- Operation From a single 5V Supply
- TRI-STATE Outputs, with Choice of Complementary Output Enables for Receiving Directly onto a Data Bus

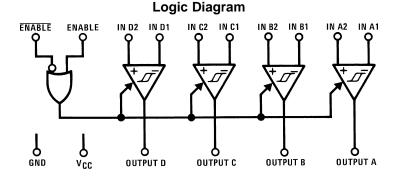
DESCRIPTION

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of \pm 7V. The DS26LS33 has an input sensitivity of 500 mV over the input voltage range of \pm 15V.

The DS26LS32A differs in function from the popular DS26LS32 and DS26LS33 in that input pull-up and pull-down resistors are included which prevent output oscillation on unused channels.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commercial operating temperature ranges.



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Connection Diagram

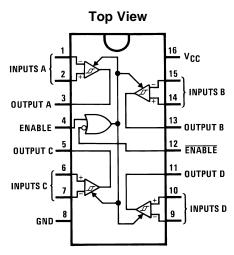


Figure 1. CDIP Package See Package Numbers NFE0016A, NAD0016A

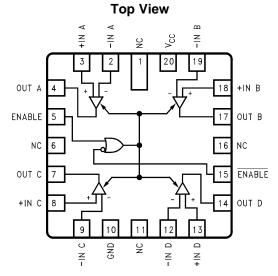


Figure 2. 20-Lead LCCC Package See Package Number NAJ0020A

Truth Table⁽¹⁾

| ENABLE | ENABLE | Input | Output |
|---------|----------|---|--------|
| 0 | 1 | X | Hi-Z |
| See No. | to Dolow | V _{ID} ≥ V _{TH} (Max) | 1 |
| See No | te Below | $V_{ID} \leq V_{TH}$ (Min) | 0 |

(1) Hi-Z = TRI-STATE

Note: Input conditions may be any combination not defined for ENABLE and ENABLE .



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1)

| 7V |
|------------------|
| ±25V |
| ±25V |
| 7V |
| 50 mA |
| |
| 1666.5 mW |
| 1875 mW |
| 967.74 mW |
| +150°C |
| |
| 100°C/W |
| 130°C/W |
| 140°C/W |
| See MIL-STD-1835 |
| −65°C to +165°C |
| 260°C |
| 500V |
| |

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation. Derate NFE0016A, package 11.11 mW/°C above 25°C; derate NAJ0020A package 12.5 mW/°C above 25°C; derate NAD0016A

(2)

Package 6.4516 mW/°C for above 25°C.

Human body model, $1.5k\Omega$ in series with 100pF. (3)

Recommended Operating Conditions

| Supply Voltage, V _{CC} | 4.5 V to 5.5 V |
|---------------------------------|-----------------|
| Temperature, T _A | −55°C to +125°C |

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

| Subgroup | Description | Temp (°C) |
|----------|---------------------|------------|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

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STRUMENTS

EXAS

DS26LS32M 883 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified. $V_{CC} = 5V$

| | Parameter | Test Conditions | Notes | Min | Мах | Unit | Sub- groups |
|-----------------------|---------------------------------------|--|--------|------|------|------|----------------|
| 1 | Incut Current | $V_{CC} = 5.5V$, $V_{IN} = 15V$ (Pin under test), other inputs -15V, $\leq V_{IN} \leq +15V$ | (1) | | 2.3 | mA | 1, 2, 3 |
| I _{IN} | Input Current | $V_{CC} = 5.5V$, $V_{IN} = -15V$ (Pin under test), other inputs -15V, $\leq V_{IN} \leq +15V$ | (1) | | -2.8 | mA | 1, 2, 3 |
| IIL | Logical "0" ENABLE Current | $V_{CC} = 5.5 V, V_{IN} = 0.4 V$ | (1) | | -360 | uA | 1, 2, 3 |
| I _{IH} | Logical "1" ENABLE Current | V _{CC} = 5.5V, V _{IN} = 2.7V | (1) | | 20 | uA | 1, 2, 3 |
| l _l | Logical "1" ENABLE Current | V _{CC} =5.5V, V _{IN} = 5.5V | (1) | | 100 | uA | 1, 2, 3 |
| V _{IC} | Input Clamp Voltage (ENABLE) | V _{CC} = 4.5V, I _{IN} = -18mA | (1) | | -1.5 | V | 1, 2, 3 |
| V _{OH} | Logical "1" Output Voltage | $\label{eq:V_CC} \begin{array}{l} V_{CC} = 4.5V, \ I_{\underline{OH}} = -440uA, \\ \DeltaV_{IN} = 1V, \ V \ ENABLE = 0.8V \end{array}$ | (1) | 2.5 | | V | 1, 2, 3 |
| | | $V_{CC} = 4.5V, I_{OL} = 4mA, \Delta V_{IN} = -1V, V ENABLE = 0.8V$ | (1) | | .4 | V | 1, 2, 3 |
| V _{OL} | Logical "0" Output Voltage | $\label{eq:V_CC} \begin{array}{l} V_{CC} = 4.5V, \ I_{OL} = 8mA, \\ \DeltaV_{IN} = -1V, \ V \ ENABLE = 0.8V \end{array}$ | (1) | | .45 | V | 1, 2, 3 |
| I _{OS} (MIN) | Output Short Circuit Current | $ \begin{array}{l} V_{CC}=5.5V, \ V_{O}=0V, \\ \DeltaV_{IN}=1V \end{array} $ | (1) | -15 | | mA | 1, 2, 3 |
| I _{OS} (MAX) | Output Short Circuit Current | $ \begin{array}{l} V_{CC} = 5.5V, V_{O} = 0V, \\ \DeltaV_{IN} = 1V \end{array} $ | (1) | | -85 | mA | 1, 2, 3 |
| I _{CC} | Supply Current | $V_{CC} = 5.5V$, All $V_{IN} = GND$, Outputs Disabled | (1) | | 70 | mA | 1, 2, 3 |
| | | $V_{CC} = 5.5 V, V_{O} = 0.4 V$ | (1) | | -20 | uA | 1, 2, 3 |
| lo | Off-State Output Current | $V_{CC} = 5.5V, V_{O} = 2.4V$ | (1) | | 20 | uA | 1, 2, 3 |
| V _{TH} | Differential Input Voltage | $-7V \le V_{CM} \le 7V$ | (1)(2) | -0.2 | 0.2 | V | 1, 2, 3 |
| R _{IN} | Input Resistance | -15V ≤ V _{CM} ≤ 15V | (1) | 6 | | kohm | 1, 2, 3 |
| V _{IL} | Logical "0" Input Voltage (ENABLE) | V _{CC} = 4.5V | (1)(2) | | 0.8 | V | 1, 2, 3 |
| V _{IH} | Logical "1" Input Voltage (ENABLE) | V _{CC} = 4.5V | (1)(2) | 2 | | V | 1, 2, 3 |

(1) For Subgroups 1 and 2, power dissipation must be externally controlled at elevated temperatures.

(2) Parameter tested go-no-go only.

DS26LS32M 883 Electrical Characteristics AC Parameters - Propagation Delay Time

The following conditions apply, unless otherwise specified. V_{CC} = 5V

| | Parameter | Test Conditions | Notes | Min | Мах | Unit | Sub- groups | |
|------------------|------------------------|---|-------|-----|-----|------|----------------|--|
| t _{PLH} | Propagation Delay Time | $C_L = 15_PF$ | (1) | | 30 | nS | 9,11, | |
| t _{PLH} | Propagation Delay Time | $C_L = 15_PF$ | (1) | | 120 | nS | 10 | |
| t _{PHL} | Propagation Delay Time | $C_L = 15_PF$ | (1) | | 30 | nS | 9,11, | |
| t _{PHL} | Propagation Delay Time | C _L = 15 _P F | (1) | | 120 | nS | 10 | |
| | | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 5_{\text{P}}\text{F}$ | (1) | | 34 | nS | 9 | |
| t _{PLZ} | Enable to Output | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 5_{\text{P}}\text{F}$ | (1) | | 64 | nS | 10 | |
| | | $\overline{ENABLE} \ C_{L} = 5_{P}F$ | (1) | | 27 | nS | 11 | |
| | Eachta ta Octavit | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 5_{\text{P}}\text{F}$ | (1) | | 32 | nS | 9,11, | |
| t _{PHZ} | Enable to Output | $\overline{\text{ENABLE}}$ C _L = 5 _P F | (1) | | 35 | nS | 10 | |
| | | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 15_{\text{P}}\text{F}$ | (1) | | 34 | nS | 9 | |
| t _{PZL} | Enable to Output | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 15_{\text{P}}\text{F}$ | (1) | | 65 | nS | 10 | |
| | | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 15_{\text{P}}\text{F}$ | (1) | | 27 | nS | 11 | |

(1) Tested at 25°C, specified but not tested at +125°C & -55°C



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DS26LS32M 883 Electrical Characteristics AC Parameters - Propagation Delay Time (continued)

The following conditions apply, unless otherwise specified. $V_{CC} = 5V$

| | Parameter | Test Conditions | Notes | Min | Max | Unit | Sub- groups |
|------------------|------------------|---|-------|-----|-----|------|----------------|
| | Enchle to Output | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 15_{\text{P}}\text{F}$ | (1) | | 35 | nS | 9, 11 |
| ^t PZH | Enable to Output | $\overline{\text{ENABLE}} \text{ C}_{\text{L}} = 15_{\text{P}}\text{F}$ | (1) | | 65 | nS | 10 |

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

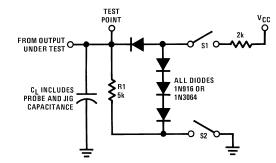
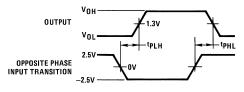
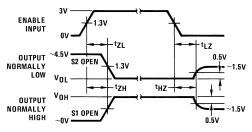


Figure 3. Load Test Circuit for TRI-STATE Outputs



- (1) Diagram shown for ENABLE low.
- (2) Pulse generator for all pulses: Rate = 1.0 MHz; $Z_0 = 50\Omega$; $t_r \le 6$ ns; $t_f \le 6.0$ ns.

Figure 4. Propagation Delay



- (1) S1 and S2 of load circuit are closed except where shown.
- (2) Pulse generator for all pulses: Rate = 1.0 MHz; $Z_0 = 50\Omega$; $t_f \le 6$ ns; $t_f \le 6.0$ ns.

Figure 5. Enable and Disable Times

TYPICAL APPLICATIONS

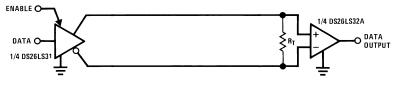


Figure 6. Two-Wire Balanced Interface—RS-422



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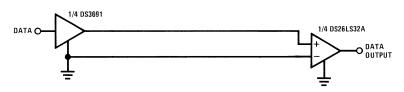


Figure 7. Single Wire with Driver Ground Reference—RS-423

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REVISION HISTORY

| Date Released | Revision | Section | Originator | Changes |
|------------------|----------|--|------------|---|
| 10/20/05 | A | New Release, Corporate format. Changes made in conversion: Ordering Info. Table, Absolute Ratings, Maximum Operating Conditions, Typos in QMLV & RH, 883 AC Electrical Characteristics Parameters Column. | R. Malone | 1 MDS data sheet converted into Corporate data sheet format. Added: SMD reference for 883 NSID's, Juction temp., Thermal Resistance θ_{JA} and θ_{JC} . Changed: Maximum Operating Conditions to Recommended Operating Conditions, Enable and Disable Time to Enable to Output. Deleted max limit: 27nS for t _{PZH} and added subgroup 11 to max limit 35nS. MDS data sheet MNDS26LS32–X, Rev. 2B0 will be Archived. |
| 4/15/2013 | В | | TIS | Changed layout of National Data Sheet to TI format |



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|-------------------------|----------------------|--------------|--|---------|
| 5962-7802006QEA | ACTIVE | CDIP | NFE | 16 | 25 | TBD | Call TI | Call TI | -55 to 125 | (DS26C32AMJ/883 ~ DS26LS32MJ/883) (5962-7802006QEA Q ~ 5962-916400 1MEA Q) | Samples |
| DS26LS32MJ/883 | ACTIVE | CDIP | NFE | 16 | 25 | TBD | Call TI | Call TI | -55 to 125 | (DS26C32AMJ/883 ~ DS26LS32MJ/883) (5962-7802006QEA Q ~ 5962-916400 1MEA Q) | Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



25-Oct-2016

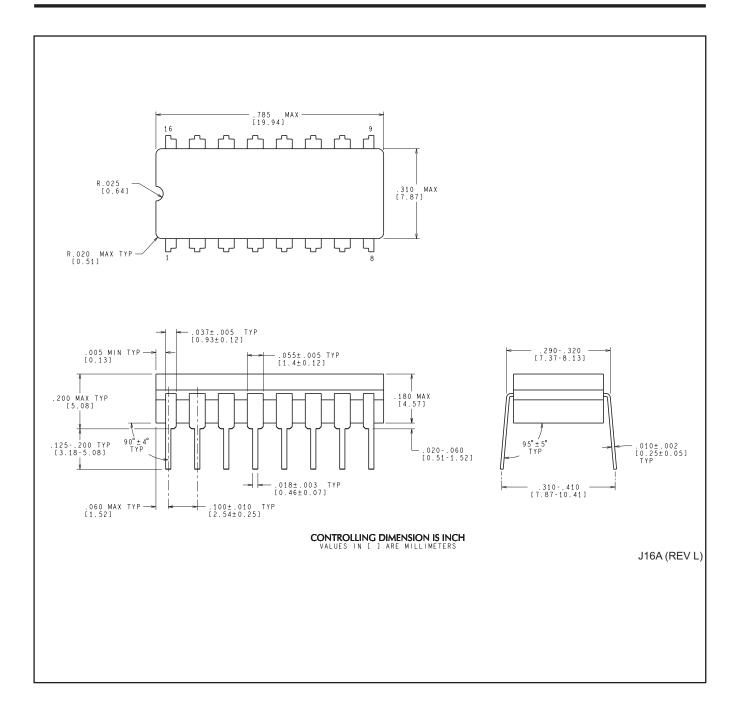
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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