National Semiconductor

DS3587/DS3487 Quad TRI-STATE® Line Driver

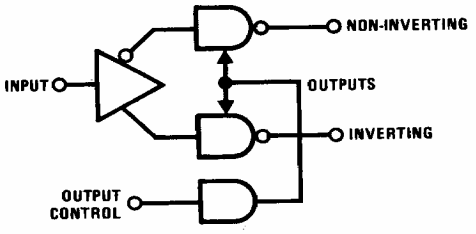
General Description

National's quad RS-422 driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs.

Features

- Four independent drivers
- TRI-STATE outputs
- Fast propagation times (typ 10 ns)
- TTL compatible
- 5V supply
- Output rise and fall times less than 15 ns
- Pin compatible with DS8924 and MC3487

Block and Connection Diagrams



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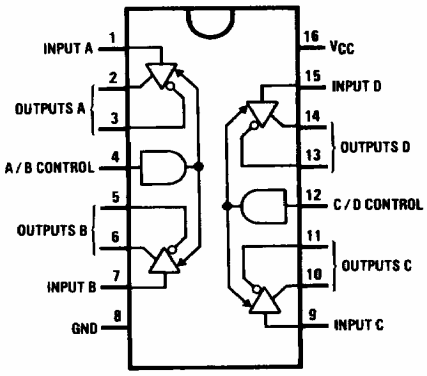
Dual-In-Line Package



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Top View

Order Number DS3587J, DS3487J, DS3487M or DS3487N
See NS Package Number J16A, M16A or N16A

Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate DIP molded package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS3587	4.5	5.5	V
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3587	−55	+125	°C
DS3487	0	+70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	μA
I_{IH}	Input High Current		V_{IH} = 2.7V			50	μA
			V_{IH} = 5.5V			100	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		V_O = 0.5V			−100	μA
			V_O = 5.5V			100	μA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0V	V_O = 6V			100	μA
			V_O = −0.25V			−100	μA
$\|V_{OS}-\bar{V}_{OS}\|$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\|V_T\|-\bar{V}_T\|$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		15	25	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

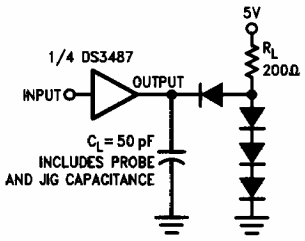
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive, all currents out of device pins as negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

AC Test Circuits and Switching Time Waveforms



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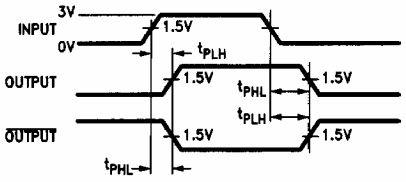

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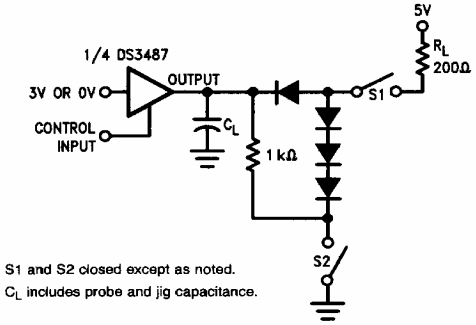
Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 1. Propagation Delays



S1 and S2 closed except as noted.

C_L includes probe and jig capacitance.

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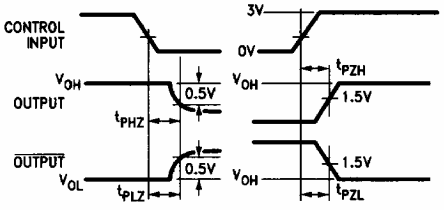

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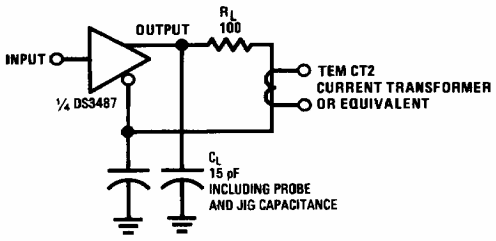
Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

S1 = open for t_{PZH}

S2 = open for t_{PZL}

FIGURE 2. TRI-STATE Enable and Disable Delays



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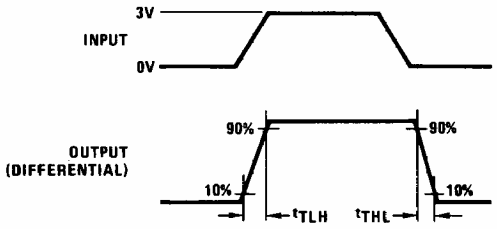

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Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 3. Differential Rise and Fall Times