National Semiconductor

February 1986

DS1628/DS3628 Octal TRI-STATE® MOS Drivers

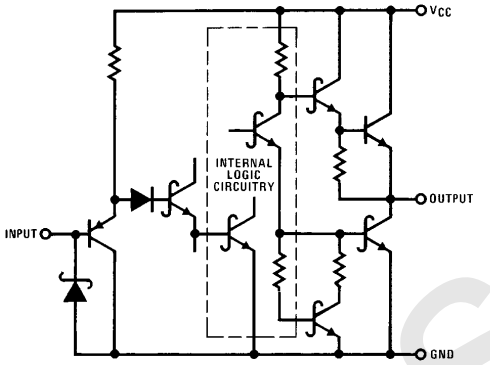
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

Features

- High speed capabilities
  - Typical 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4V min)
- High density
  - Eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

Schematic and Connection Diagrams



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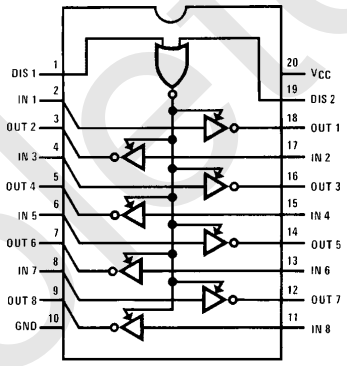
(Equivalent Input/Output Circuit)

Dual-In-Line Package



Top View

TL/F/5875–2

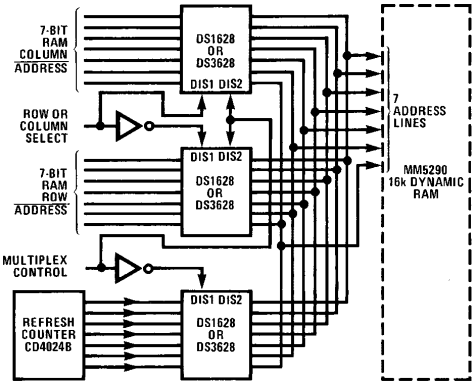
Order Number
DS1628J, DS3628J, DS3628N
See NS Package Number J20A or N20A

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1628	−55	+125	°C
DS3628	0	+70	°C

Electrical Characteristics (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			−180	−400	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V I_{IN} = −18 mA			−0.7	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1628	3.4	4.3		V
			DS3628	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1628		0.25	0.4	V
			DS3628		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1628	2.5	3.9		V
			DS3628	2.7	3.9		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1628/DS3628		0.35	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 6)			−150		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 6)			150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, DIS1 or DIS2 = 2.0V		−40	0.1	40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All Other Inputs = X, Outputs at Hi-Z		90	120	mA
			DIS1, DIS2 = 0V, Others = 3V Outputs on		70	100	mA
			All Inputs = 0V, Outputs Off		25	50	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 6)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{S+-}	Storage Delay Negative Edge	(*Figure 1*)	C_L = 50 pF		4.0	5.0	ns
			C_L = 500 pF		6.5	8.0	
t_{S-+}	Storage Delay Positive Edge	(*Figure 1*)	C_L = 50 pF		4.2	5.0	ns
			C_L = 500 pF		6.5	8.0	
t_F	Fall Time	(*Figure 1*)	C_L = 50 pF		4.2	6.0	ns
			C_L = 500 pF		19	22	
t_R	Rise Time	(*Figure 1*)	C_L = 50 pF		5.2	7.0	ns
			C_L = 500 pF		20	24	
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF to GND	R_L = 2 kΩ to V_{CC} (*Figure 2*)		19	25	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF to GND	R_L = 2 kΩ to GND (*Figure 2*)		13	20	ns

Switching Characteristics (Continued) (V_{CC} = 5V, T_A = 25°C) (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF to GND R_L = 400Ω to V_{CC} (*Figure 3*)		18	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF to GND R_L = 400Ω to GND (*Figure 3*)		8.5	15	ns

AC Test Circuits and Switching Time Waveforms

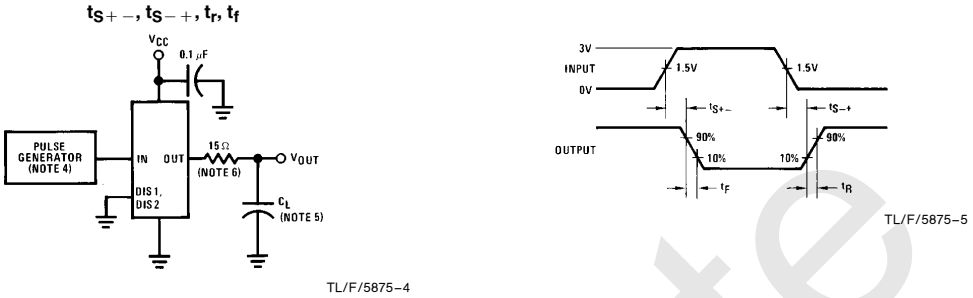


FIGURE 1

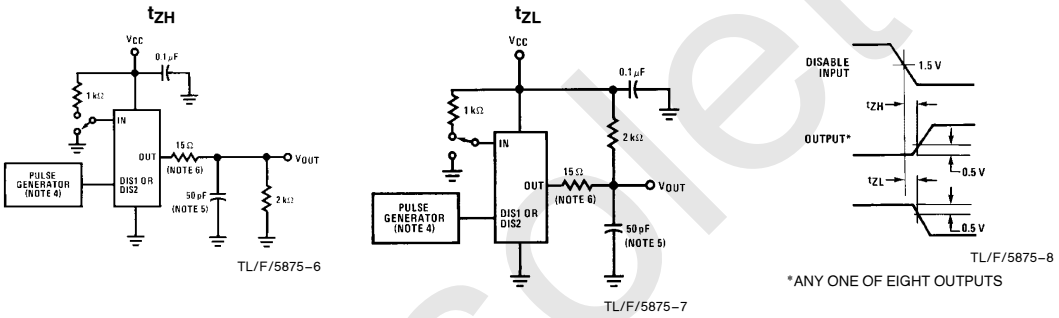


FIGURE 2

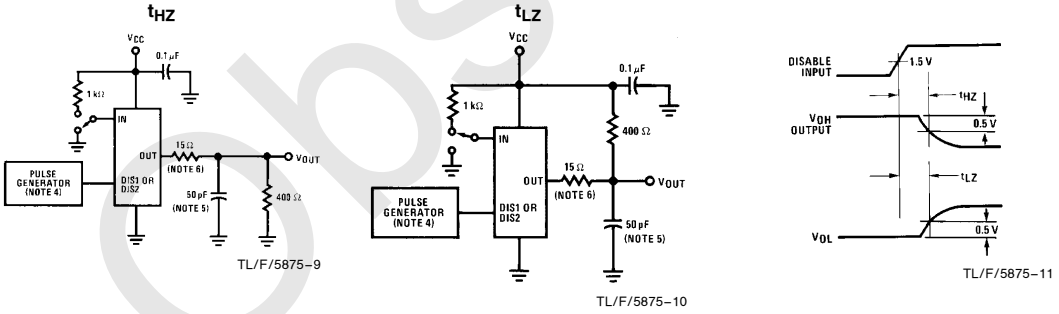


FIGURE 3

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1628 and across the 0°C to +70°C range for the DS3628. All typical values are for T_A = 25°C and V_{CC} = 5V.

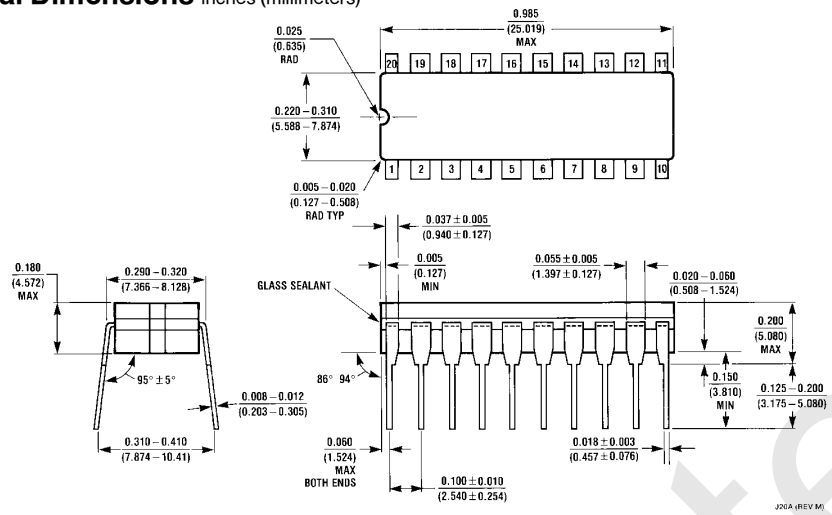
Note 3: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages references to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The pulse generator has the following characteristics: Z_{OUT} = 50Ω and PRR ≤ 1 mHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

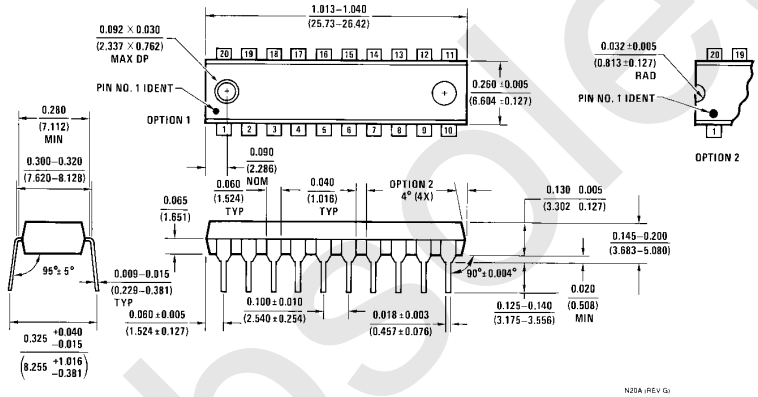
Note 5: C_L includes probe and jig capacitance.

Note 6: When measuring output drive current and switching response for the DS1628 and DS3628 a 15Ω resistor should be placed in series with each output.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number DS1628J or DS3628J
NS Package Number J20A



Molded Dual-In-Line Package (N)
Order Number DS3628N
NS Package Number N20A

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408