National Semiconductor

February 1986

DS3647A Quad TRI-STATE® MOS Memory I/O Register

General Description

The DS3647A is a 4-bit I/O buffer register intended for use in MOS memory systems. This circuit employs a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. This circuit uses Schottky-clamped transistor logic for minimum propagation delay and employs PNP input transistors so that input currents are low, allowing a large fan-out for this circuit which is needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

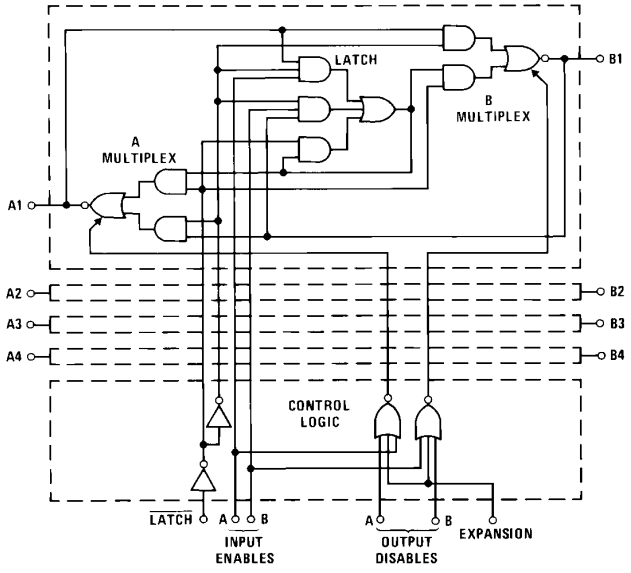
The DS3647A features TRI-STATE outputs. The "B" port outputs are designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA.

Data going from port "A" to port "B" and from "B" to port "A" is inverted in the DS3647A.

Features

- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL compatible
- Transmission line driver output

Logic and Connection Diagrams



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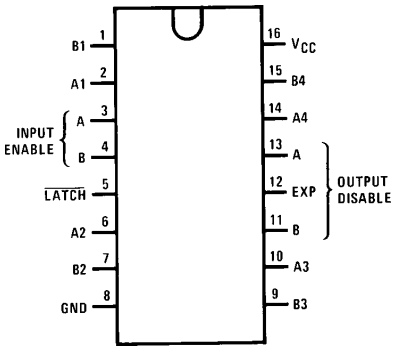
Dual-In-Line Package



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Top View

Order Number DS3647AD or DS3647AN
See NS Package Number D16C or N16A

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65° to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 10.0 mW/° C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS3647A	0	+70	° C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V	Latch, Disable Inputs		0.1	40	μA
			Expansion		0.2	80	μA
			A Ports, B Ports		0.2	100	μA
			Enable Inputs		0.4	200	μA
$I_{IN(0)}$	Logic "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V	Latch, Disable Inputs		−25	−250	μA
			Expansion		−50	−500	μA
			A Ports, B Ports		−50	−500	μA
			Enable, Inputs		−0.1	−1.25	mA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.6	−1.2	V
$V_{OL(A)}$	Logic "0" Output Voltage A Ports	V_{CC} = 4.5V, I_{OL} = 20 mA			0.4	0.5	V
$V_{OL(B)}$	Logic "0" Output Voltage B Ports	V_{CC} = 4.5V	I_{OL} = 30 mA		0.3	0.4	V
			I_{OL} = 50 mA		0.4	0.5	V
$V_{OH(A)}$	Logic "1" Output Voltage A Ports	I_{OH} = −1 mA	V_{CC} = 5V	3.0	3.4		V
			V_{CC} = 4.5V	2.5	3.4		V
$V_{OH(B)}$	Logic "1" Output Voltage B Ports	I_{OH} = −5.2 mA, (Note 4)	V_{CC} = 5V	2.9	3.3		V
			V_{CC} = 4.5V	2.4	3.3		V
$I_{OS(A)}$	Output Short-Circuit Current A Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Note 4)		−50	−80	−120	mA
$I_{OS(B)}$	Output Short-Circuit Current B Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Note 4)		−70	−120	−180	mA
I_{CC}	Power Supply Current	Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS3647A		100	140	mA
		Enable A, Latch = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS3647A		70	105	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Only one output at a time should be shorted.

Switching Characteristics (V_{CC} = 5V, T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA TRANSFER B PORT TO A PORT						
t_{pd0}	Propagation Delay to a Logic "0"	CL = 50 pF, R_L = 280Ω, *(Figures 1 and 4)*		7.5	15	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 280Ω, *(Figures 1 and 4)*		6.0	12	ns
A PORT CONTROL FROM OUTPUT DISABLE A INPUT						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 1 and 5)*		13	20	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 1 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 1 and 7)*		10	15	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 1 and 8)*		25	35	ns
DATA TRANSFER A PORT TO B PORT, DS3647A						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		6.5	12	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.0	15	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS3647A						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 2 and 5)*		15	25	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 2 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 2 and 7)*		10	16	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 2 and 8)*		25	35	ns
LATCH SET-UP AND HOLD TIMES, ALL DEVICES						
t_{SET-UP}	Set-Up Time of Data Input Before $\overline{\text{Latch}}$ Goes Low		5	0		ns
t_{HOLD}	Hold Time of Data Input After $\overline{\text{Latch}}$ Goes Low		10	5		ns

Product Description

Device Number	B Port To A Port Function	A Port To B Port Function	A Port Outputs	B Port Outputs
DS3647A	Inverting	Inverting	TRI-STATE	TRI-STATE

Truth Table

Input Enables		$\overline{\text{Latch}}$	Output Disables		Expansion	A Ports A1-A4	B Ports B1-B4	Comments
A	B		A	B				
1	0	1	0	0	0	Hi-Z	$\overline{A}$	Data in on A, output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Data in on B, output to A
1	0	0	0	0	0	Hi-Z	$\overline{A}$	Data stored which is present when $\overline{\text{latch}}$ goes low
0	1	0	0	0	0	$\overline{B}$	Hi-Z	Data stored which is present when $\overline{\text{latch}}$ goes low
1	0	x	0	1	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on A, may be latched
0	1	x	1	0	0	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data in on B, may be latched
x	x	x	x	x	1	Hi-Z	Hi-Z	Both A and B in Hi-Z state

AC Test Circuits

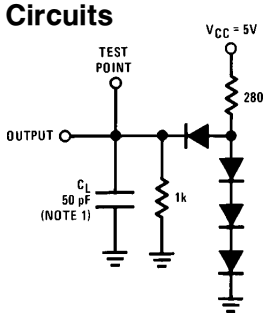

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FIGURE 1. A Port Load

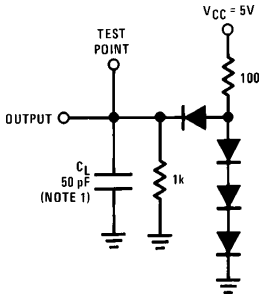

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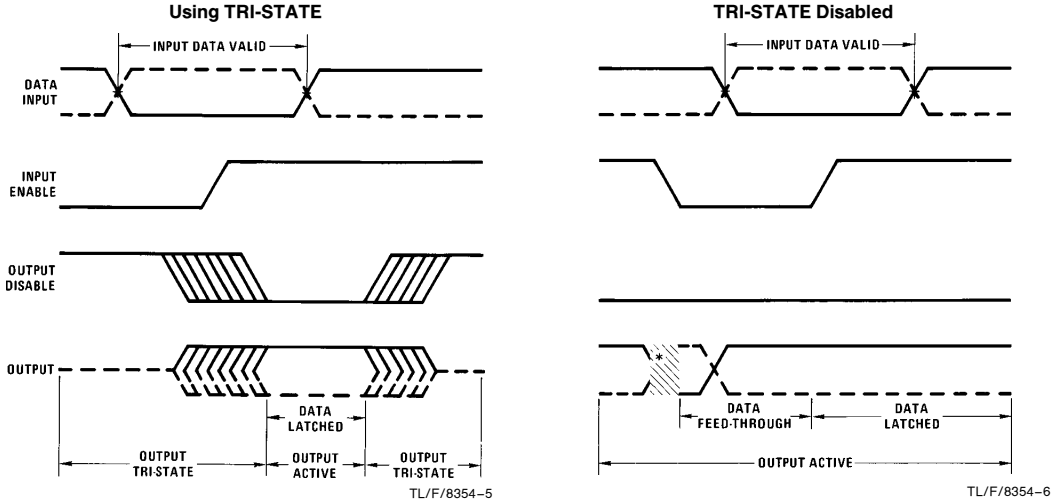
FIGURE 2. B Port Load

Note 1: C_L includes probe and jig capacitance.

Operating Waveforms



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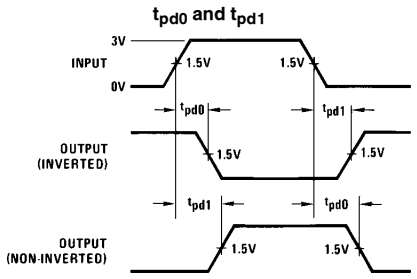
*When the Input Enable makes a negative transition, the output will be indeterminate for a short duration. The negative transition of the Input Enable normally occurs during a don't-care timing state at the output.

Switching Time Waveforms



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Input Characteristics: f = 1 MHz, $t_R = t_F \leq 5$ ns (10% to 90% points), duty cycle = 50%, $Z_{OUT} = 50\ \Omega$

FIGURE 4

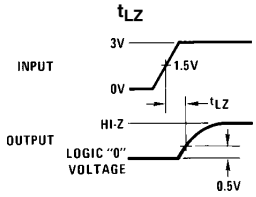

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FIGURE 5

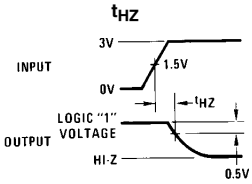

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FIGURE 6

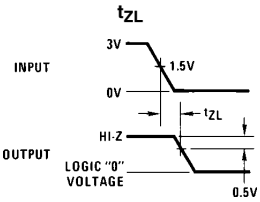

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FIGURE 7

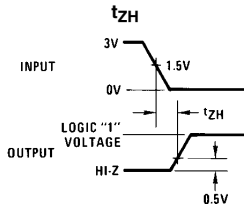

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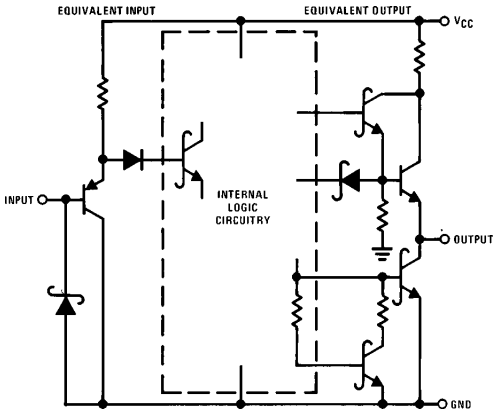
FIGURE 8

Schematic Diagram



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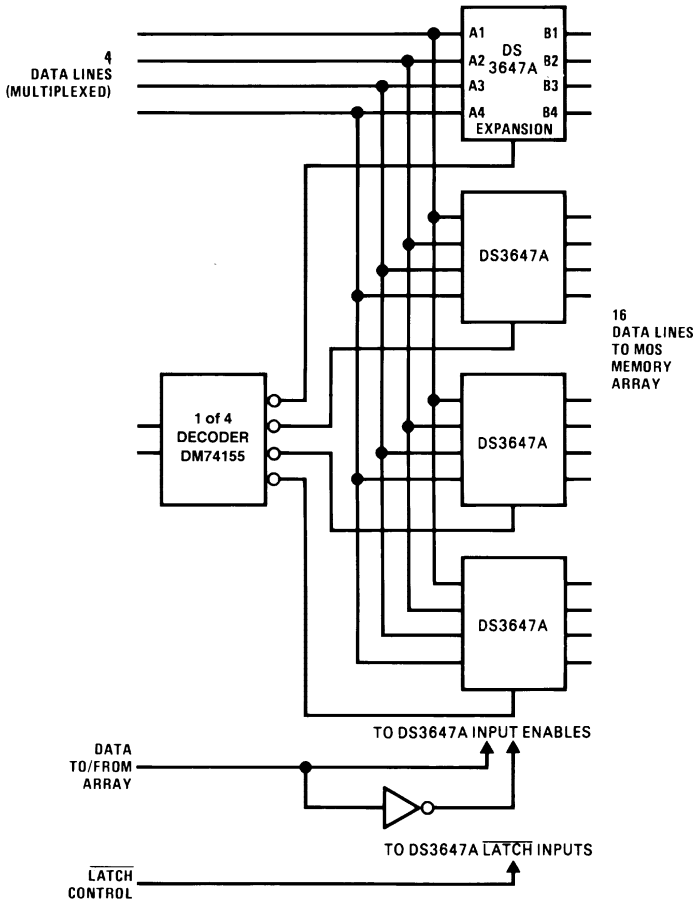
Note. Data pins A1–A4 and B1–B4 consist of an input and an output tied together.

Typical Application

The diagram below shows how the DS3647A can be used as a register capable of multiplexing data lines.



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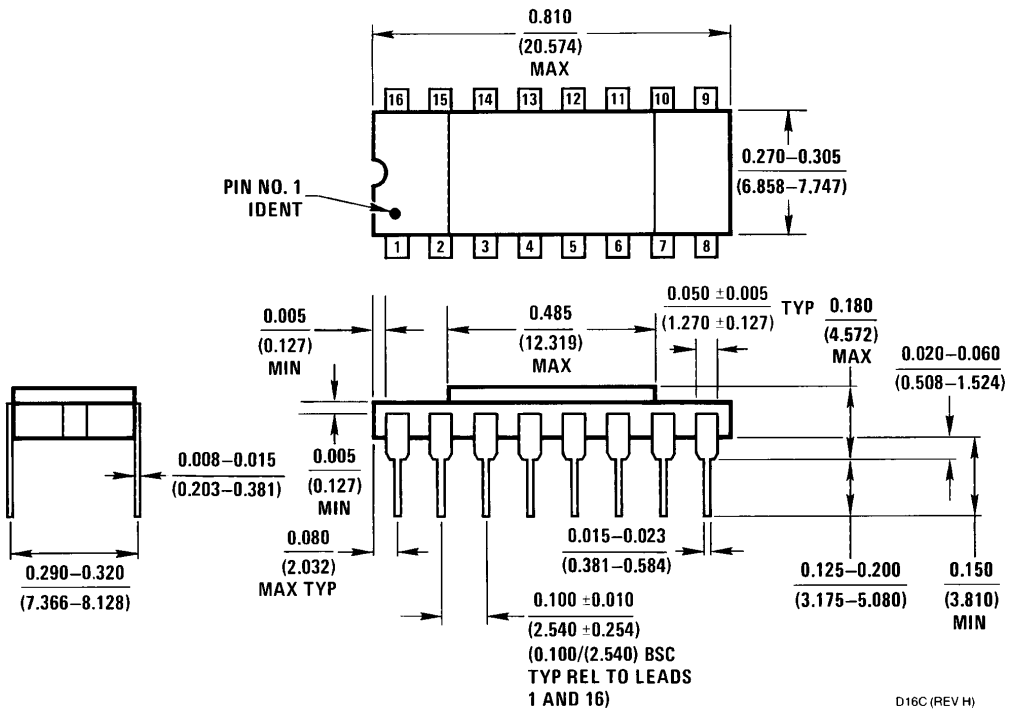
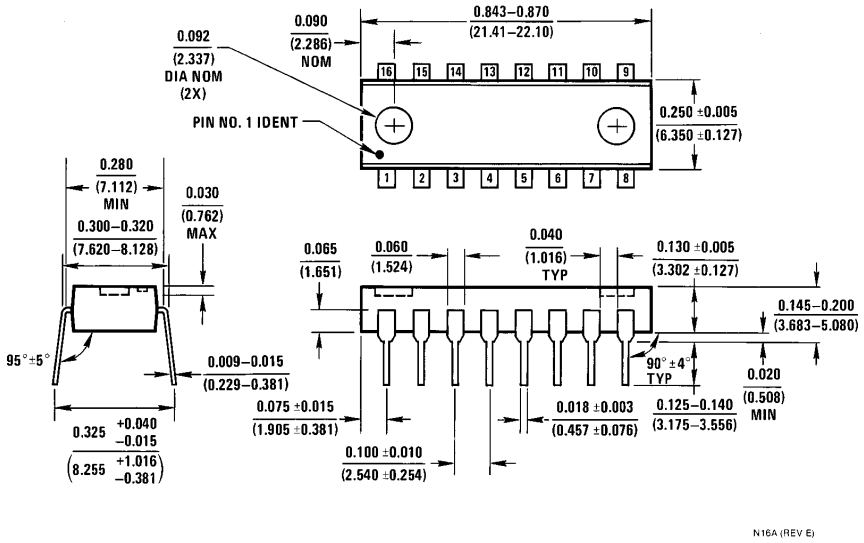
Physical Dimensions inches (millimeters)



Hermetic Dual-In-Line Package (D)
Order Number DS3647AD
NS Package D16C

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number DS3647AN
NS Package N16A

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