National Semiconductor

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DS40MB200
Dual 4 Gb/s 1:2 Mux/Buffer with Input Equalization and Output Pre-Emphasis

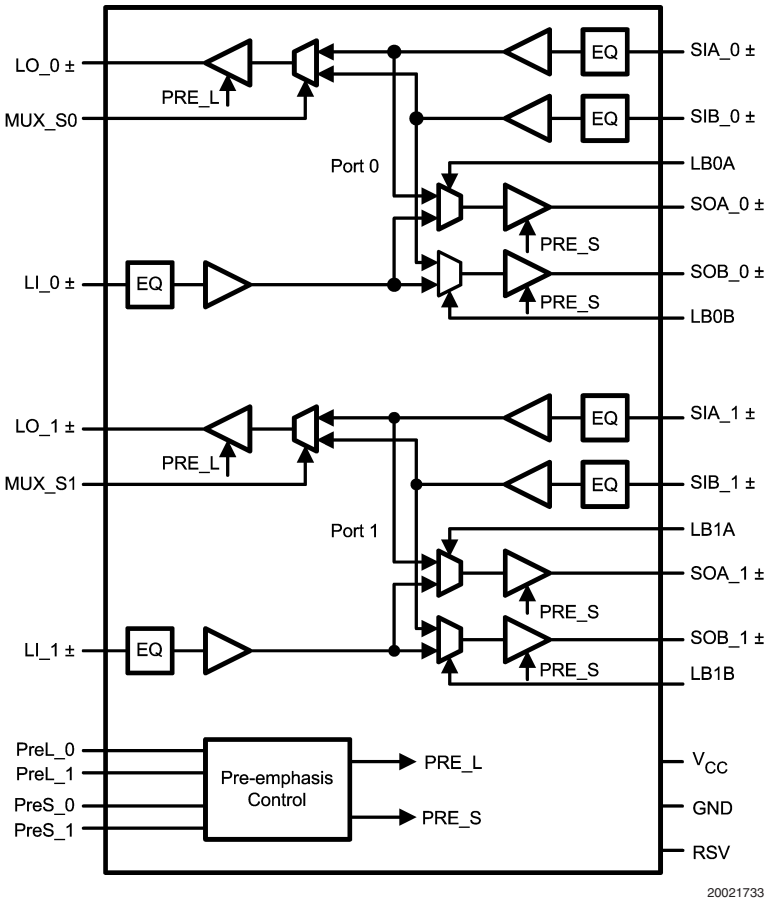
General Description

The DS40MB200 is a dual signal conditioning 2:1 multiplexer and 1:2 fan-out buffer designed for use in backplane redundancy applications. Signal conditioning features include input equalization and programmable output pre-emphasis that enable data communication in FR4 backplanes up to 4 Gb/s. Each input stage has a fixed equalizer to reduce ISI distortion from board traces. All output drivers have 4 selectable steps of pre-emphasis to compensate for transmission losses from long FR4 backplanes and reduce deterministic jitter. The pre-emphasis levels can be independently controlled for the line-side and switch-side drivers. The internal loopback paths from switch-side input to switch-side output enable at-speed system testing. All receiver inputs and driver outputs are internally terminated with 100Ω differential terminating resistors

Features

- Dual 2:1 multiplexer and 1:2 buffer
- 1– 4 Gbps fully differential data paths
- Fixed input equalization
- Programmable output pre-emphasis
- Independent switch and line side pre-emphasis controls
- Programmable switch-side loopback mode
- On-chip terminations
- +3.3V supply
- Low power, 1W max
- ESD rating HBM 6 kV
- Lead-less LLP-48 package (7mmx7mmx0.8mm, 0.5mm pitch)
- 0˚C to +85˚C operating temperature range

Functional Block Diagram



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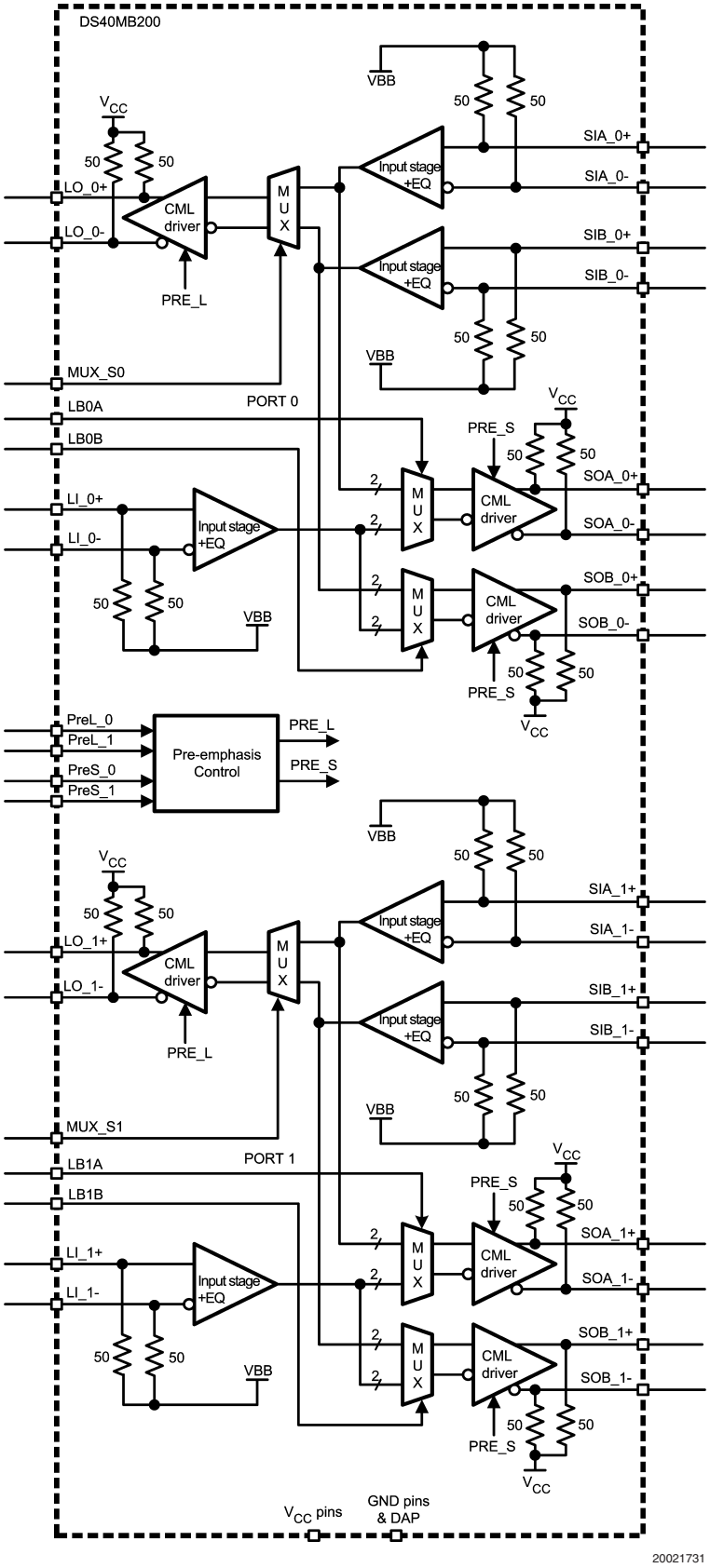
Simplified Block Diagram



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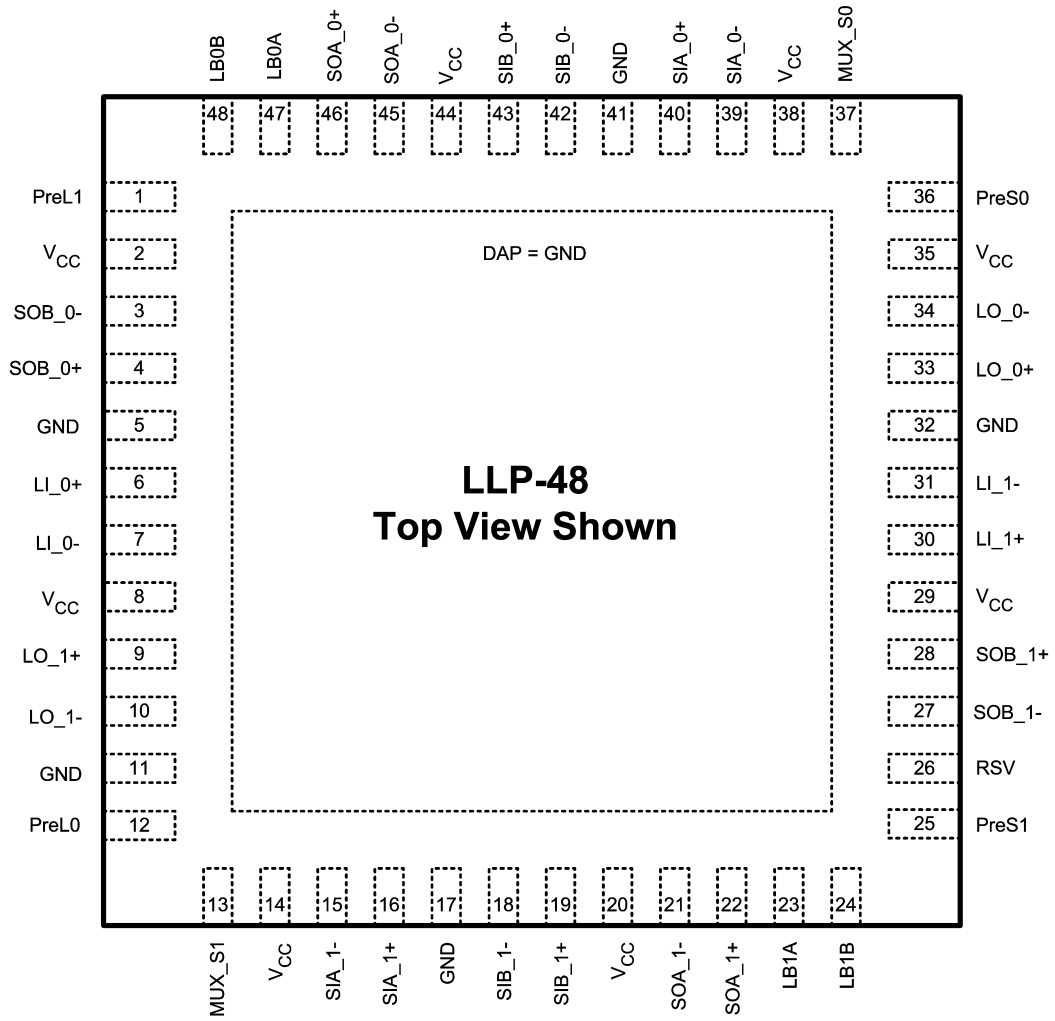
Connection Diagram



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Order number DS40MB200SQ
See NS Package Number SQA48D

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Pin Descriptions

Pin Name	Pin Number	I/O	Description
LINE SIDE HIGH SPEED DIFFERENTIAL IO's			
LI_0+ LI_0–	6 7	I	Inverting and non-inverting differential inputs of port_0 at the line side. LI_0+ and LI_0– have an internal 50Ω connected to an internal reference voltage.
LO_0+ LO_0–	33 34	O	Inverting and non-inverting differential outputs of port_0 at the line side. LO_0+ and LO_0– have an internal 50Ω connected to V_{CC}.
LI_1+ LI_1–	30 31	I	Inverting and non-inverting differential inputs of port_1 at the line side. LI_1+ and LI_1– have an internal 50Ω connected to an internal reference voltage.
LO_1+ LO_1–	9 10	O	Inverting and non-inverting differential outputs of port_1 at the line side. LO_1+ and LO_1– have an internal 50Ω connected to V_{CC}.
SWITCH SIDE HIGH SPEED DIFFERENTIAL IO's			
SOA_0+ SOA_0–	46 45	O	Inverting and non-inverting differential outputs of mux_0 at the switch_A side. SOA_0+ and SOA_0– have an internal 50Ω connected to V_{CC}.
SOB_0+ SOB_0–	4 3	O	Inverting and non-inverting differential outputs of mux_0 at the switch_B side. SOB_0+ and SOB_0– have an internal 50Ω connected to V_{CC}.
SIA_0+ SIA_0–	40 39	I	Inverting and non-inverting differential inputs to the mux_0 at the switch_A side. SIA_0+ and SIA_0– have an internal 50Ω connected to an internal reference voltage.
SIB_0+ SIB_0–	43 42	I	Inverting and non-inverting differential inputs to the mux_0 at the switch_B side. SIB_0+ and SIB_0– have an internal 50Ω connected to an internal reference voltage.
SOA_1+ SOA_1–	22 21	O	Inverting and non-inverting differential outputs of mux_1 at the switch_A side. SOA_1+ and SOA_1– have an internal 50Ω connected to V_{CC}.
SOB_1+ SOB_1–	28 27	O	Inverting and non-inverting differential outputs of mux_1 at the switch_B side. SOB_1+ and SOB_1– have an internal 50Ω connected to V_{CC}.
SIA_1+ SIA_1–	16 15	I	Inverting and non-inverting differential inputs to the mux_1 at the switch_A side. SIA_1+ and SIA_1– have an internal 50Ω connected to an internal reference voltage.
SIB_1+ SIB_1–	19 18	I	Inverting and non-inverting differential inputs to the mux_1 at the switch_B side. SIB_1+ and SIB_1– have an internal 50Ω connected to an internal reference voltage.
CONTROL (3.3V LVCMOS)			
MUX_S0	37	I	A logic low at MUX_S0 selects mux_0 to switch B. MUX_S0 is internally pulled high. Default state for mux_0 is switch A.
MUX_S1	13		A logic low at MUX_S1 selects mux_1 to switch B. MUX_S0 is internally pulled high. Default state for mux_1 is switch A.
PREL_0 PREL_1	12 1	I	PREL_0 and PREL_1 select the output pre-emphasis of the line side drivers (LO_0± and LO_1±). PREL_0 and PREL_1 are internally pulled high. See *Table 3* for line side pre-emphasis levels.
PRES_0 PRES_1	36 25	I	PRES_0 and PRES_1 select the output pre-emphasis of the switch side drivers (SOA_0±, SOB_0±, SOA_1± and SOB_1±). PRES_0 and PRES_1 are internally pulled high. See *Table 4* for switch side pre-emphasis levels.
LB0A	47	I	A logic low at LB0A enables the internal loopback path from SIA_0± to SOA_0±. LB0A is internally pulled high.
LB0B	48	I	A logic low at LB0B enables the internal loopback path from SIB_0± to SOB_0±. LB0B is internally pulled high.
LB1A	23	I	A logic low at LB1A enables the internal loopback path from SIA_1± to SOA_1±. LB1A is internally pulled high.
LB1B	24	I	A logic low at LB1B enables the internal loopback path from SIB_1± to SOB_1±. LB1B is internally pulled high.
RSV	26	I	Reserve pin to support factory testing. This pin can be left open, or tied to GND, or tied to GND through an external pull-down resistor.

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Pin Descriptions (Continued)

Pin Name	Pin Number	I/O	Description
POWER			
V_{CC}	2, 8, 14, 20, 29, 35, 38, 44	P	V_{CC} = 3.3V ± 5%. Each V_{CC} pin should be connected to the V_{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V_{CC} pin. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each V_{CC} pin to ground plane.
GND	5, 11, 17, 32, 41	P	Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	Die Attach Pad (DAP) is the metal contact at the bottom side, located at the center of the LLP-48 package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.

Note: I = Input, O = Output, P = Power

Functional Description

The DS40MB200 is a signal conditioning 2:1 multiplexer and a 1:2 buffer designed to support port redundancy up to 4 Gb/s. Each input stage has a fixed equalizer that provides equalization to compensate about 5 dB of transmission loss from a short backplane trace (about 10 inches backplane). The output driver has pre-emphasis (driver-side equalization) to compensate the transmission loss of the backplane that it is driving. The driver conditions the output signal such that the lower frequency and higher frequency pulses reach approximately the same amplitude at the end of the backplane, and minimize the deterministic jitter caused by the amplitude disparity. The DS40MB200 provides 4 steps of user-selectable pre-emphasis ranging from 0, -3, -6 and –9 dB to handle different lengths of backplane. Figure 1 shows a driver pre-emphasis waveform. The pre-emphasis duration is 200ps nominal, corresponds to 0.75 bit-width at 4 Gb/s. The pre-emphasis levels of switch-side and line-side can be individually programmed.

The high speed inputs are self-biased to about 1.5V and are designed for AC coupling. The inputs are compatible to most AC coupling differential signals such as LVDS, LVPECL and CML.

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TABLE 1. LOGIC TABLE FOR MULTIPLEX CONTROLS

MUX_S0	**Mux Function**
0	MUX_0 select switch_B input, SIB_0±.
1 (default)	MUX_0 select switch_A input, SIA_0±.
MUX_S1	**Mux Function**
0	MUX_1 select switch_B input, SIB_1±.
1 (default)	MUX_1 select switch_A input, SIA_0±.

TABLE 2. LOGIC TABLE FOR LOOPBACK Controls

LB0A	**Loopback Function**
0	Enable loopback from SIA_0± to SOA_0±.
1 (default)	Normal mode. Loopback disabled.
LB0B	**Loopback Function**
0	Enable loopback from SIB_0± to SOB_0±.
1 (default)	Normal mode. Loopback disabled.
LB1A	**Loopback Function**
0	Enable loopback from SIA_1± to SOA_1±.
1 (default)	Normal mode. Loopback disabled.
LB1B	**Loopback Function**
0	Enable loopback from SIB_1± to SOB_1±.
1 (default)	Normal mode. Loopback disabled.

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Functional Description (Continued)

TABLE 3. LINE-SIDE PRE-EMPHASIS CONTROLS

PreL_[1:0]	Pre-Emphasis Level in mV_{PP} (VODB)	De-Emphasis Level in mV_{PP} (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 board trace
0 0	1200	1200	0	10 inches
0 1	1200	850	–3	20 inches
1 0	1200	600	–6	30 inches
1 1 (default)	1200	426	–9	40 inches

TABLE 4. SWITCH-SIDE PRE-EMPHASIS CONTROLS

PreS_[1:0]	Pre-Emphasis Level in mV_{PP} (VODB)	De-Emphasis Level in mV_{PP} (VODPE)	Pre-Emphasis in dB (VODPE/VODB)	Typical FR4 board trace
0 0	1200	1200	0	10 inches
0 1	1200	850	–3	20 inches
1 0	1200	600	–6	30 inches
1 1 (default)	1200	426	–9	40 inches

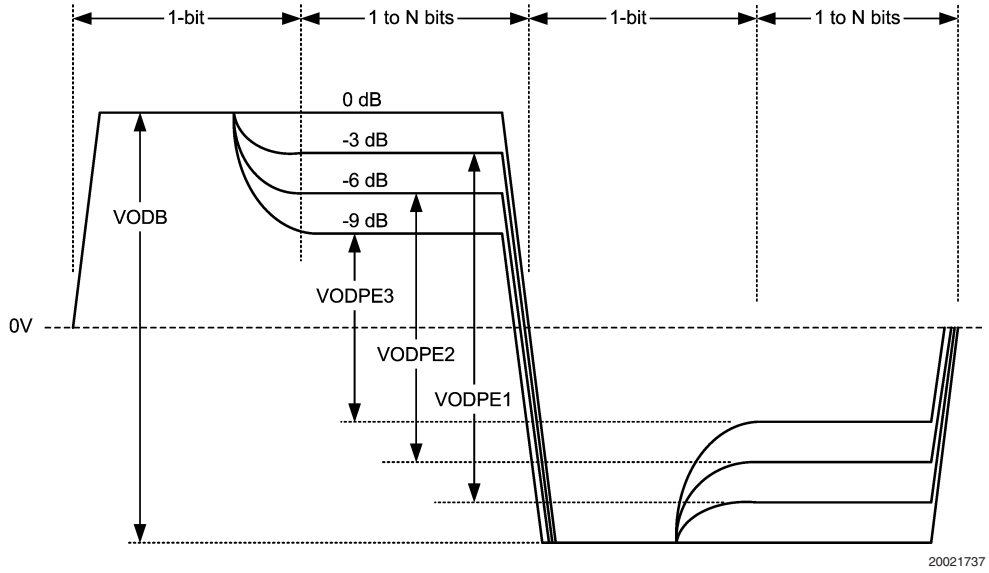

FIGURE 1. Driver Pre-Emphasis Differential Waveform (showing all 4 pre-emphasis steps)

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to 4V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} +0.3V)
CML Input/Output Voltage	−0.3V to (V_{CC} +0.3V)
Junction Temperature	+125˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature	
Soldering, 4 sec	+260˚C
Thermal Resistance, θ_{JA}	33.7˚C/W
Thermal Resistance, $\theta_{JC\text{-}top}$	20.7˚C/W
Thermal Resistance, $\theta_{JC\text{-}bottom}$	5.8˚C/W
Thermal Resistance,Φ_{JB}	18.2˚C/W
ESD Rating HBM, 1.5 kΩ, 100 pF	6 kV
ESD Rating Machine Model	250V

Recommended Operating Ratings

	Min	Typ	Max	Units
Supply Voltage (V_{CC}-GND)	3.135	3.3	3.465	V
Supply Noise Amplitude 10 Hz to 2 GHz			20	mV_{PP}
Ambient Temperature	0		85	˚C
Case Temperature			100	˚C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC} +0.3	V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	−10		10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND	75	94	124	µA
R_{PU}	Pull-High Resistance			35		kΩ
RECEIVER SPECIFICATIONS						
V_{ID}	Differential Input Voltage Range	AC Coupled Differential Signal Below 1.25 Gb/s At 1.25 Gbps–3.125 Gbps Above 3.125 Gbps This parameter is not production tested.	 100 100 100		 1750 1560 1200	 $mV_{P\text{-}P}$ $mV_{P\text{-}P}$ $mV_{P\text{-}P}$
V_{ICM}	Common Mode Voltage at Receiver Inputs	Measured at receiver inputs reference to ground.		1.3		V
R_{ITD}	Input Differential Termination	On-chip differential termination between IN+ or IN−.	84	100	116	Ω
R_{ITSE}	Input Termination (single-end)	On-chip termination IN+ or IN− to GND for frequency > 100 MHz.		50		Ω
DRIVER SPECIFICATIONS						
VODB	Output Differential Voltage Swing without Pre-Emphasis	R_L = 100Ω ±1% PRES_1=PRES_0=0 PREL_1=PREL_0=0 Driver pre-emphasis disabled. Running K28.7 pattern at 4 Gbps. See *Figure 5* for test circuit.	1000	1200	1400	$mV_{P\text{-}P}$

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Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
DRIVER SPECIFICATIONS						
V_{PE}	Output Pre-Emphasis Voltage Ratio 20*log(VODPE/VODB)	R_L = 100Ω ±1% Running K28.7 pattern at 4 Gbps PREx_[1:0]=00 PREx_[1:0]=01 PREx_[1:0]=10 PREx_[1:0]=11 x=S for switch side pre-emphasis control x=L for line side pre-emphasis control See *Figure 1* on waveform. See *Figure 5* for test circuit.		 0 −3 −6 −9		 dB dB dB dB
t_{PE}	Pre-Emphasis Width (Note 8)	Tested at −9 dB pre-emphasis level, PREx[1:0]=11 x=S for switch side pre-emphasis control x=L for line side pre-emphasis control See *Figure 4* on measurement condition.	125	200	250	ps
R_{OTSE}	Output Termination	On-chip termination from OUT+ or OUT− to V_{CC}	42	50	58	Ω
R_{OTD}	Output Differential Termination	On-chip differential termination between OUT+ and OUT−		100		Ω
ΔR_{OTSE}	Mis-Match in Output Termination Resistors	Mis-match in output terminations at OUT+ and OUT−			5	%
V_{OCM}	Output Common Mode Voltage			2.7		V
POWER DISSIPATION						
P_D	Power Dissipation	V_{DD} = 3.465V All outputs terminated by 100Ω ±1%. PREL_[1:0]=0, PRES_[1:0]=0 Running PRBS 2^7-1 pattern at 4 Gbps			1	W
AC CHARACTERISTICS						
t_R	Differential Low to High Transition Time	Measured with a clock-like pattern at 100 MHz, between 20% and 80% of the differential output voltage. Pre-emphasis disabled. Transition time is measured with fixture as shown in *Figure 5*, adjusted to reflect the transition time at the output pins.		80		ps
t_F	Differential High to Low Transition Time			80		ps
t_{PLH}	Differential Low to High Propagation Delay	Measured at 50% differential voltage from input to output.		0.5	2	ns
t_{PHL}	Differential High to Low Propagation Delay			0.5	2	ns
t_{SKP}	Pulse Skew (Note 8)	$\lvert t_{PHL} - t_{PLH} \rvert$			20	ps
t_{SKO}	Output Skew (Notes 7, 8)	Difference in propagation delay among data paths in the same device.			200	ps
t_{SKPP}	Part-to-Part Skew (Note 8)	Difference in propagation delay between the same output from devices operating under identical condition.			500	ps

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Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
AC CHARACTERISTICS						
t_{SM}	Mux Switch Time	Measured from V_{IH} or V_{IL} of the mux-control or loopback control to 50% of the valid differential output.		1.8	6	ns
RJ	Device Random Jitter (Note 5) (Note 8)	See *Figure 5* for test circuit. Alternating-1-0 pattern. Pre-emphasis disabled. At 1.25 Gbps At 4 Gbps			 2 2	 psrms psrms
DJ	Device Deterministic Jitter (Note 6) (Note 8)	See *Figure 5* for test circuit. Pre-emphasis disabled. At 4 Gbps, PRBS7 pattern			 30	 pspp
DR_{MAX}	Maximum Data Rate (Note 8)	Tested with alternating-1-0 pattern	4			Gbps

Note 1: "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Typical parameters measured at V_{CC} = 3.3V, T_A = 25˚C. They are for reference purposes and are not production-tested.

Note 3: IN+ and IN– are generic names refer to one of the many pairs of complimentary inputs of the DS40MB200. OUT+ and OUT– are generic names refer to one of the many pairs of the complimentary outputs of the DS40MB200. Differential input voltage V_{ID} is defined as |IN+–IN–|. Differential output voltage V_{OD} is defined as |OUT+–OUT–|.

Note 4: K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000}

K28.5 pattern is a 20-bit repeating pattern of +K28.5 and –K28.5 code groups {110000 0101 001111 1010}

Note 5: Device output random jitter is a measurement of the random jitter contribution from the device. It is derived by the equation sqrt(RJ_{OUT}^2– RJ_{IN}^2), where RJ_{OUT} is the total random jitter measured at the output of the device in psrms, RJ_{IN} is the random jitter of the pattern generator driving the device.

Note 6: Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation (DJ_{OUT}–DJ_{IN}), where DJ_{OUT} is the total peak-to-peak deterministic jitter measured at the output of the device in pspp, DJ_{IN} is the peak-to-peak deterministic jitter of the pattern generator driving the device.

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Note 7: t_{SKO} is the magnitude difference in the propagation delays among data paths between switch A and switch B of the same port and similar data paths between port 0 and port 1. An example is the output skew among data paths from SIA_0± to LO_0±, SIB_0± to LO_0±, SIA_1± to LO_1± and SIB_1± to LO_1±. Another example is the output skew among data paths from LI_0± to SOA_0±, LI_0± to SOB_0±, LI_1± to SOA_1± and LI_1± to SOB_1±. t_{SKO} also refers to the delay skew of the loopback paths of the same port and between similar data paths between port 0 and port 1. An example is the output skew among data paths SIA_0± to SOA_0±, SIB_0± to SOB_0±, SIA_1± to SOA_1± and SIB_1± to SOB_1±.

Note 8: Guaranteed by desigh and characterization using statistical analysis.

Timing Diagrams

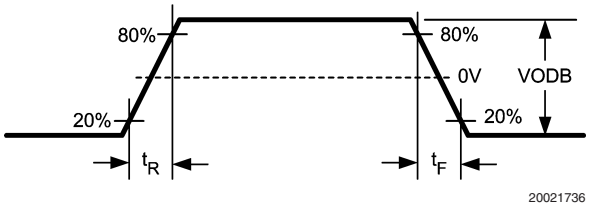

FIGURE 2. Driver Output Transition Time

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Timing Diagrams (Continued)

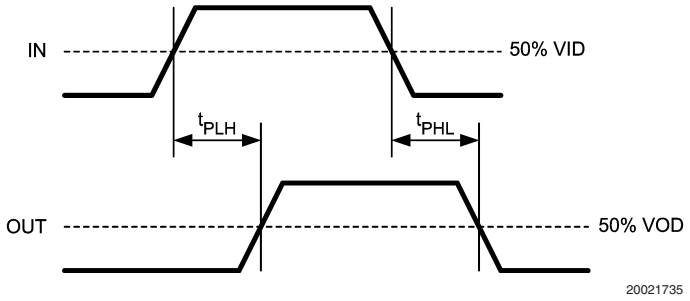

FIGURE 3. Propagation Delay from input to output

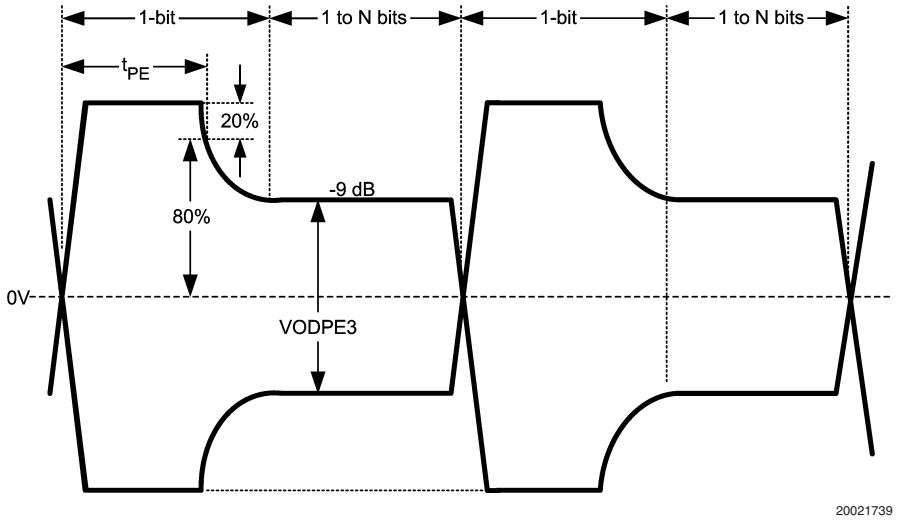

FIGURE 4. Test condition for output pre-emphasis duration

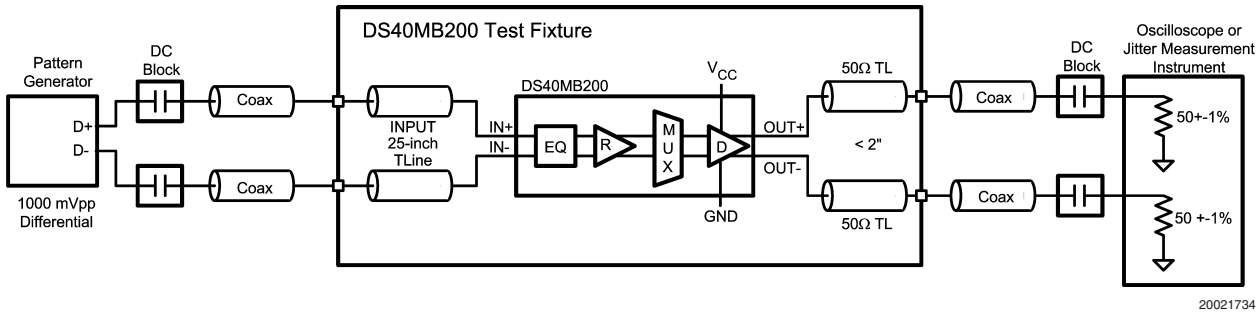

FIGURE 5. AC Test Circuit

The DS40MB200 input equalizer provides equalization to compensate about 5 dB of transmission loss from a short backplane transmission line. For characterization purposes, a 25-inch FR4 coupled micro-strip board trace is used in place of the short backplane link. The 25-inch microstrip board trace has approximately 5 dB of attenuation between 375 MHz and 1.875 GHz, representing closely the transmission loss of the short backplane transmission line. The 25-inch microstrip is connected between the pattern generator and the differential inputs of the DS40MB200 for AC measurements.

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Timing Diagrams (Continued)

Trace Length	Finished Trace Width W	Separation between Traces	Dielectric Height H	Dielectric Constant ϵ_R	Loss Tangent
25 inches	8.5 mil	11.5 mil	6 mil	3.8	0.022

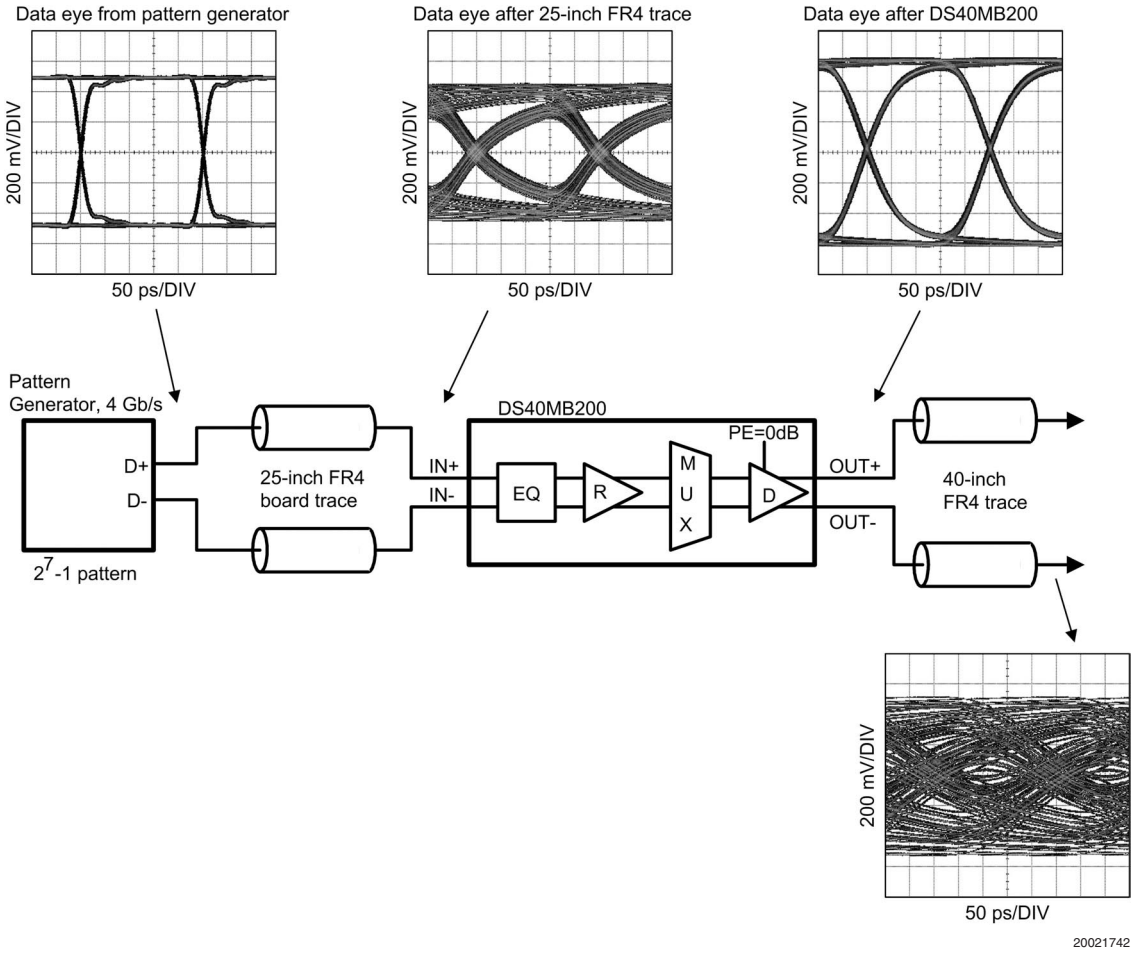

FIGURE 6. Data input and output eye patterns with driver set to 0 dB pre-emphasis

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Timing Diagrams (Continued)

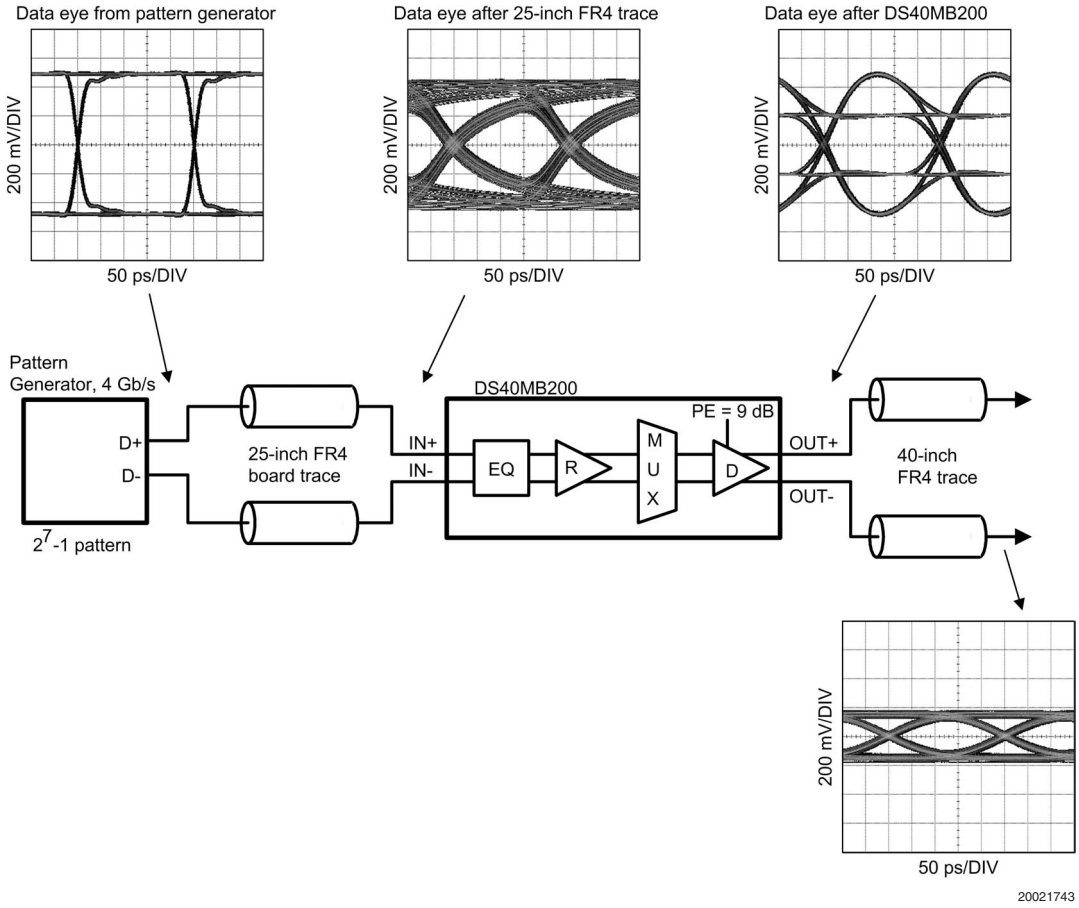

FIGURE 7. Data input and output eye patterns with driver set to 9dB pre-emphasis

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Application Information

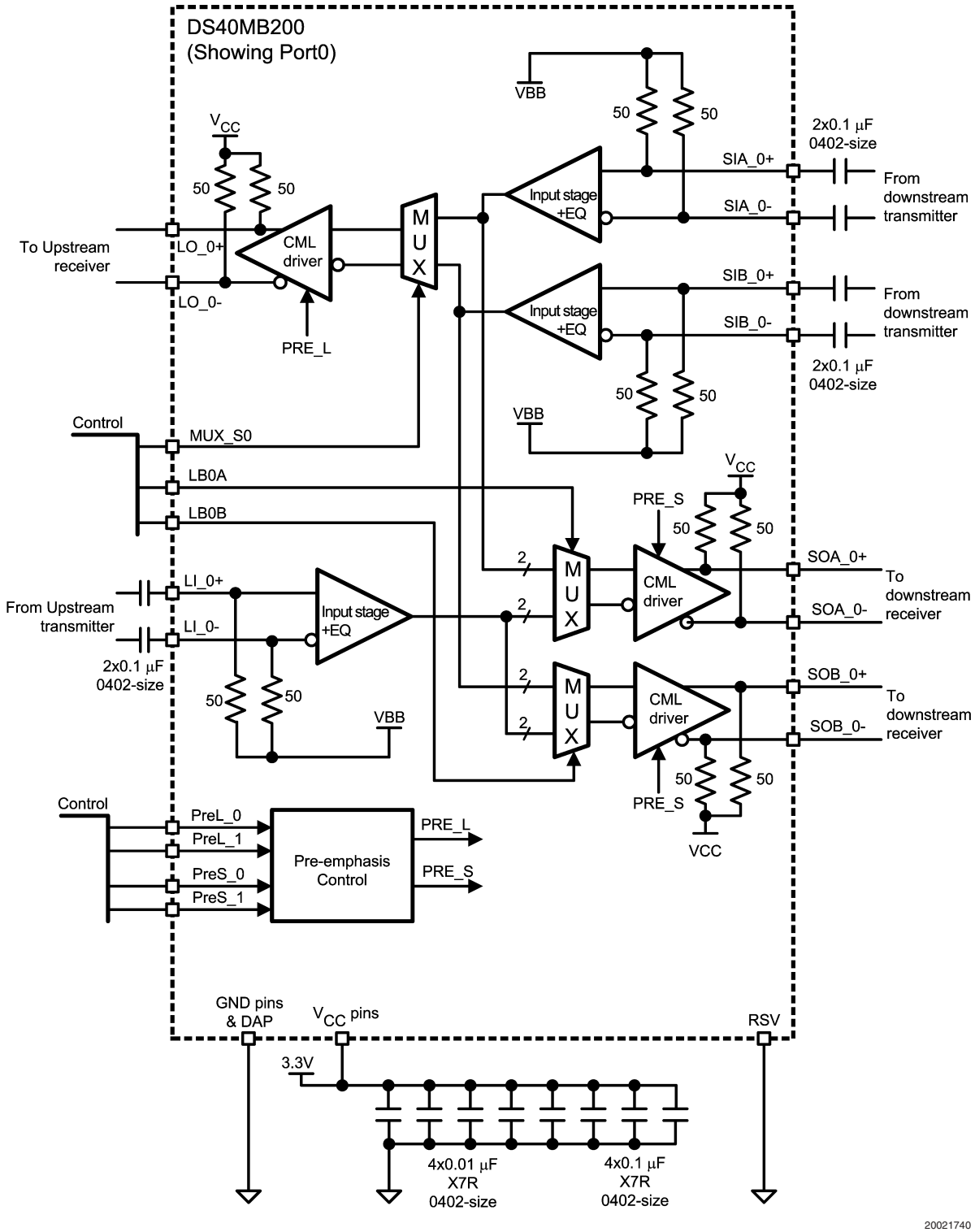

FIGURE 8. Application diagram (showing data paths of port 0)

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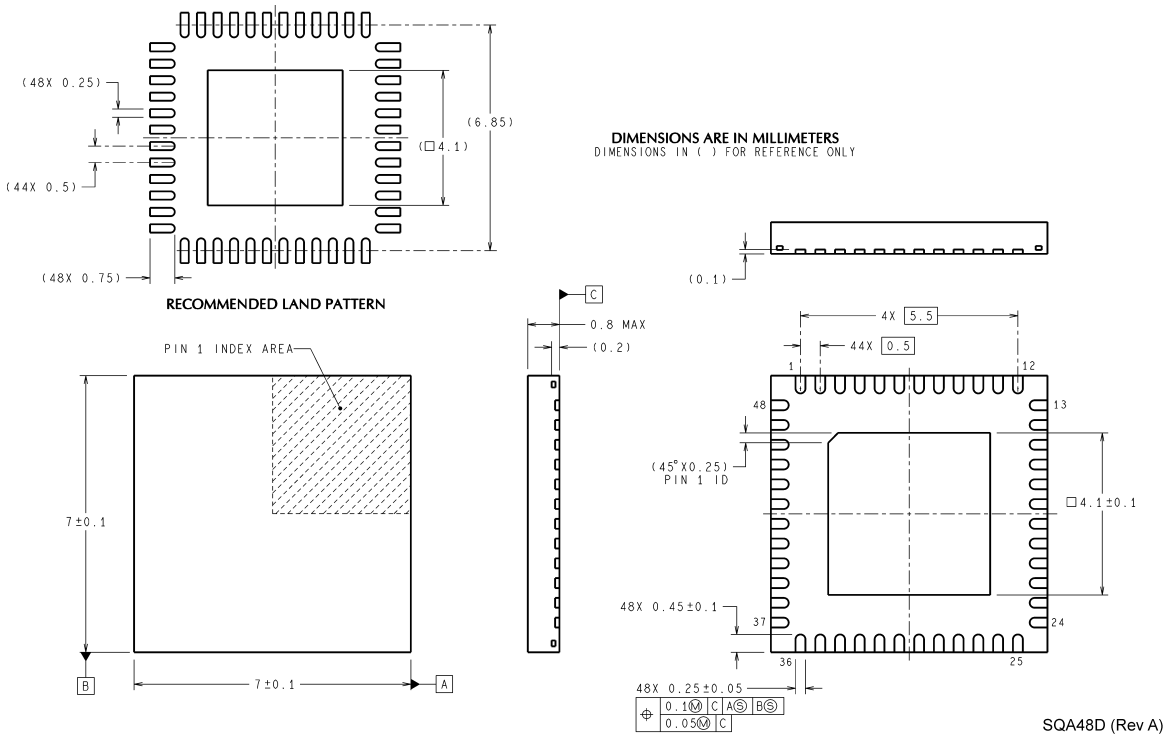
Physical Dimensions inches (millimeters) unless otherwise noted



LLP-48 Package

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