



DS4-XO Series Crystal Oscillators

General Description

The DS4125, DS4155, DS4156, DS4160, DS4311, DS4312, DS4622, and DS4776 ceramic surface-mount crystal oscillators are part of Maxim's DS4-XO series crystal oscillators family. These devices offer output frequencies at 125MHz, 155.52MHz, 156.25MHz, 160MHz, 311.04MHz, 312.5MHz, 622.08MHz, and 77.76MHz. The clock oscillators are suited for systems with tight tolerances because of the jitter, phase noise, and stability performance. The small package provides a format made for applications where PCB space is critical.

These clock oscillators are crystal based and use a fundamental crystal with PLL technology to provide the final output frequencies. Each device is offered with LVDS or LVPECL output types. The output enable pin is active-high logic.

These clock oscillators have very low phase jitter and phase noise. Typical phase jitter is $< 0.6\text{ps}_{\text{RMS}}$ from 12kHz to 20MHz. The devices are designed to operate with a $3.3\text{V} \pm 5\%$ supply voltage, and are available in a $5.0\text{mm} \times 3.2\text{mm} \times 1.49\text{mm}$, 10-pin LCCC surface-mount ceramic package.

Applications

Infiniband
BPON/GPON
Ethernet
10GbE
SONET/SDH

Pin Configuration and Selector Guide appear at end of data sheet.

Features

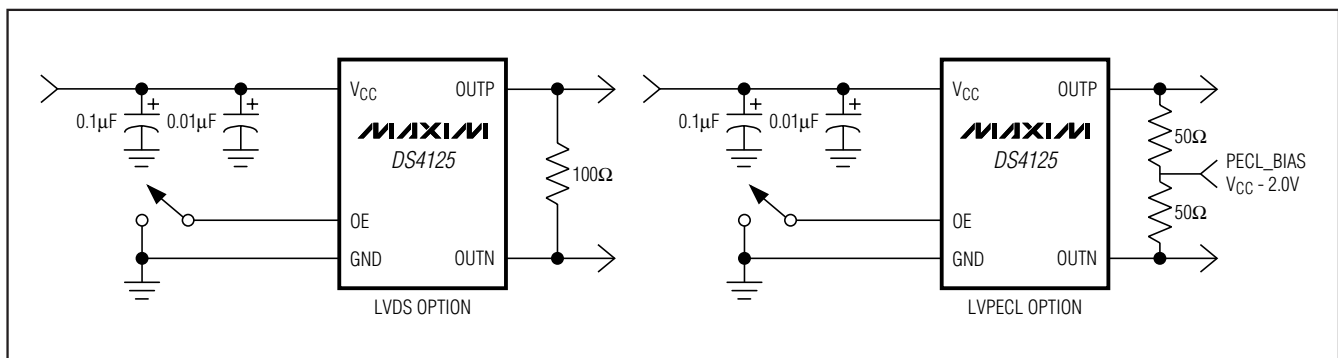
- ◆ $< 0.6\text{ps}_{\text{RMS}}$ from 12kHz to 20MHz Jitter
- ◆ LVDS or LVPECL Output Types
- ◆ 3.3V Operating Voltage
- ◆ $5.0\text{mm} \times 3.2\text{mm} \times 1.49\text{mm}$, 10-Pin LCCC Ceramic Package
- ◆ -40°C to $+85^\circ\text{C}$ Operating Temperature Range
- ◆ Lead Free/RoHS Compliant

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------------|--|-------------|
| DS4125D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4125P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4155D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4155P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4156D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4156P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4160D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4160P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4311D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4311P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4312D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4312P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4622D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4622P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4776D+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |
| DS4776P+ | -40°C to $+85^\circ\text{C}$ | 10 LCCC |

+ Denotes a lead-free package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Typical Operating Circuits



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ABSOLUTE MAXIMUM RATINGS

| | |
|--|--|
| Power-Supply Voltage (V _{CC}).....-0.3V, +4V | Storage Temperature Range-55°C to +85°C |
| Operating Temperature Range-40°C to +85°C | Soldering Temperature Profile |
| Junction Temperature+150°C | (3 passes max of reflow).....See IPC/JEDEC J-STD-020 Specification |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.135V to 3.465V, T_A = -40°C to +85°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------------|--|-----------------------|------------------|-----------------------|-------|
| Operating Voltage Range | V _{CC} | (Note 1) | 3.135 | 3.3 | 3.465 | V |
| Operating Current | I _{CC_D} | LVDS, output loaded or unloaded | | 50 | 70 | mA |
| | I _{CC_PU} | LVPECL, output unloaded | | 45 | 65 | |
| | I _{CC_PI} | LVPECL, output load 50Ω at V _{CC} - 2.0V | | 70 | 95 | |
| Output Frequency | f _{OUT} | | | f _{NOM} | | MHz |
| Oscillator Startup Time | t _{STARTUP} | (Note 2) | | | 50 | ms |
| Frequency Stability | Δf _{TOTAL} | Over temperature range, aging, load, supply, and initial tolerance (Note 3) | -50 | f _{NOM} | +50 | ppm |
| Frequency Stability Over Temperature with Initial Tolerance | Δf _{TEMP} | V _{CC} = 3.3V | -35 | | +35 | ppm |
| Initial Tolerance | Δf _{INITIAL} | V _{CC} = 3.3V, T _A = +25°C | | ±20 | | ppm |
| Frequency Change Due to ΔV _{CC} | Δf _{VCC} | V _{CC} = 3.3V ±5% | -3 | | +3 | ppm/V |
| Frequency Change Due to Load Variation | Δf _{LOAD} | ±10% variation in termination resistance | | ±1 | | ppm |
| Aging (15 Years) | Δf _{AGING} | | -7 | | +7 | ppm |
| Jitter | J _{RMS} | Integrated phase RMS; 12kHz to 5MHz, V _{CC} = 3.3V, T _A = +25°C | | < 0.5 | | ps |
| | | Integrated phase RMS; 12kHz to 20MHz, V _{CC} = 3.3V, T _A = +25°C | | < 0.6 | | |
| | | Integrated phase RMS; 12kHz to 80MHz, V _{CC} = 3.3V, T _A = +25°C | | < 1.0 | | |
| Input-Voltage High (OE) | V _{IH} | (Note 1) | 0.7 x V _{CC} | | V _{CC} | V |
| Input-Voltage Low (OE) | V _{IL} | (Note 1) | 0 | | 0.3 x V _{CC} | V |
| Input Leakage (OE) | I _{LEAK} | GND ≤ OE ≤ V _{CC} | -50 | | +5.0 | μA |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 3.135V$ to $3.465V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------|---|------------------|-------|-----------------|----------|
| LVDS | | | | | | |
| Output High Voltage | $V_{OHLVDSO}$ | 100 Ω differential load (Note 1) | | | 1.475 | V |
| Output Low Voltage | $V_{OLLVDSO}$ | 100 Ω differential load (Note 1) | 0.925 | | | V |
| Differential Output Voltage | $ V_{ODLVDSO} $ | 100 Ω differential load | 250 | | 425 | mV |
| Output Common-Mode Voltage Variation | $V_{LVDSOCOM}$ | 100 Ω differential load | | | 150 | mV |
| Change in Differential Magnitude or Complementary Inputs | $\Delta V_{ODLVDSO} $ | 100 Ω differential load | | | 25 | mV |
| Offset Output Voltage | $V_{OFFLVDSO}$ | 100 Ω differential load (Note 1) | 1.125 | | 1.275 | V |
| Differential Output Impedance | R_{OLVDSO} | | 80 | | 140 | Ω |
| Output Current | $I_{VSSLVDSO}$ | OUTN or OUTP shorted to ground and measure the current in the shorting path | | | 40 | mA |
| | I_{LVDSO} | OUTN or OUTP shorted together | | 6.5 | | |
| Output Rise Time (Differential) | t_{RLVDSO} | 20% to 80% | | 175 | | ps |
| Output Fall Time (Differential) | t_{FLVDSO} | 80% to 20% | | 175 | | ps |
| Duty Cycle | D_{CYCLE_LVDS} | | 45 | | 55 | % |
| Propagation Delay from OE Going LOW to Logical 1 at OUTP | t_{PA1} | | | | 200 | ns |
| Propagation Delay from OE Going HIGH to Output Active | t_{P1A} | | | | 200 | ns |
| LVPECL | | | | | | |
| Output High Voltage | V_{OH} | Output connected to 50 Ω at PECL_BIAS at $V_{CC} - 2.0V$ | $V_{CC} - 1.085$ | | $V_{CC} - 0.88$ | V |
| Output Low Voltage | V_{OL} | Output connected to 50 Ω at PECL_BIAS at $V_{CC} - 2.0V$ | $V_{CC} - 1.825$ | | $V_{CC} - 1.62$ | V |
| Differential Voltage | V_{DIFF_PECL} | Output connected to 50 Ω at PECL_BIAS at $V_{CC} - 2.0V$ | 0.595 | 0.710 | | V |
| Rise Time | t_{R-PECL} | | | 200 | | ps |
| Fall Time | t_{F-PECL} | | | 200 | | ps |
| Duty Cycle | D_{CYCLE_PECL} | | 45 | | 55 | % |
| Propagation Delay from OE Going LOW to Output High Impedance | t_{PAZ} | | | | 200 | ns |
| Propagation Delay from OE Going HIGH to Output Active | t_{PZA} | | | | 200 | ns |

Note 1: All voltages referenced to ground.

Note 2: AC parameters are guaranteed by design and not production tested.

Note 3: Frequency stability is calculated as: $\Delta f_{TOTAL} = \Delta f_{INITIAL} + \Delta f_{TEMP} + (\Delta f_{VCC} \times 0.165) + \Delta f_{LOAD} + \Delta f_{AGING}$.

DS4125/DS4155/DS4156/DS4160/DS4311/DS4312/DS4622/DS4776

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SINGLE-SIDEBAND PHASE NOISE AT $f_0 = f_{NOM}$

| $f_M =$ | SINGLE-SIDEBAND PHASE NOISE AT $f_0 = f_{NOM}$ (dBc/Hz) | | | | | | | |
|---------|---|-----------|-----------|-----------|-----------|-----------|----------|-----------|
| | 77.76MHz | 125.00MHz | 155.52MHz | 156.25MHz | 160.00MHz | 311.04MHz | 312.5MHz | 622.08MHz |
| 10Hz | -60 | -70 | -70 | -70 | -70 | -65 | -65 | -60 |
| 100Hz | -95 | -100 | -100 | -100 | -100 | -95 | -95 | -90 |
| 1kHz | -122 | -120 | -120 | -120 | -120 | -113 | -113 | -107 |
| 10kHz | -126 | -120 | -120 | -120 | -120 | -113 | -113 | -107 |
| 100kHz | -131 | -125 | -125 | -125 | -125 | -118 | -118 | -113 |
| 1MHz | -143 | -142 | -142 | -142 | -142 | -137 | -137 | -131 |
| 10MHz | -149 | -149 | -149 | -149 | -149 | -149 | -149 | -147 |
| 20MHz | -153 | -153 | -153 | -153 | -153 | -153 | -153 | -150 |

Pin Description

| PIN | NAME | FUNCTION |
|---------|------|---|
| 1 | OE | Active-High Output Enable. Has an internal pullup 100kΩ resistor. |
| 2, 7–10 | N.C. | No Connection. Must be floated. |
| 3 | GND | Ground |
| 4 | OUTP | Positive Output for LVPECL or LVDS |
| 5 | OUTN | Negative Output for LVPECL or LVDS |
| 6 | VCC | Supply Voltage |
| — | EP | Exposed Paddle. The exposed pad must be used for thermal relief. This pad can be connected to ground. |

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DS4125/DS4155/DS4156/DS4160/DS4311/DS4312/DS4622/DS4776

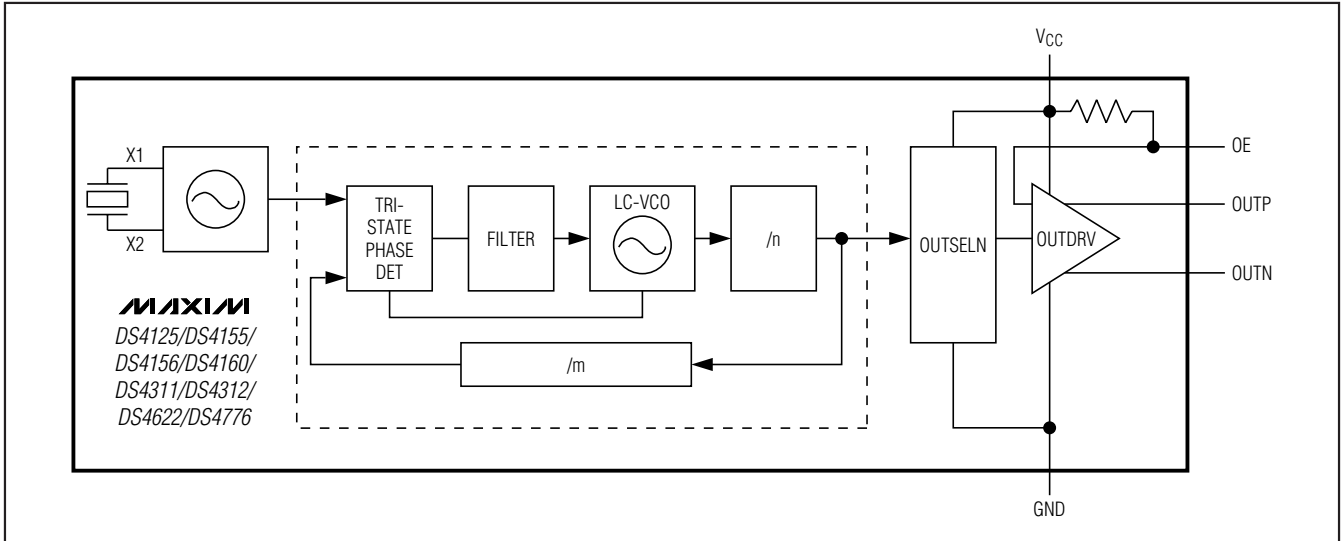


Figure 1. Functional Diagram

Detailed Description

The devices consist of a fundamental-mode, AT-cut crystal and a synthesizer IC that can synthesize any one of these frequencies: 77.76MHz, 125MHz, 155.52MHz, 156.25MHz, 160MHz, 311.04MHz, 312.5MHz, and 622.08MHz.

All devices support two types of differential output drivers: LVDS and LVPECL. When the OE signal is low,

LVPECL outputs go to the PECL_BIAS level of $V_{CC} - 2.0V$, while the LVDS outputs are a logical one. See Figures 2 and 3 for an LVDS and LVPECL output timing diagram.

Additional Information

For more available frequencies, refer to the DS4106 data sheet at www.maxim-ic.com/DS4106.

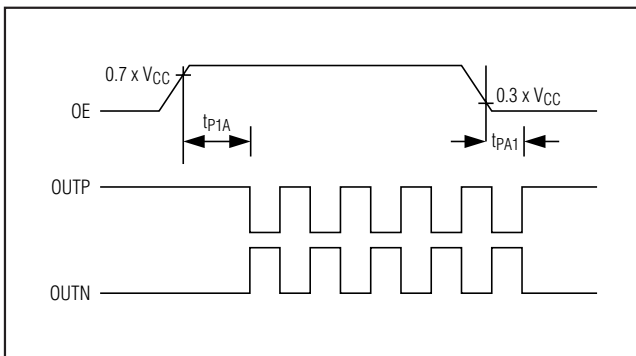


Figure 2. LVDS Output Timing Diagram When OE Is Enabled and Disabled

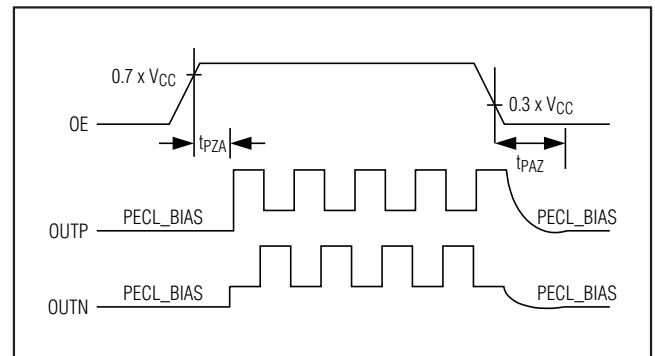


Figure 3. LVPECL Output Timing Diagram When OE Is Enabled and Disabled

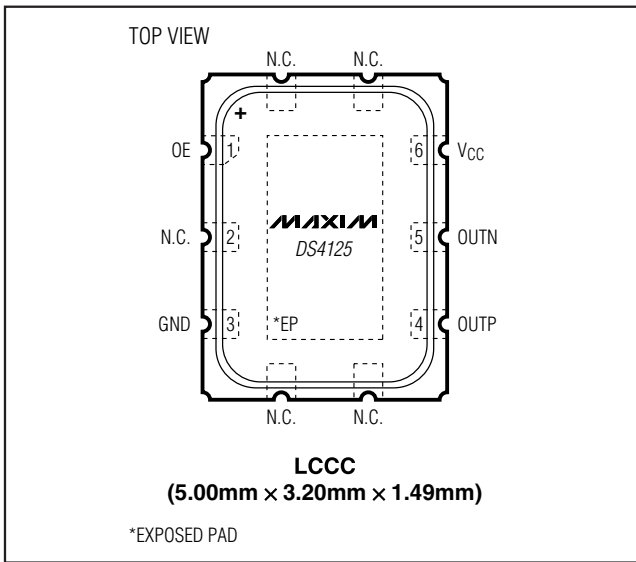
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Selector Guide

| PART | FREQUENCY (NOM) (MHz) | FREQUENCY STABILITY (ppm) | OUTPUT TYPE | TOP MARK |
|----------|-----------------------|---------------------------|-------------|----------|
| DS4125D+ | 125.00 | ±50 | LVDS | 25D |
| DS4125P+ | 125.00 | ±50 | LVPECL | 25P |
| DS4155D+ | 155.52 | ±50 | LVDS | 55D |
| DS4155P+ | 155.52 | ±50 | LVPECL | 55P |
| DS4156D+ | 156.25 | ±50 | LVDS | 56D |
| DS4156P+ | 156.25 | ±50 | LVPECL | 56P |
| DS4160D+ | 160.00 | ±50 | LVDS | 60D |
| DS4160P+ | 160.00 | ±50 | LVPECL | 60P |
| DS4311D+ | 311.04 | ±50 | LVDS | 31D |
| DS4311P+ | 311.04 | ±50 | LVPECL | 31P |
| DS4312D+ | 312.50 | ±50 | LVDS | 32D |
| DS4312P+ | 312.50 | ±50 | LVPECL | 32P |
| DS4622D+ | 622.08 | ±50 | LVDS | 62D |
| DS4622P+ | 622.08 | ±50 | LVPECL | 62P |
| DS4776D+ | 77.76 | ±50 | LVDS | 76D |
| DS4776P+ | 77.76 | ±50 | LVPECL | 76P |

+Denotes a lead-free package. The lead finish is JESD97 category e4 (Au over Ni) and is compatible with both lead-based and lead-free soldering processes.

Pin Configuration



Chip Information

SUBSTRATE CONNECTED TO GROUND
PROCESS: Bipolar SiGe

Thermal Information

| THETA-JA (°C/W) |
|-----------------|
| 90 |

Package Information

(For the latest package outline information go to www.maxim-ic.com/DallasPackInfo.)

| PACKAGE TYPE | DOCUMENT NO. |
|--------------|--------------|
| 10 LCCC | 56-G5032-002 |

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