Euvis
DS856 Datasheet

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1. Add more spectrum data

High-Speed Direct Digital Synthesizer
DS856
Clock Rate up to 3.2 GHz
32-bit Frequency Resolution
13-bit ROM Phase Resolution
11-bit DAC Amplitude Resolution
Up to 1.6 GHz Analog Outputs
64-Pin QFN Package

PRODUCT DESCRIPTION

The **DS856** is a high-speed Direct Digital Synthesizer (DDS) with a frequency tuning resolution of 32 bits, ROM phase resolution of 13-bit and a DAC amplitude resolution of 11 bits. Sine waves in the 1st Nyquist band can be generated up to near 1.6 GHz (at a 3.2-GHz clock rate). The initial phase can be reset to zero degrees to start with. The chip has a pair of complementary outputs with 50-Ω back terminations. The frequency of output waveforms can be controlled by thirty-two frequency control bits, **Vi[0:31]**. The **DS856** accepts either differential clock inputs or a single-ended clock input and features 50-Ω on-chip back terminations with user-defined threshold. The frequency resolution bits accept LVTTL or CMOS input levels. Only a single –5V power supply is required.

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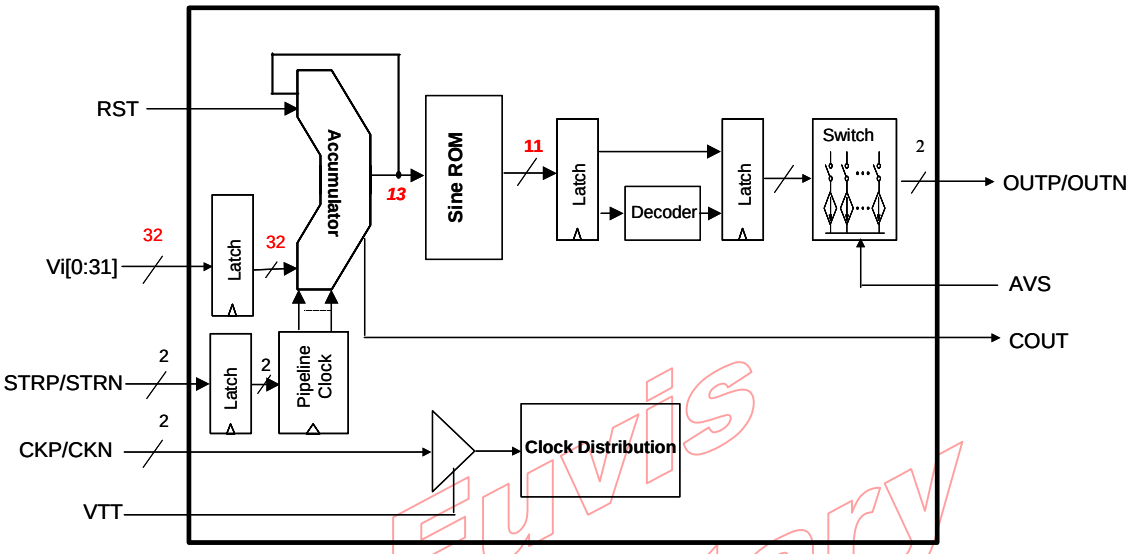
KEY FEATURES

- 32-bit frequency tuning word
- 13-bit ROM phase address resolution
- On chip DAC with 11 bit linearity
- Clock rate up to 3.2 GHz
- Sine wave generation up to 1.6 GHz
- Complementary analog waveform outputs with 50 Ω back terminations
- Carry bit RF output from phase accumulator for synchronization triggering of testing scope or system applications
- Worst SFDR > 45 dBc (DC to 1.6-GHz Bandwidth) at a 3.2 GHz clock rate
- LVTTL/CMOS digital pattern control input
- Reset (**RST**) pin to initiate phase 0 starting state
- High speed strobe inputs (**STR_P/N**) to update the frequency word and DAC output frequency
- High speed strobe inputs allow **DS856** to be controlled by micro-controller or DSP chips for real time chirping function
- Frequency update rate as fast as 8 clock cycles
- 3.5 W power consumption with a single -5V power supply
- 64-pin QFN package

BLOCK DIAGRAM



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ELECTRICAL SPECIFICATIONS & TYPICAL OPERATION CONDITIONS

V_{EE} = –5.0 V and R_L = 50 Ω (for DAC **OUT_P/N** Analog Outputs)

Parameter	Symbol	Min	Typical	Max	Unit
Ground[1]	VCC		0		V
Power Supply Voltage for Digital Circuits[2]	VEE	-4.5	-5.0	-5.5	V
Power Supply Voltage for DAC Digital Circuits[2]	VEED	-4.5	-5.0	-5.5	V
Power Supply Voltage for DAC Analog Circuits[2]	VEEA	-4.5	-5.0	-5.5	V
Total Power Supply Current	I_{EE}	650	700	750	mA
Operating Temperature	T_o	–40	25	85	°C
Highest Clock Rate	f_{cks}	3.0	3.2	3.4	GSPS
Clock Single Ended Input Amplitude	ΔV_{Clk}	300		800	mV
Clock Threshold Level	VTT	-1.3	0	1.3	V
Clock Input Resistance (**CK_P/N** to **VTT**)	R_{ck}	45	50	55	Ω
Reset, **RST**, Low Level (Free Running)	V_{RSTL}	-0.3	0	0.3	V
Reset, **RST**, High Level (Reset Applied)	V_{RSTH}	1.0	1.4~2.0	3.5	V
Strobe, **STR_P/N**, Single-Ended Swing	ΔV_{STR}	300		1000	mV
Common Mode Level of **STR_P/N**	V_{STR_CM}	0		1.5	V
Frequency Word (**Vi[0:31]**) Low Level	V_{DataL}	-0.3	0	0.3	V
Frequency Word (**Vi[0:31]**) High Level	V_{DataH}	1.0	1.4~2.0	3.5	V
COUT Voltage Amplitude (CML Terminated to a 50 Ω to Ground)	V_{Cout}	300	333	350	mV
Analog Output Swing	$\Delta V_{OUTP/N}$	400	600	800	mV_{PP}
Analog Output Common Mode Voltage	OUT_{CM}		-300		mV
Analog Output Swing Control[3]	AVS	-3.4	-3.0	-2.6	V
Input Clock Coupling	DC or AC Coupled				
Frequency Word Input Data Coupling	DC Coupled				
Analog Output Coupling[4]	DC Coupled				

Note 1: The ground for digital circuits (such as accumulator and ROM), the ground for DAC digital circuits and the ground for DAC analog circuits were separated on the chip. All these grounds were down bonded to the package substrate and not distinguishable by the users.

Note 2: VEE, VEED and VEEA were separated on the chip and bonded to different pins of the package. Bypass capacitances should be put as close to these pins as possible for decoupling purpose and then all these power supplies can share the same power plane on PCB.

Note 3: AVS pin can be left open as default and the corresponding output swing is 600 mV_{PP}.

Note 4: Although DC coupled is recommended, AC coupled can be used if necessary. With AC coupled, the common mode voltage of OUTP/N will shift from –300 mV to –600 mV.

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Theory of Operation

The DS856 core consists of a 32-bit accumulator, a sine wave look up table in the form of a ROM, and a 11-bit Digital to Analog Converter (DAC). The 32-bit accumulator is a phase accumulator, where the 32 frequency control bits are latched and added to the previous output of the accumulator at each clock cycle. The accumulator output stores the phase of the output waveform of the chip. Sine wave generation requires the phase from the accumulator be passed to a ROM to look up the appropriate amplitude for the waveform. To save on size the ROM only stores the first quadrant of sine wave data. To form the full pattern the two most significant bits of the phase are used with the first quadrant data to generate the full sine wave. The final 11-bit digital outputs of the ROM are passed to the DAC stage to synthesize the sine waveform. The DAC employs R-2R ladders and segmented architecture to improve linearity and reduce output glitches. The 22 current switches are all differential to produce a complementary pair of output signals.

All 11 data bits of the digital outputs of the ROM are re-latched with the same clock edge, providing a uniform setup time for the DAC stage. Then the 4 MSB bits are decoded into fifteen lines. The decoding employed reduces output glitches and improves dc linearity. The remaining 7 LSB bits (D0-D6) are passed on unchanged. The clock latches all 22 lines again. The latched data controls 7 R-2R and 15 segmented current switches respectively to produce the analog outputs. The four MSB bits control 15 identical current switches, while the seven LSB bits control 7 current switches connected through an R-2R ladder. The output signals should be connected with 50-Ω terminations to ground. Once terminated each output will produce a 600 mV full-scale voltage range. The differential outputs can be combined with a broadband balun to achieve 1.2V single ended output with the even-order harmonics suppressed to certain degree.

The state of the accumulator can be reset to zero when **RST** is set to voltage higher than 1.0V. This has the effect of setting the initial phase of the sine wave to zero. In normal operation **RST** should be set at 0V. When the accumulator overflows, a carry output bit is propagated to **COUT**. **COUT** has a 250-Ω back termination with 4 mA current sink. The **COUT** signal can be very useful to trigger or synchronize the DDS outputs with other chips, functions or equipments in the system. A pair of complementary clock inputs with 50-Ω terminations to **VTT** are provided. **VTT** acts as the logic threshold and can be set by the user. Once the 32 parallel frequency control data input bits **Vi[0:31]** are settled at the input pins, the high speed strobe pulse (**STRP**/**STRN**) will latch (at the negative transition edge) the 32 data input bits into accumulator and initiate new frequency signal at the DAC outputs. The phase of output signals will be continuous between the two output frequency signals before and after the strobe pulse. This high speed strobe feature allows DS856 to be controlled by micro-controller or DSP chips for real time chirping function.

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Input Data Timing

The frequency word data inputs **Vi[0:31]** are latched into the registers of the DDS chip with timing generated by both the main clock and the STROBE (**STR_P/N** pins) input. The **STR_P/N** signals can be either differential or single ended (with **STRN** set at the center DC voltage of **STRP**). The accumulator of **DS856** uses an 8-stage pipeline architecture. As shown in the following figure, at the falling edge of **STRP**, a pulse CKP1 with width of one main clock cycle will be generated in the chip to latch all 32 bit data inputs to the master latches of input registers. After the 32 bit data latched into the master latches (i.e. at the falling edge of CKP1), the frequency word data bus are free for the new data to be updated. It takes 8 clock cycles to complete the loading of all 32-bit data into the slave latches of the register due to the 8-pipe pipeline architecture.. Therefore, the minimal spacing between successive falling edges of STROBE is 8 clock cycles which sets the highest frequency word update rate.

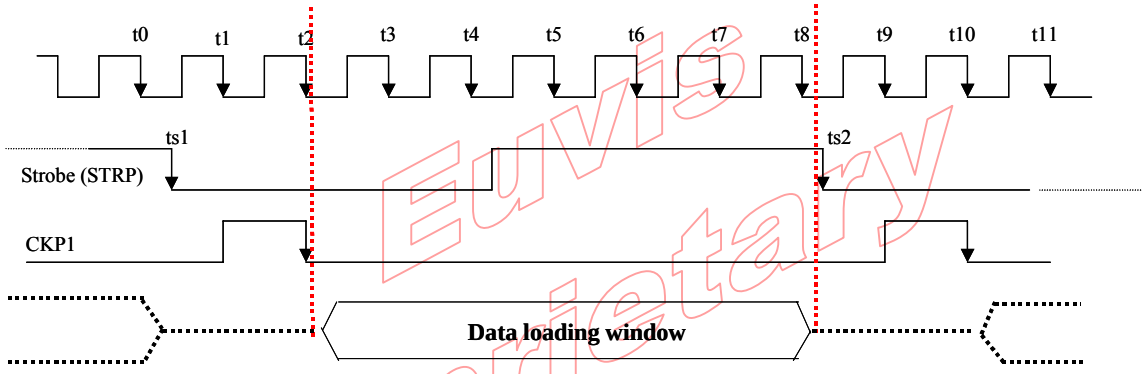

Fig.1 Timing relationship of **STRP** and main clock. CKP1 pulse with one main clock cycle width was generated at the first falling edge of main clock after the falling edge of **STRP**. The falling edge of CKP1 was used to latch all the 32-bit data inputs into the master latches of input registers. The minimal spacing between successive falling edges of **STRP** is 8 clock cycles. The data loading window is more than 6 clock cycles.

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RESET TIMING

The RESET input **RST** is an asynchronous input for the registers of the accumulator. Upon application of the RESET signal all the registers of the accumulator are set to LOW. To ensure the reset logic functions the RESET signal must be applied for at least the hold time, t_{RH}, of 500 psec. Ideally when RESET is released, that is set LOW, the following falling clock edge will trigger accumulation of phase in the accumulator unit. However if the falling clock edge follows the falling RESET edge to closely the registers of the accumulator will remain LOW for one more clock cycle. To ensure that a falling clock edge triggers the accumulator RESET must be low at least for the setup time, t_{RS}, of 500 psec. The latency of RESET is 5 falling clock edges.

TIMING SUMMURY

All setup and hold times in this data sheet are to be considered maximum values the DS856 may require. Real performance may reduce these timing limitations. Below is a table summary of the time characteristics discussed in the document.

Parameter	Symbol	Min.	Typ.	Max.	Unit
STROBE (**STR_P/N**) setup time	t_{SS}			250	psec
STROBE (**STR_P/N**) hold time	t_{SH}			500	psec
Frequency Data (**Vi[0:31]**) setup time	t_{DS}			500	psec
Frequency Data (**Vi[0:31]**) hold time	t_{DH}			500	psec
RESET (**RST**) setup time	t_{RS}			500	psec
RESET (**RST**) hold time	t_{RH}			500	psec
STROBE/Data latency to RF output[1]		13			falling clock edges
RESET latency to RF output[1]		5			falling clock edges

Note 1: Assumes setup and hold times are not violated.

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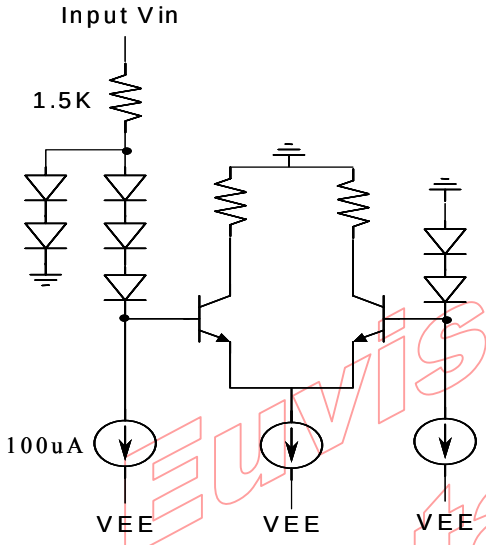
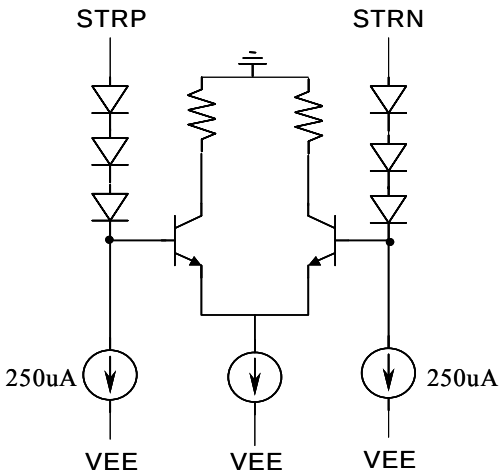
DATA INPUT INTERFACE

A simplified schematic of single ended frequency word **Vi[0:31]** and reset **RST** input circuit is shown below. As Vin is higher than 1.4V, it will draw current of [Vin–1.4 V]/1500 mA due to the two clamping diode to ground. If Vin is lower than 1.4V, it will draw no more than 100 uA. Users need to make sure the chip used to drive this DDS has enough driving capability and pay attention on its output impedance which wouldn't cause too much voltage drop in the high state.



STROBE STR_P/N INPUT INTERFACE

A simplified schematic of differential strobe (**STR_P/N**) input circuit is shown below. Users need to make sure the driver to provide strobe signals has 250 uA driving capability. For single ended implementation, STRBN should be set at the middle level of STRP swing.



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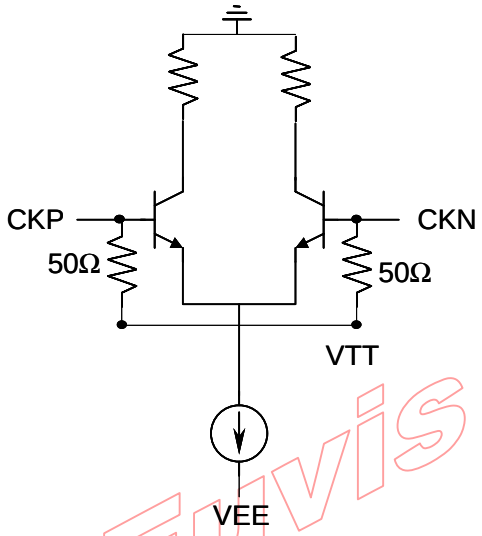
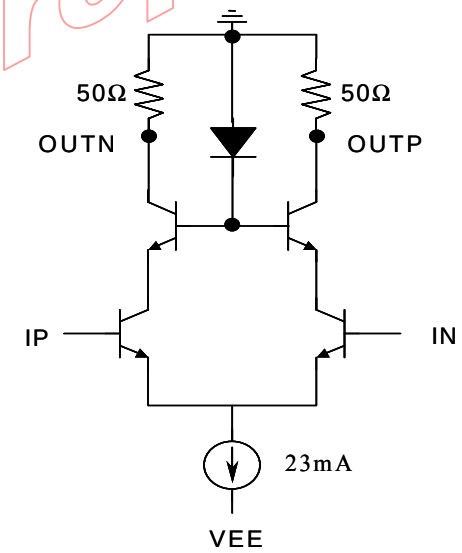
Clock Input Interface

A simplified schematic of clock input circuit is shown below. It has input impedance of 50Ω terminated to VTT- which can be used to set clock input DC level. VTT should be grounded when clock signals are AC coupled. It's recommended to have both CKN and VTT grounded and CKP AC-coupled to the input.



Analog Output Interface

A simplified schematic of analog output circuit is shown below. Look into the **OUT_P/N**, each terminal has internal 50 ohm terminated to ground. The **OUT_P/N** should go through 50 ohm transmission line and either DC or AC terminated to an external 50 ohm load to ground.



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ABSOLUTE MAXIMUM RATINGS – WITH NEGATIVE SUPPLY VOLTAGE

Parameter	Symbol	Typical	Unit
Ambient Temperature	T_A	–40~85	°C
Storage Temperature	T_{STR}	–65~150	°C
Data Input	V_{DMAX}	–3 ~ 6	V
CLK, CLKN	V_{CKMAX}	–3 ~ 1	V
Power Supply Voltage	V_{EE}	-8	V

TERMINAL DESCRIPTION

Name	Function	I/O	Signal
VCC	Ground	I	DC
VEE	Power Supply for Digital Circuits	I	DC
VEEA	Power Supply for Analog Circuits of DAC	I	DC
VEED	Power Supply for Digital Circuits of DAC	I	DC
CKP/CKN	Clock Inputs	I	RF
VTT	Complementary Clock Threshold	I	DC
RST	Accumulator Reset	I	DC
STRP/STRN	Strobe Vi0~Vi31 Inputs to Change Output Frequency	I	DC
Vi[0:31]	Frequency Control Input Bits (Selects Output Frequency)	I	DC
COUT	Carry Output Bit From Accumulator	O	RF
OUTP/OUTN	DAC Complementary Analog Outputs	O	RF
AVS	Analog Output Swing Control	I	DC
VCSU/VCSM/ TP1/TP2/TPR	Test Point for Internal Checking (No Connections for Users)	O	DC

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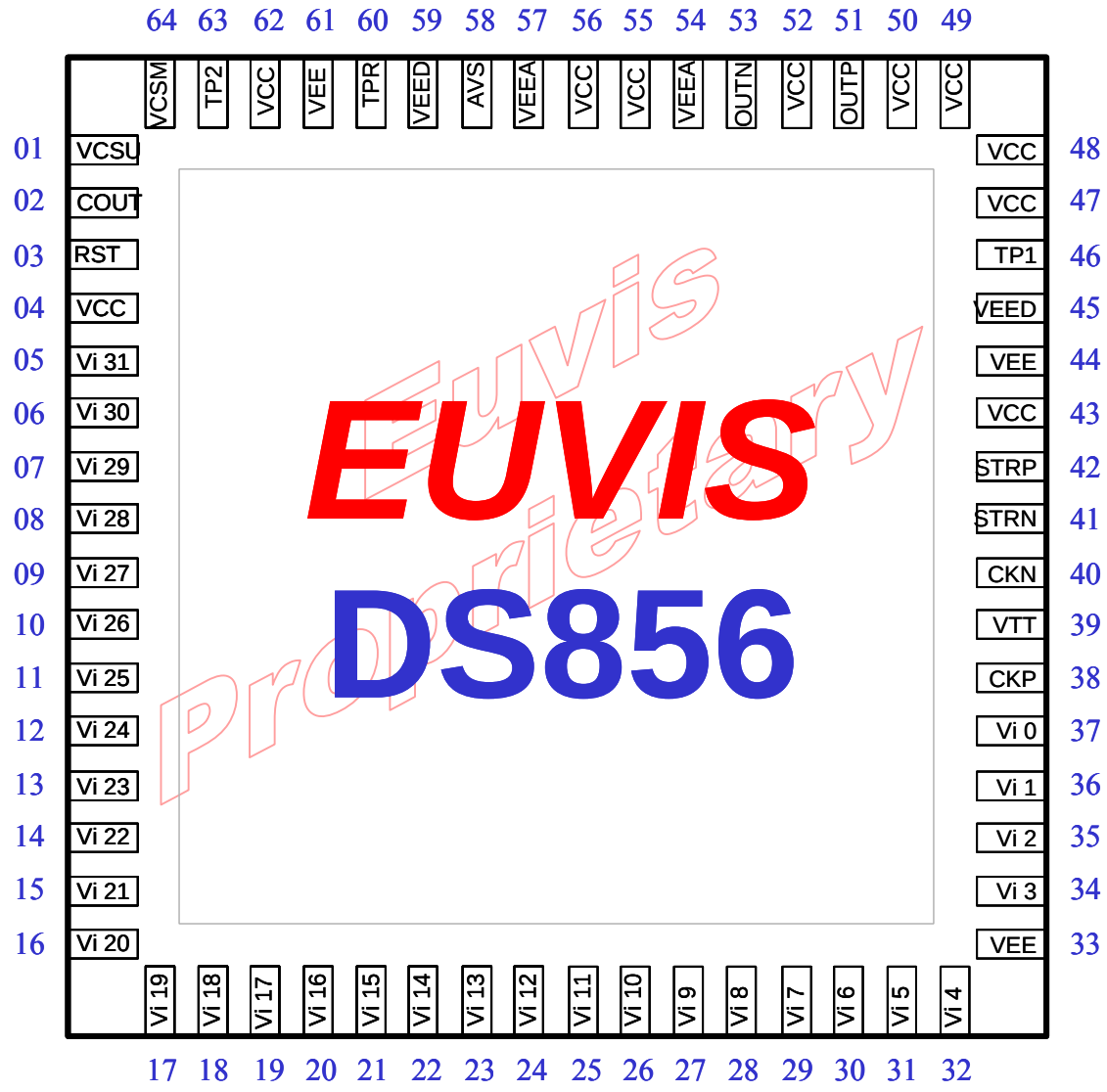
BIT WEIGHT OF FREQUENCY WORD INPUTS

BIT POSISTION	FREQUENCY PER BIT POSISTION
Vi0 (LSB)	F(CLK)/2^32
Vi1	F(CLK)/2^31
Vi2	F(CLK)/2^30
Vi3	F(CLK)/2^29
Vi4	F(CLK)/2^28
Vi5	F(CLK)/2^27
Vi6	F(CLK)/2^26
Vi7	F(CLK)/2^25
Vi8	F(CLK)/2^24
Vi9	F(CLK)/2^23
Vi10	F(CLK)/2^22
Vi11	F(CLK)/2^21
Vi12	F(CLK)/2^20
Vi13	F(CLK)/2^19
Vi14	F(CLK)/2^18
Vi15	F(CLK)/2^17
Vi16	F(CLK)/2^16
Vi17	F(CLK)/2^15
Vi18	F(CLK)/2^14
Vi19	F(CLK)/2^13
Vi20	F(CLK)/2^12
Vi21	F(CLK)/2^11
Vi22	F(CLK)/2^10
Vi23	F(CLK)/2^9
Vi24	F(CLK)/2^8
Vi25	F(CLK)/2^7
Vi26	F(CLK)/2^6
Vi27	F(CLK)/2^5
Vi28	F(CLK)/2^4
Vi29	F(CLK)/2^3
Vi30	F(CLK)/2^2
Vi31(MSB)	F(CLK)/2

PIN ASSIGNMENTS

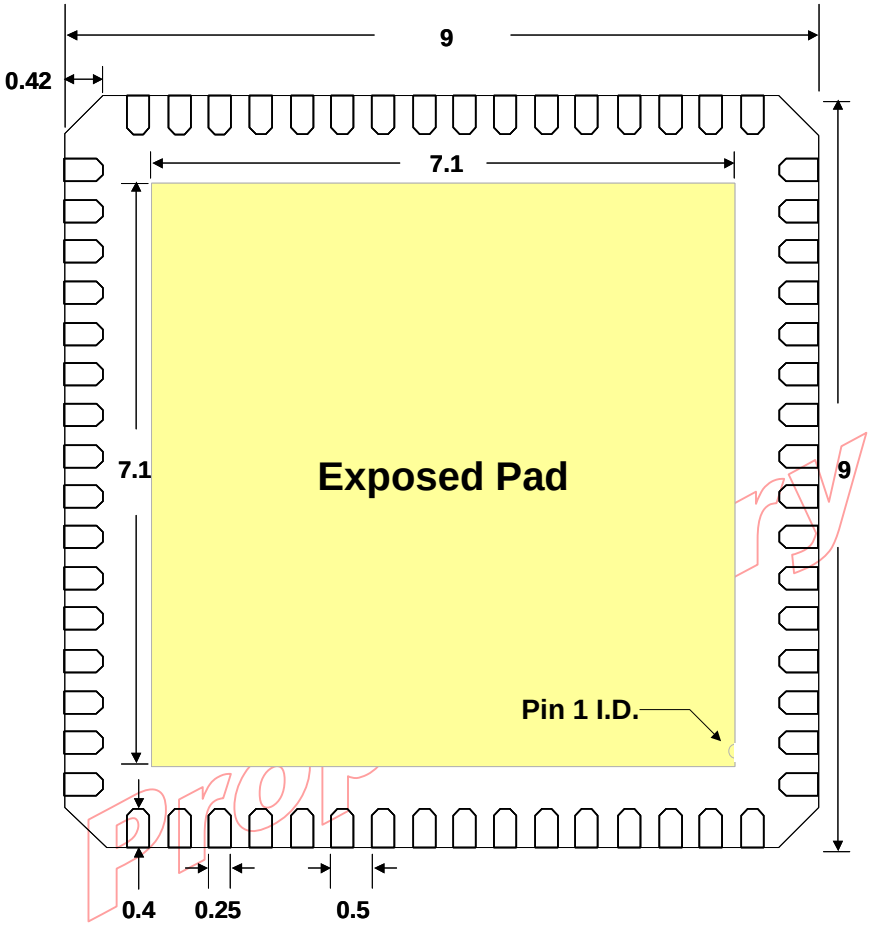
- Package Format: 64-pin QFN
- Package Size: 9 mm x 9 mm
- Pin Pitch: 0.5 mm

Top View

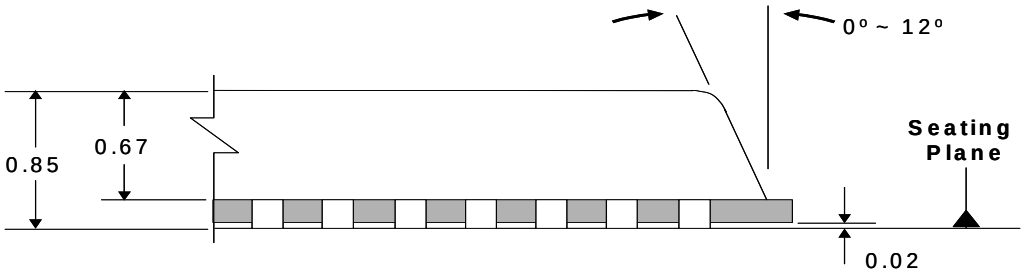


QFN9x9 Mechanical Dimensions

Bottom View

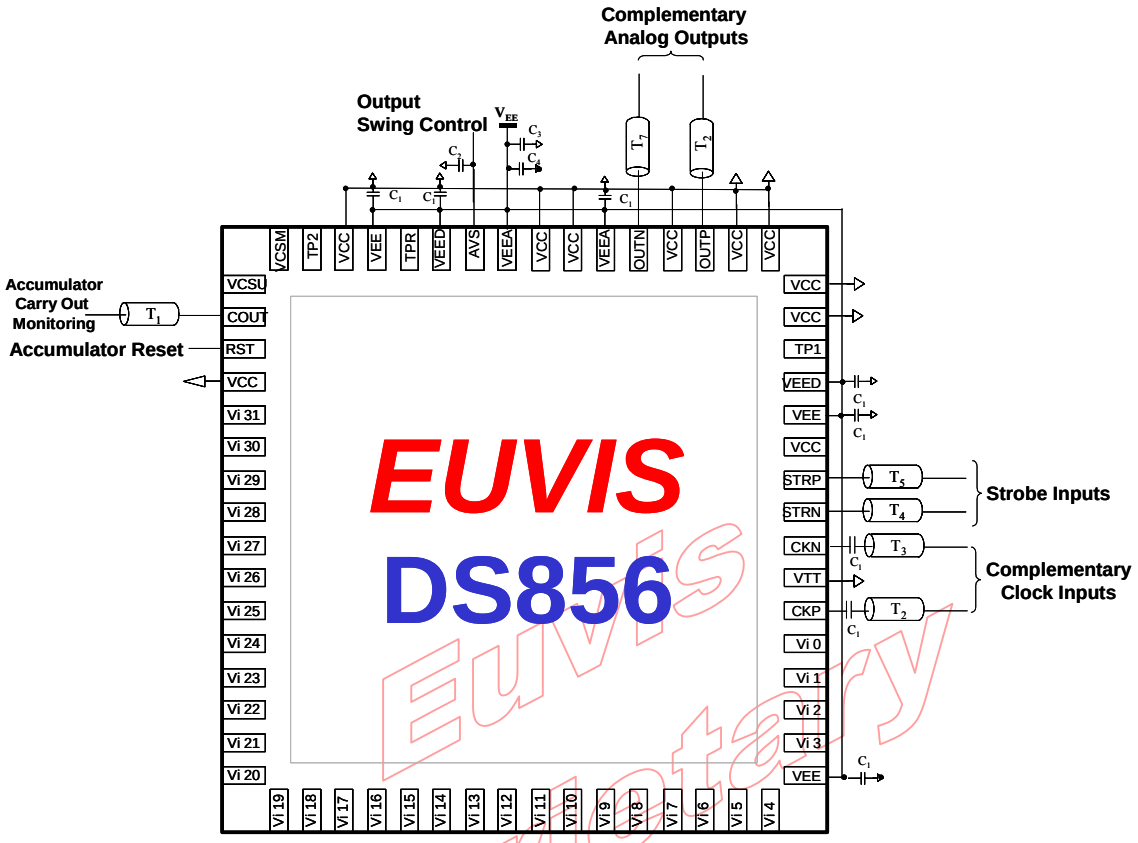


Side View



Unit: mm

TYPICAL CONNECTION



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NOTES:

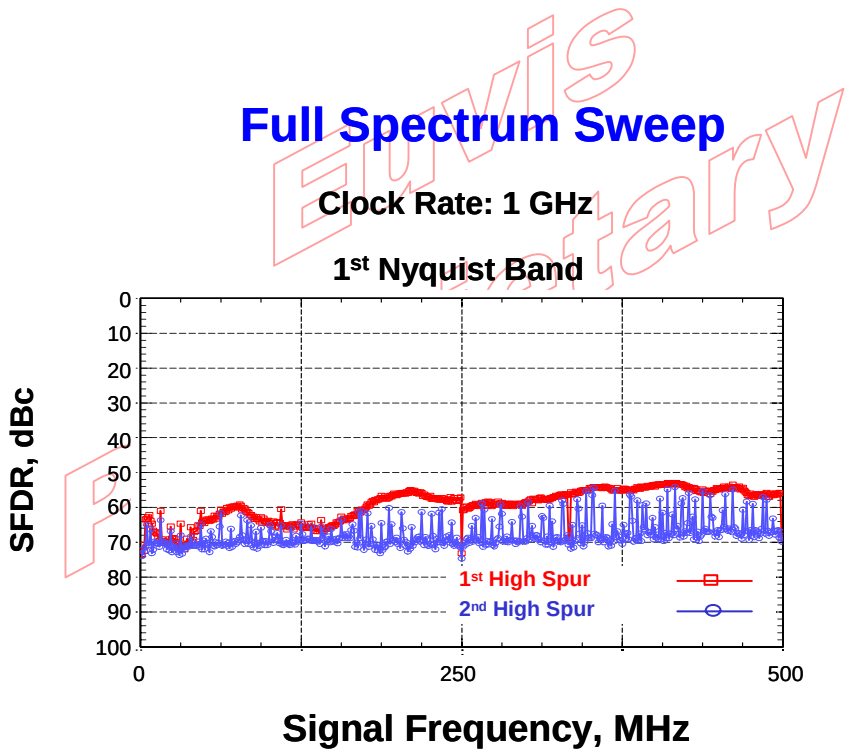
V_{CC}'s and package bottom exposed pad are connected to ground
V_{EE}'s, V_{EED}'s and V_{EEA}'s are connected to power supply –5.0 V
T_1~T_7: 50-Ω transmission lines
C_1~C_3: 100-nF surface mount capacitors
C_4: a 10-uF capacitor on the power trace

MEASUREMENT RESULTS

Worst SFDR across Nyquist Band

The RF performance was characterized by ***Euvis*** DDS evaluation board with USB interface and PC Window Driver control. Please refer to the DDS Ev_Board Data Sheet for the details of the set up.

The following figures show typical SFDR versus signal frequency at clock rates of 1.0 GHz, 2.0 GHz and 3.0 GHz respectively. The SFDR was derived based on the difference of the single-ended signal output and the highest (or the 2nd highest) spur between DC and 0.5 * f_{clk} (i.e the whole 1st Nyquist band) without filtering. The highest spurs (data in red) are 2nd harmonics related spurs for each output frequency.



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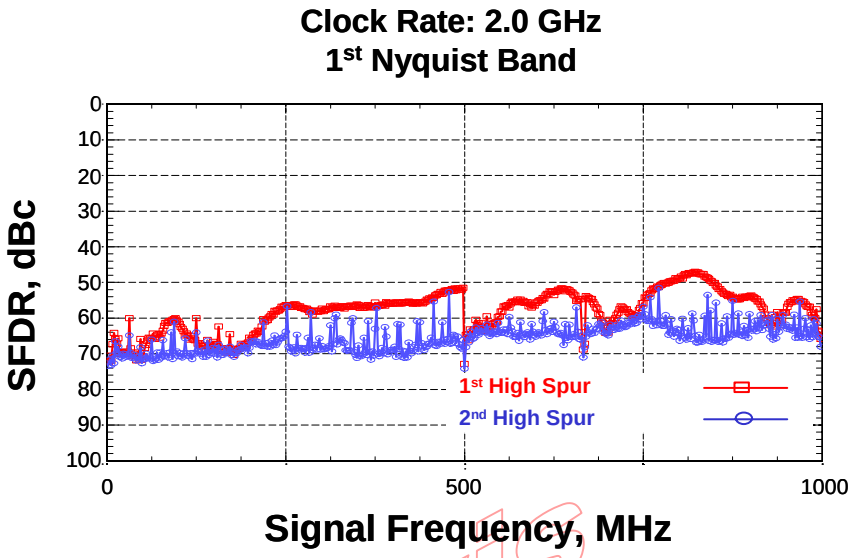

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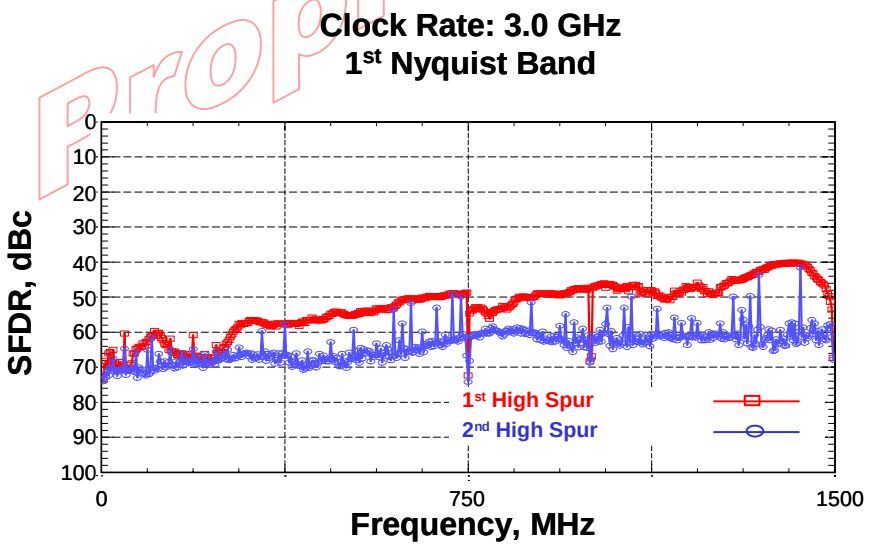
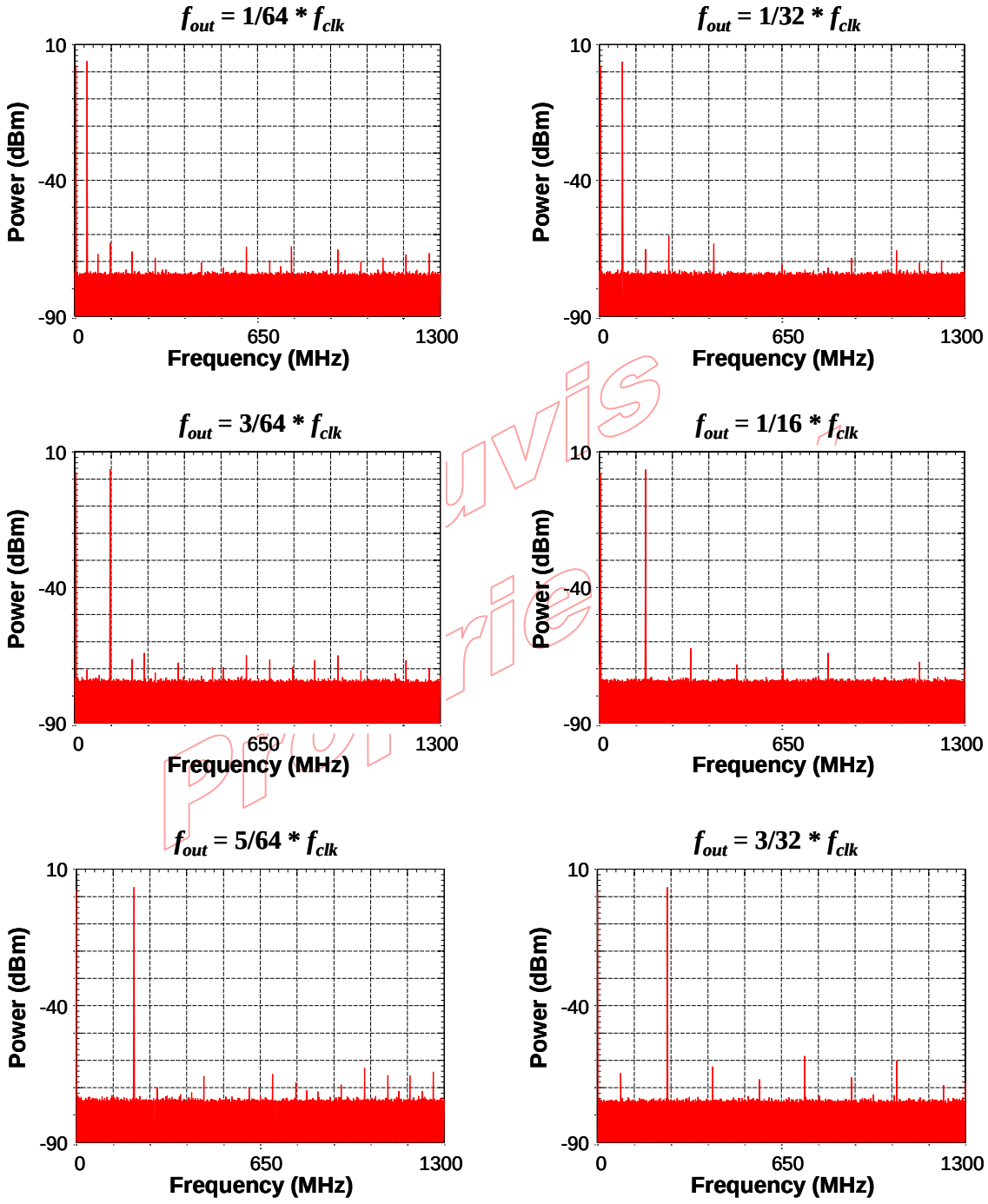
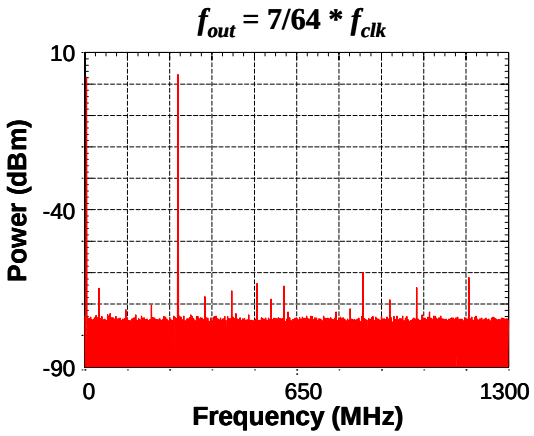
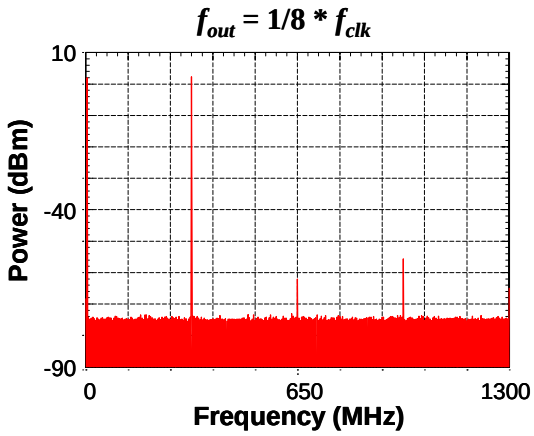


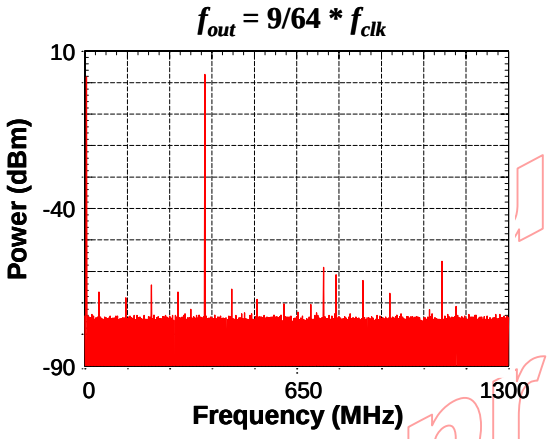
Broadband (Nyquist Band) Spectrum with f_{clk} = 2.6 GHz

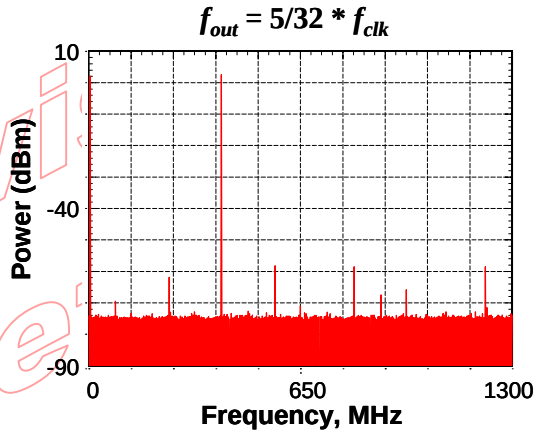
The following broadband spectra were measured at a clock rates of 2.6 GHz with the increment of f_{out} in step of 1/64*f_{clk}. These spectra should cover the harmonics-related worst spurs across the Nyquist band.

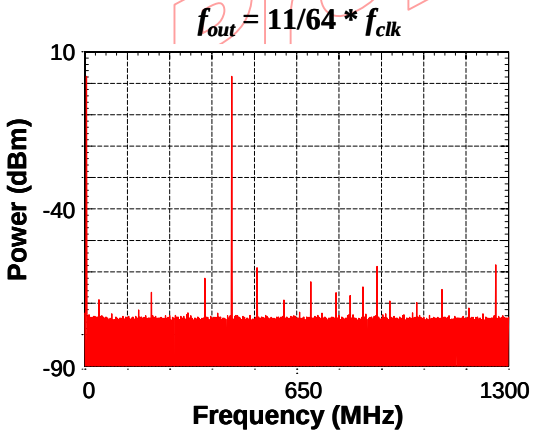


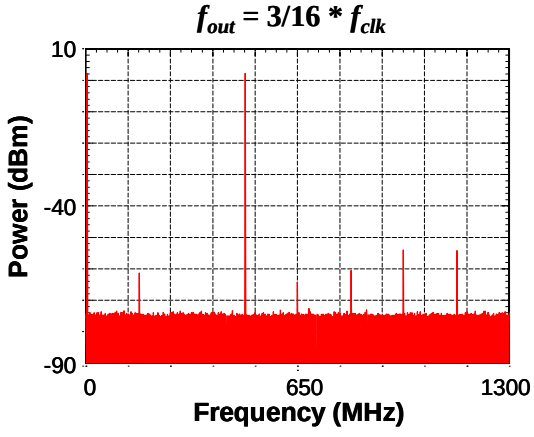












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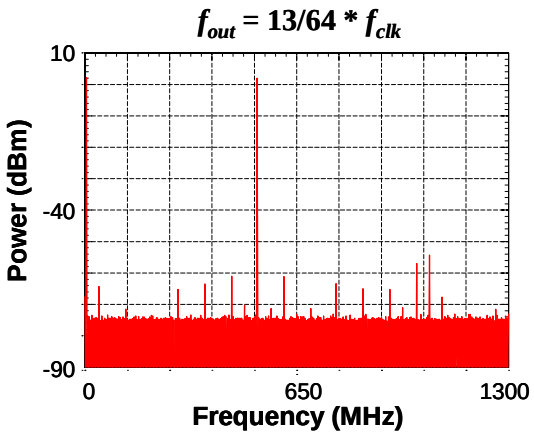

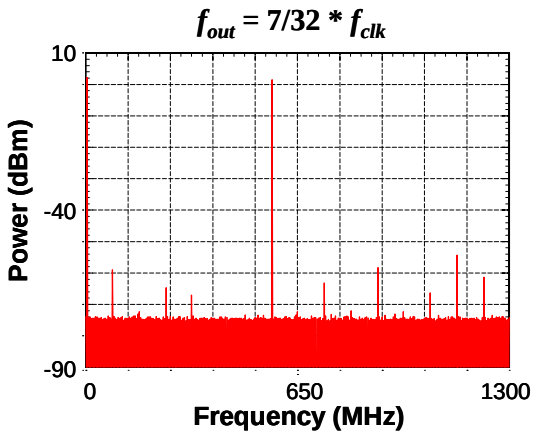

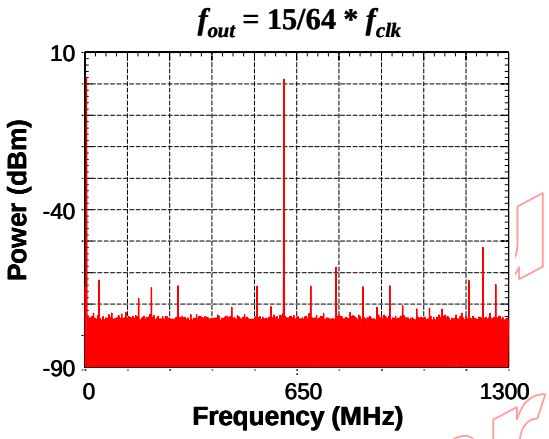

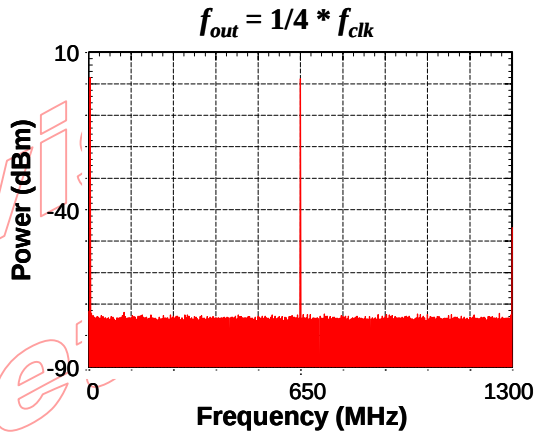

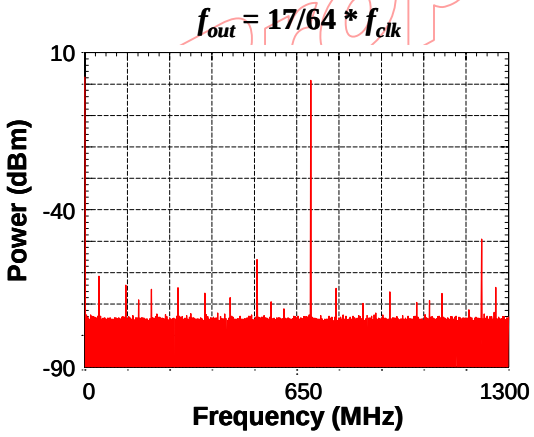

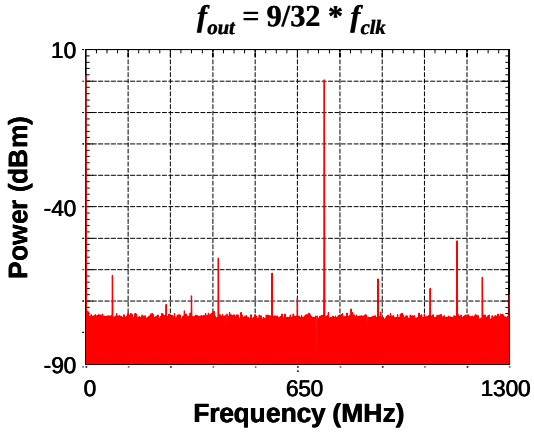

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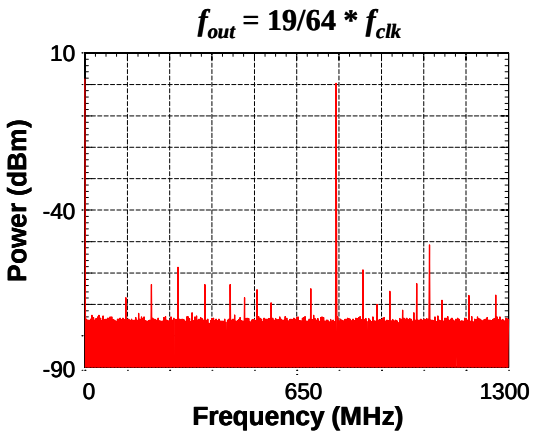
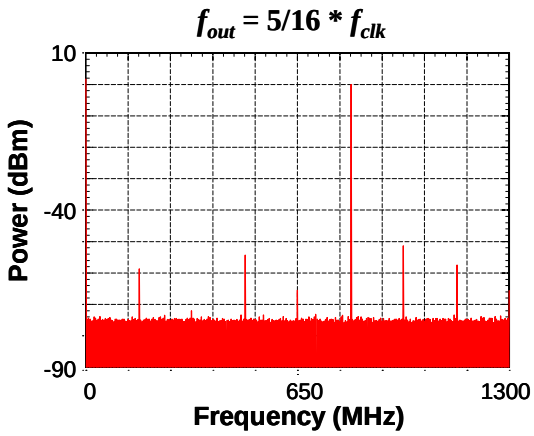
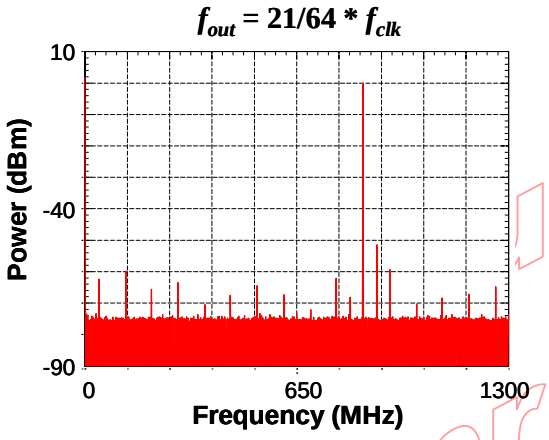
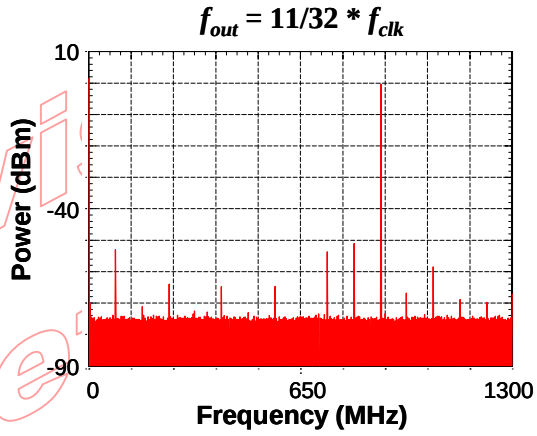
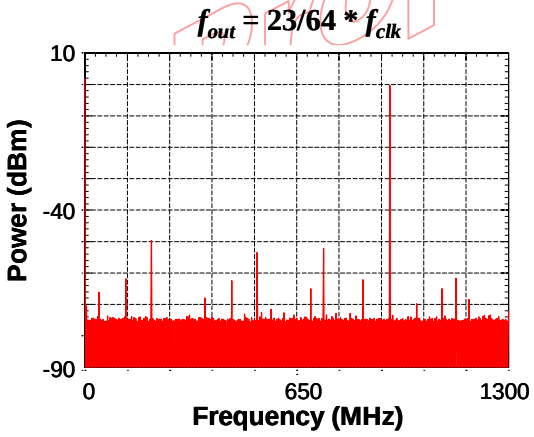
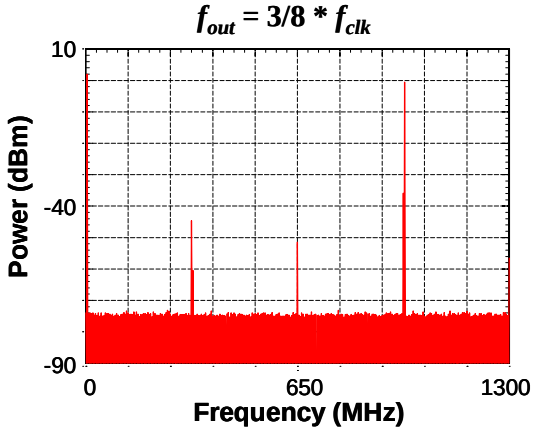






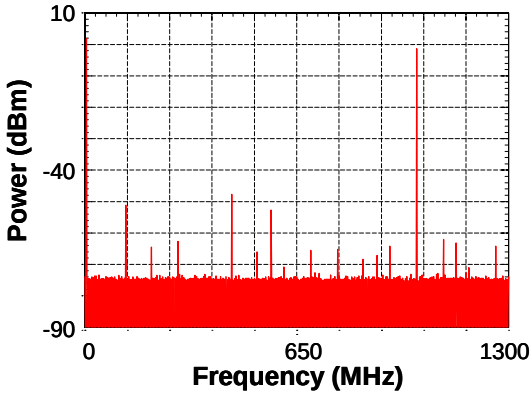




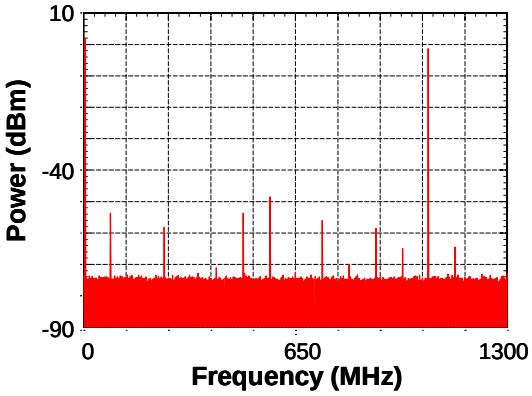


Euvis Proprietary

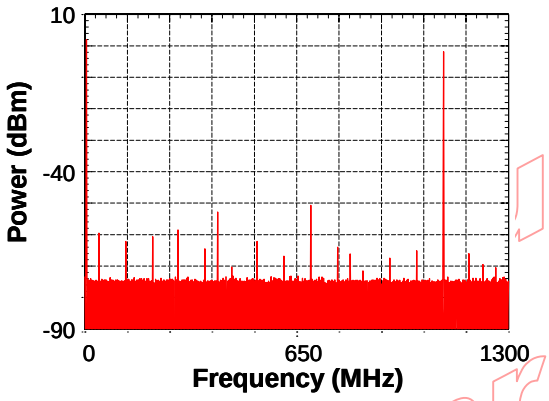
f_{out} = 25/64 * f_{clk}



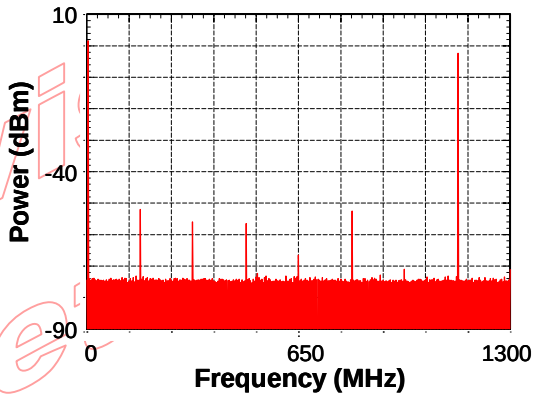
f_{out} = 13/32 * f_{clk}



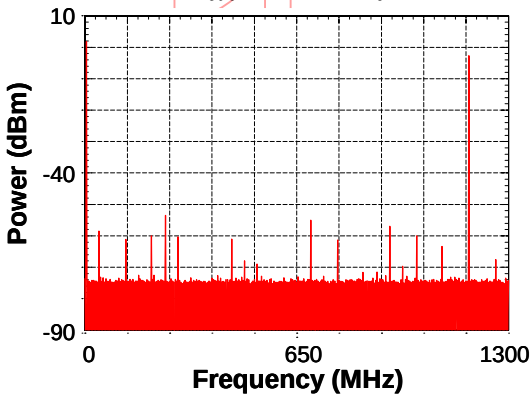
f_{out} = 27/64 * f_{clk}



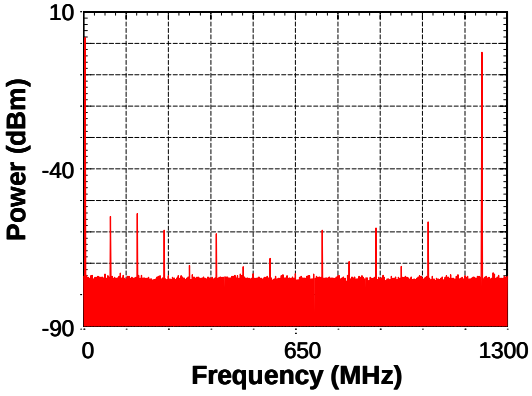
f_{out} = 7/16 * f_{clk}



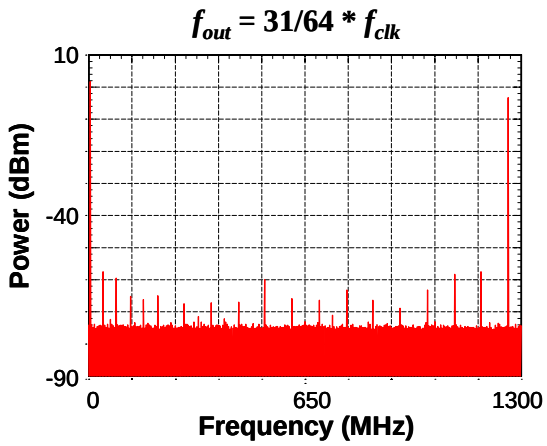
f_{out} = 29/64 * f_{clk}



f_{out} = 15/32 * f_{clk}



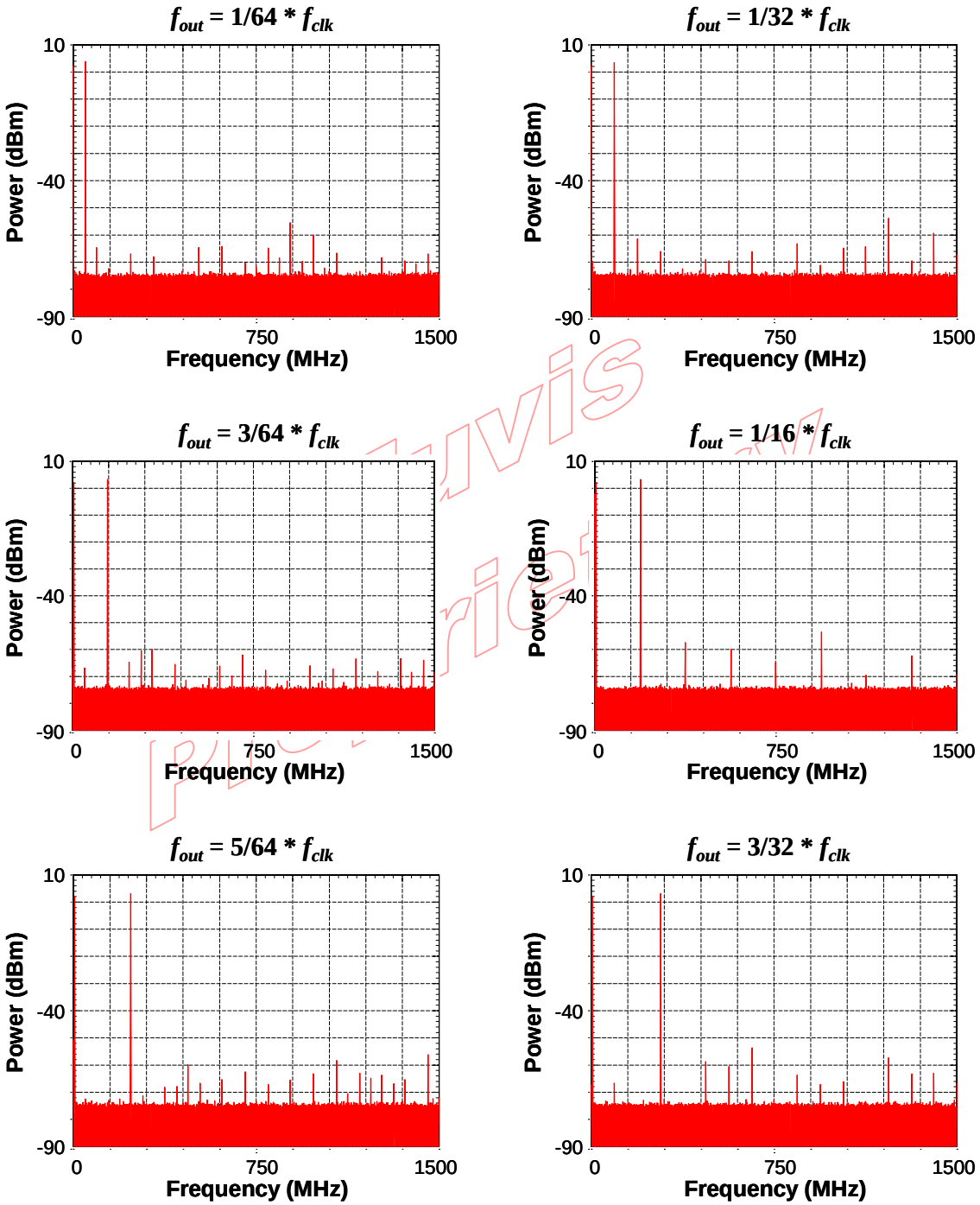
Euvis Proprietary

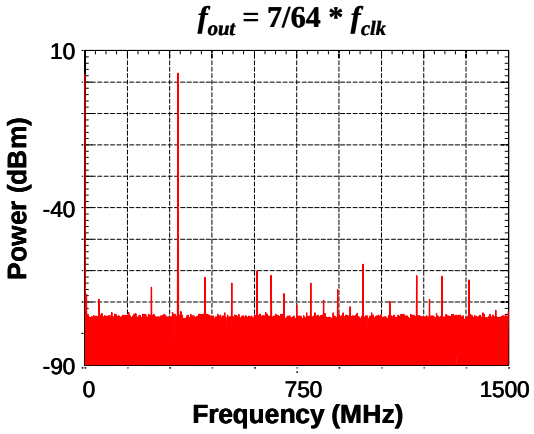


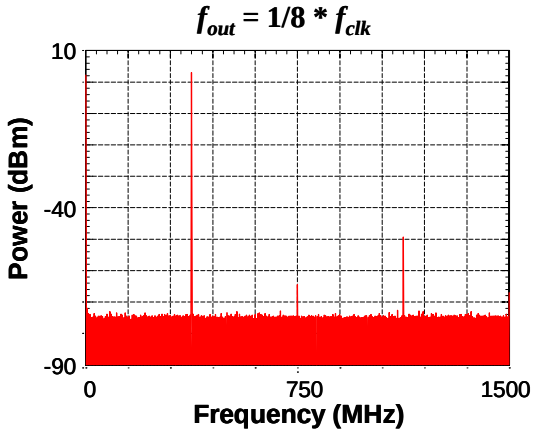
Euvis Proprietary

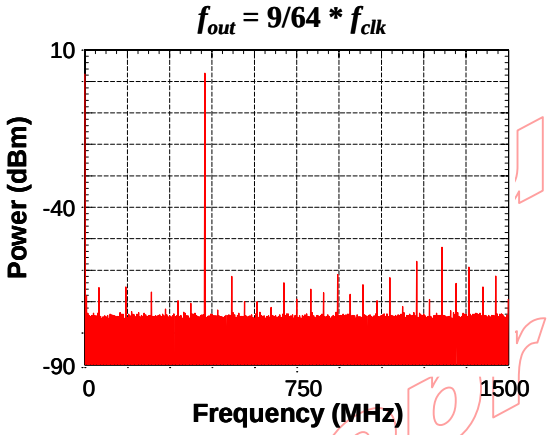
Broadband (Nyquist Band) Spectrum with f_{clk} = 3.0 GHz

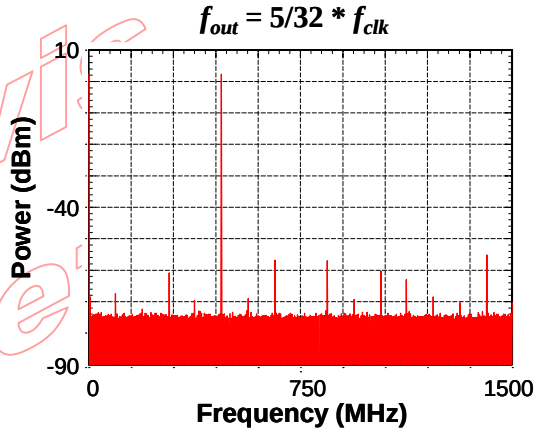
The following broadband spectra were measured at a clock rates of 3.0 GHz with the increment of f_{out} in step of 1/64*f_{clk}. These spectra should cover the harmonics-related worst spurs across the Nyquist band.

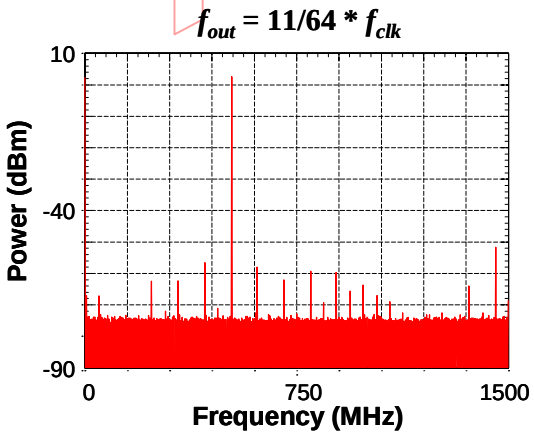


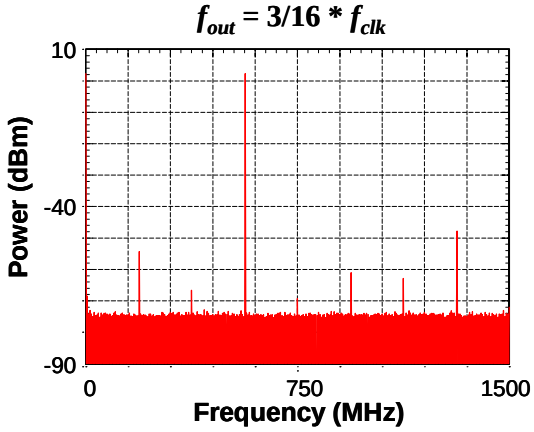












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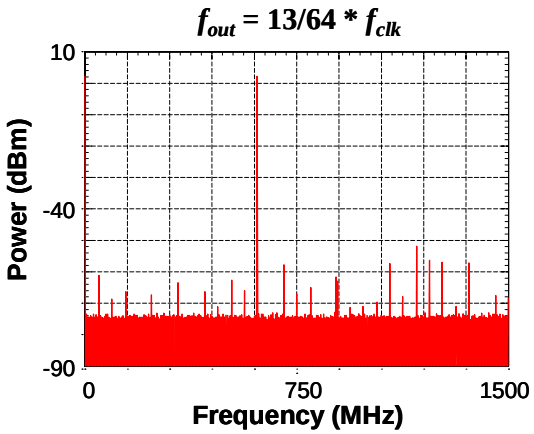
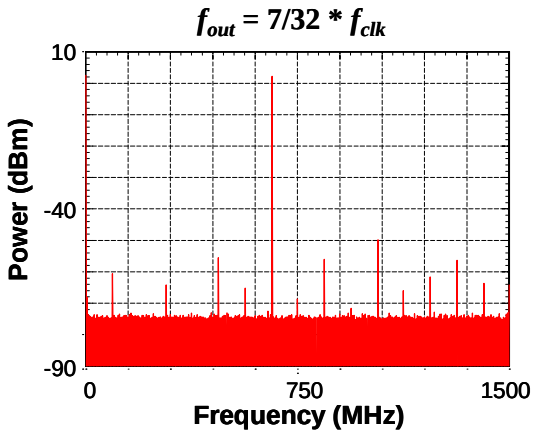
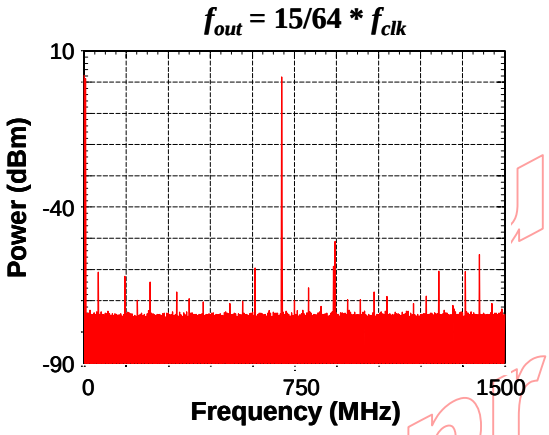
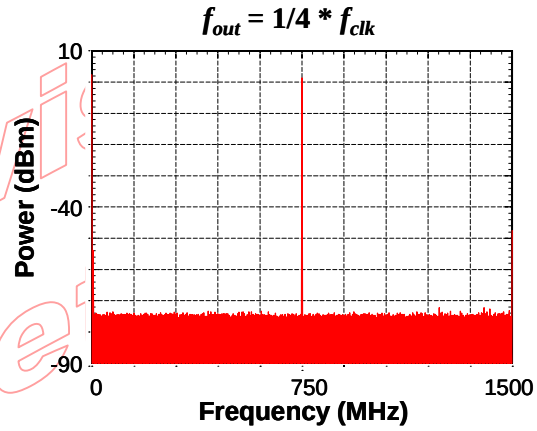
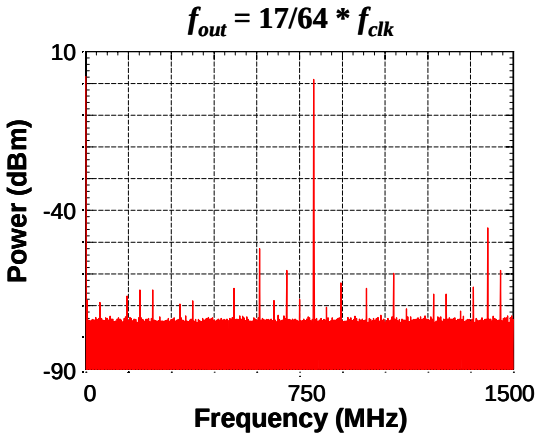
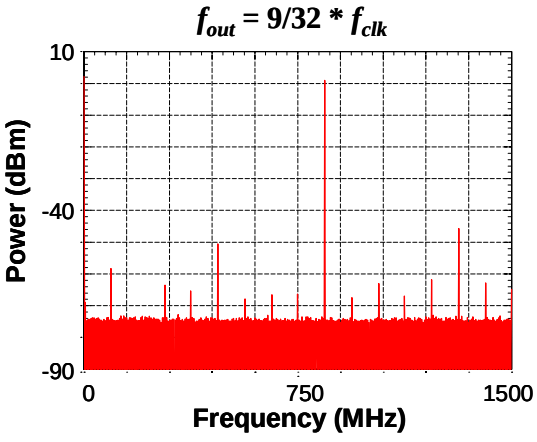




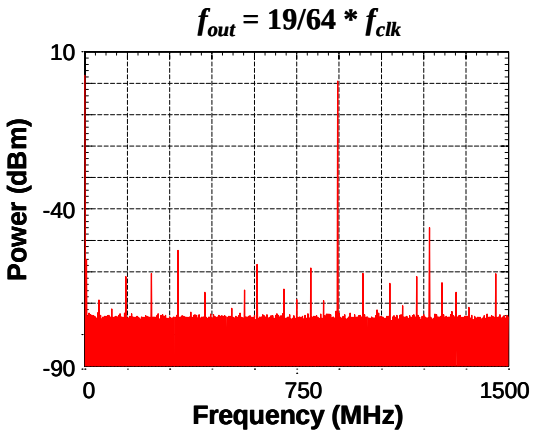


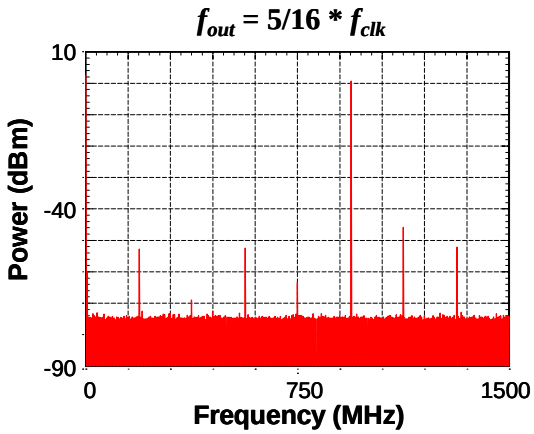


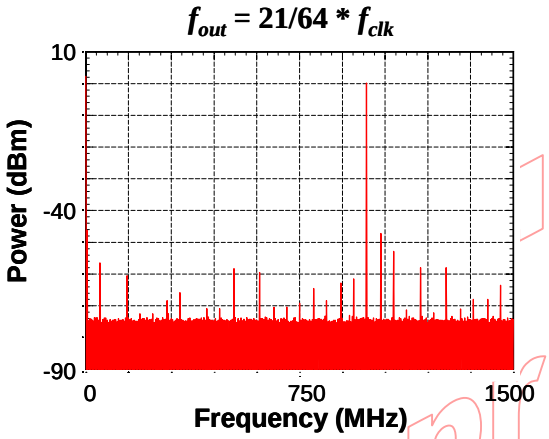


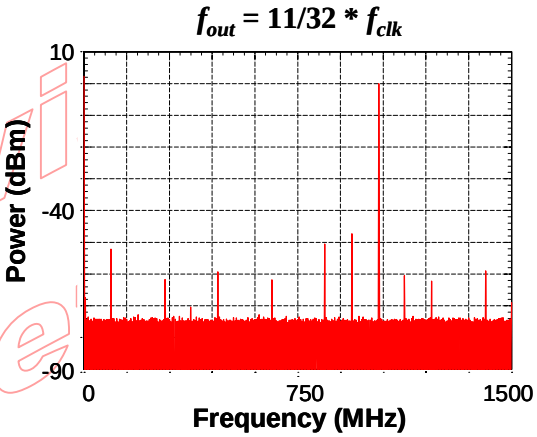


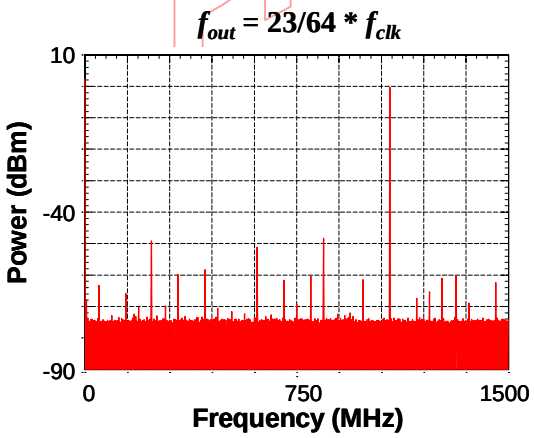
Euvis Proprietary

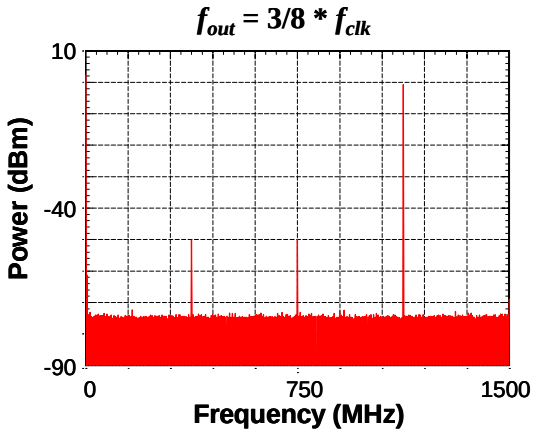




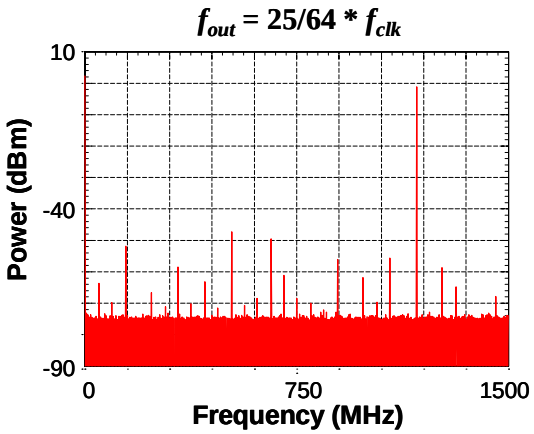


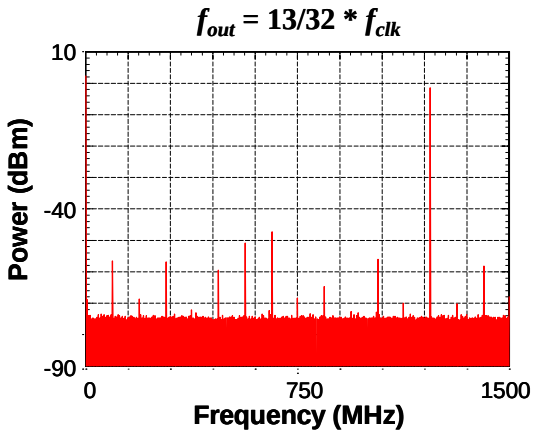


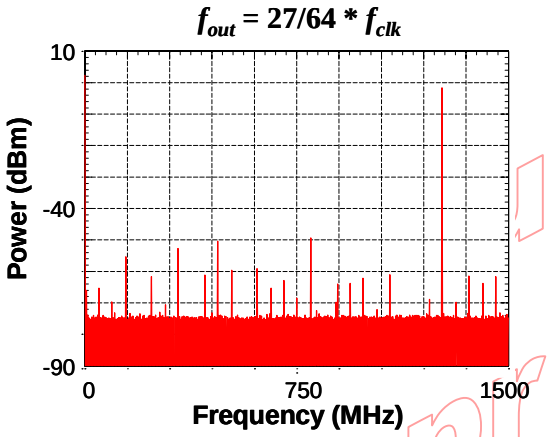


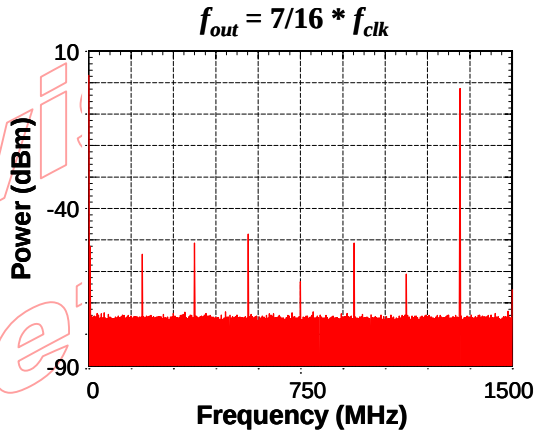


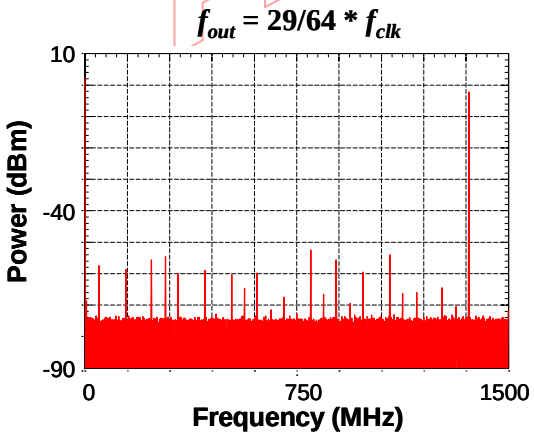
Euvis Proprietary

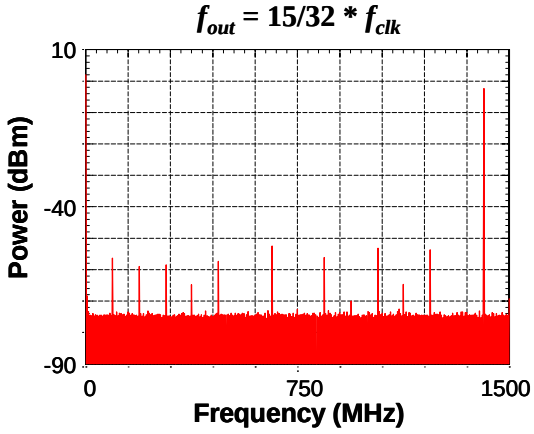




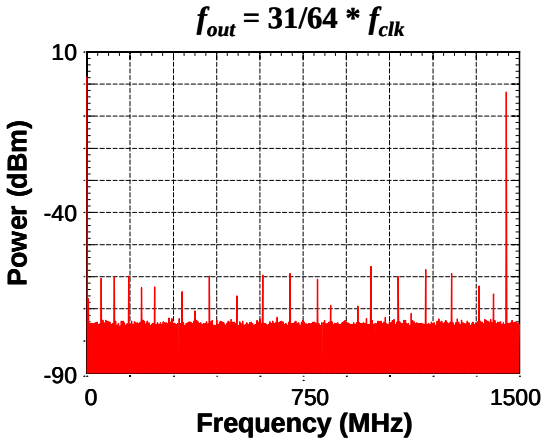








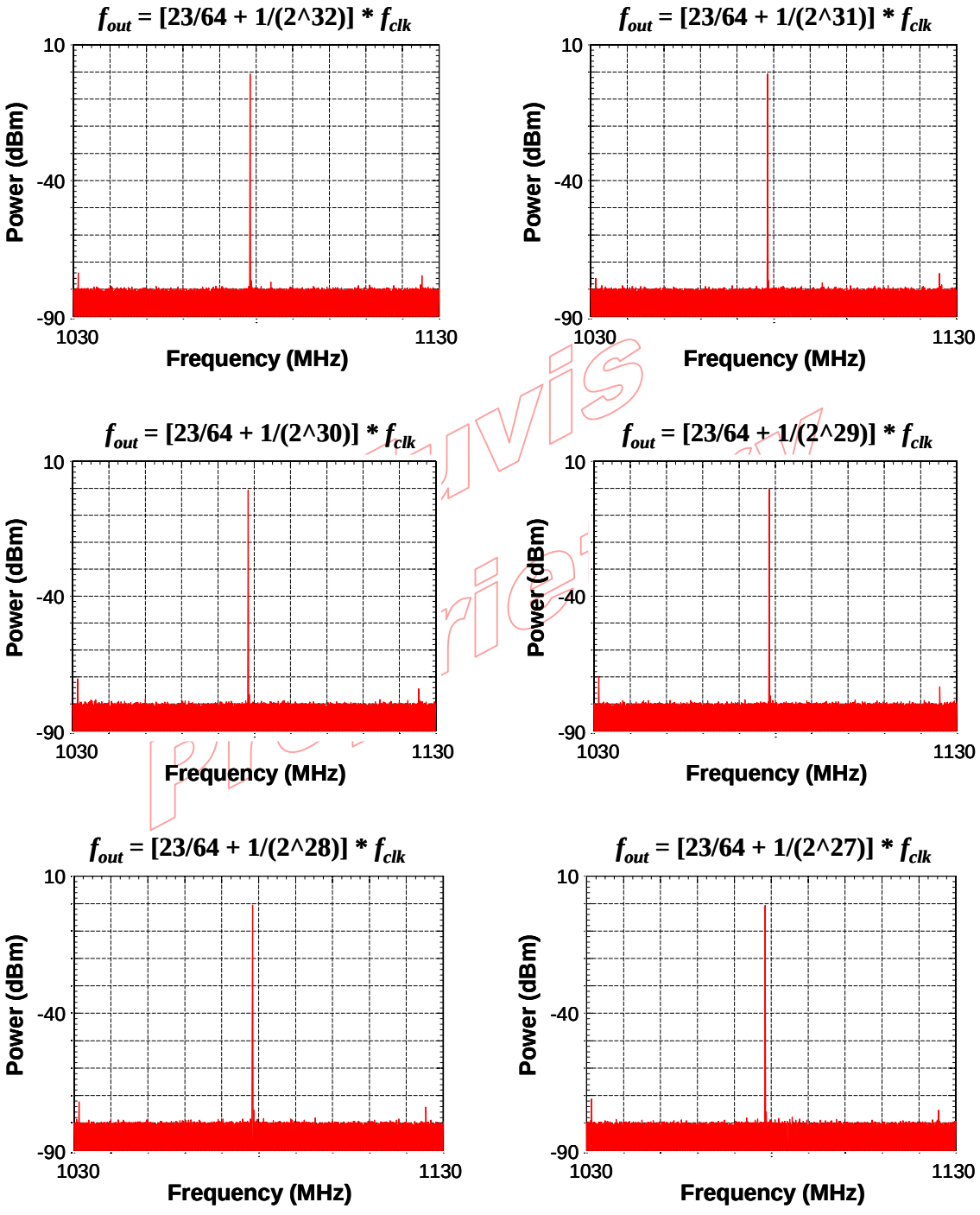
Euvis Proprietary

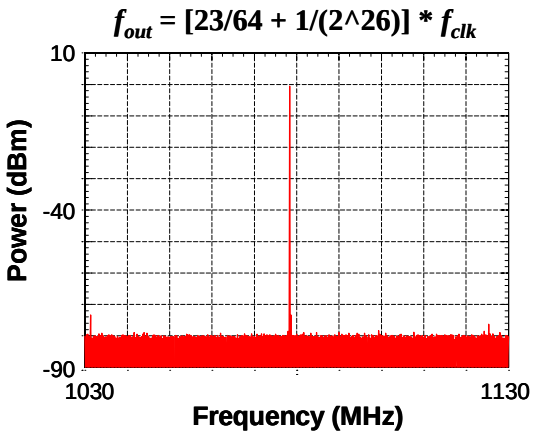


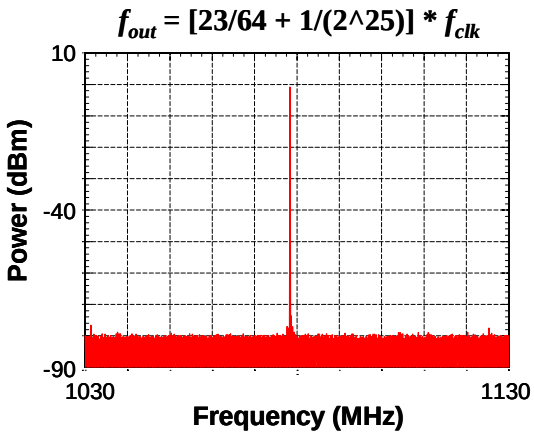
Euvis Proprietary

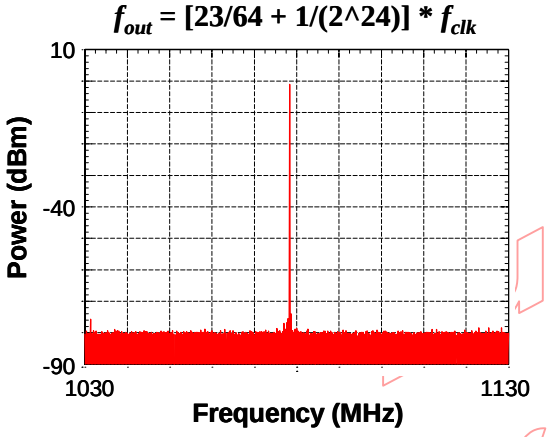
Narrow Band (100MHz Span) Spectrum with f_{clk} = 3.0 GHz

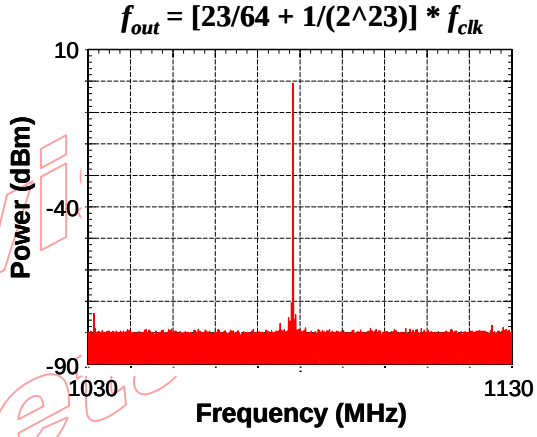
The following narrow band 100 MHz bandwidth spectra were measured at a clock rate of 3.0 GHz. The main frequency f_{out} is set at 17/64*f_{clk} with various single LSB turned on in each plot.

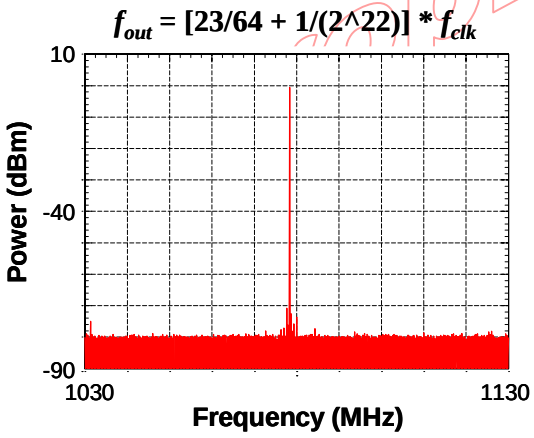


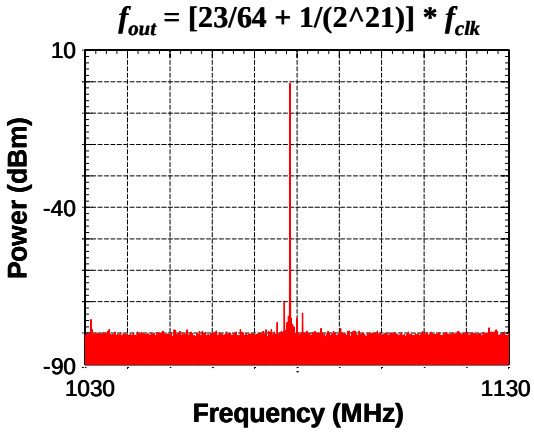

f_{out} = [23/64 + 1/(2^26)] * f_{clk}
10
-40
-90
Power (dBm)
1030
1130
Frequency (MHz)


f_{out} = [23/64 + 1/(2^25)] * f_{clk}
10
-40
-90
Power (dBm)
1030
1130
Frequency (MHz)

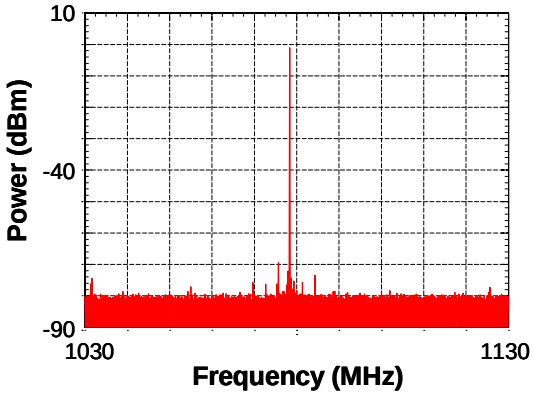

f_{out} = [23/64 + 1/(2^24)] * f_{clk}
10
-40
-90
Power (dBm)
1030
1130
Frequency (MHz)


f_{out} = [23/64 + 1/(2^23)] * f_{clk}
10
-40
-90
Power (dBm)
1030
1130
Frequency (MHz)

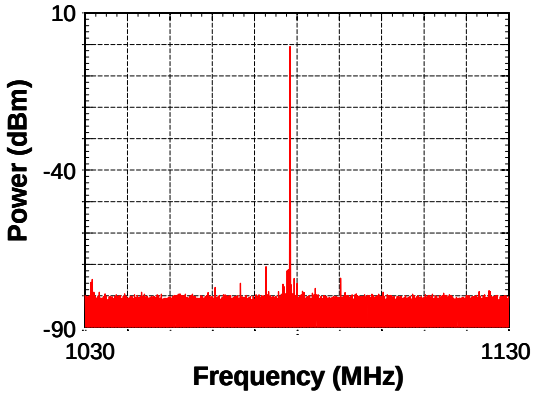

f_{out} = [23/64 + 1/(2^22)] * f_{clk}
10
-40
-90
Power (dBm)
1030
1130
Frequency (MHz)


f_{out} = [23/64 + 1/(2^21)] * f_{clk}
10
-40
-90
Power (dBm)
1030
1130
Frequency (MHz)

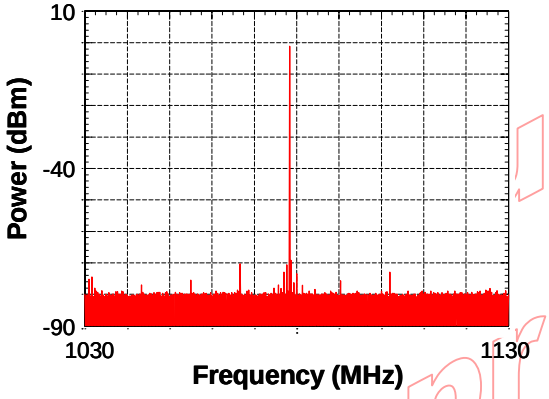
f_{out} = [23/64 + 1/(2^20)] * f_{clk}



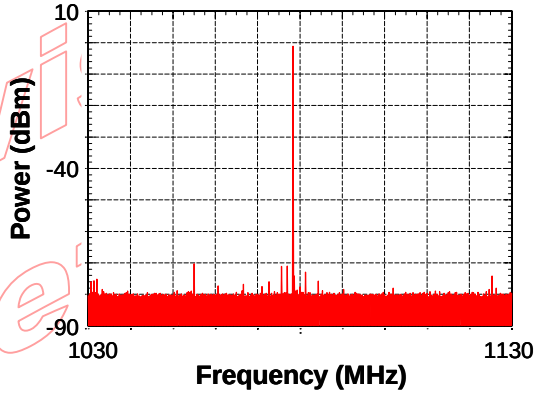
f_{out} = [23/64 + 1/(2^19)] * f_{clk}



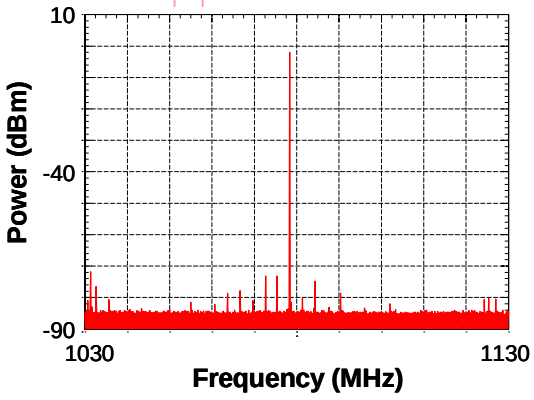
f_{out} = [23/64 + 1/(2^18)] * f_{clk}



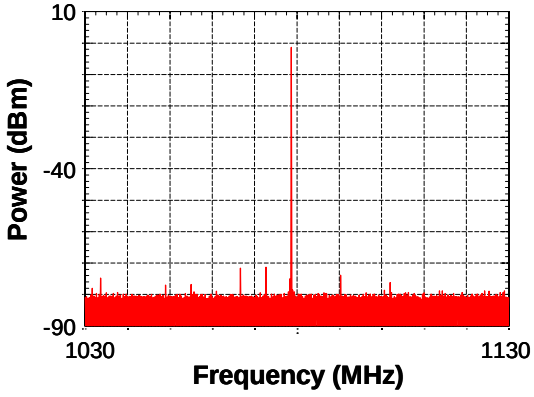
f_{out} = [23/64 + 1/(2^17)] * f_{clk}



f_{out} = [23/64 + 1/(2^16)] * f_{clk}



f_{out} = [23/64 + 1/(2^15)] * f_{clk}



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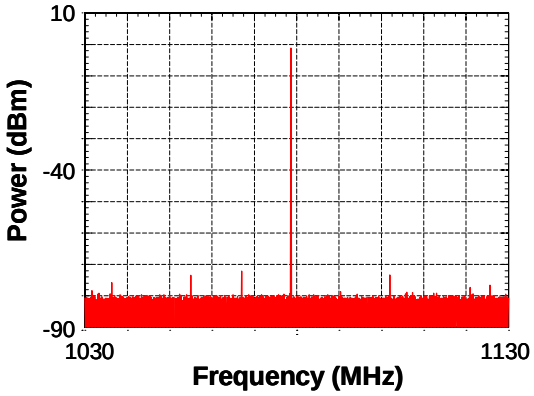
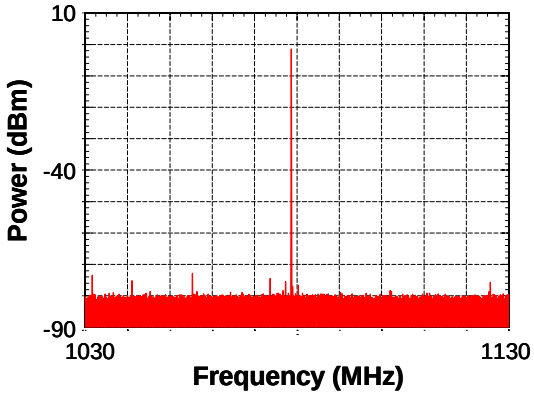
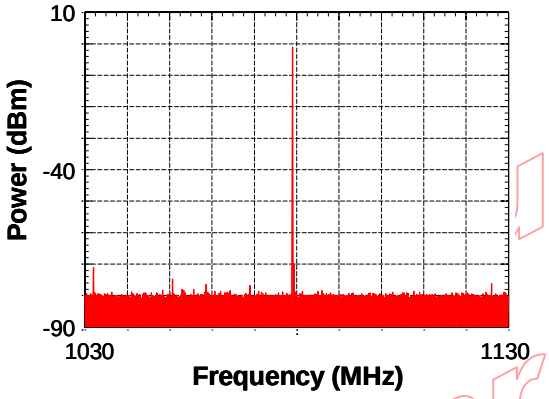
f_{out} = [23/64 + 1/(2^14)] * f_{clk}



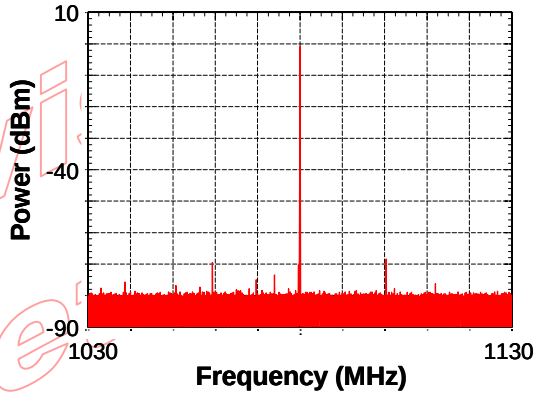
f_{out} = [23/64 + 1/(2^13)] * f_{clk}



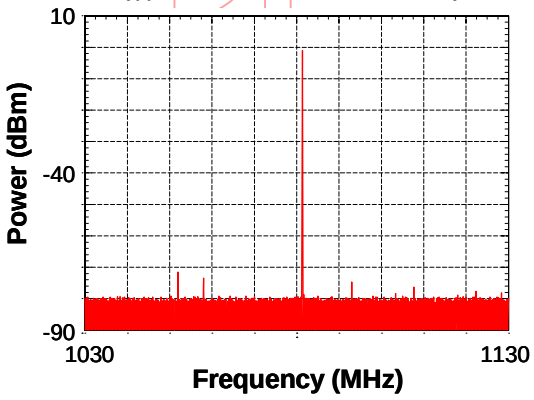
f_{out} = [23/64 + 1/(2^12)] * f_{clk}



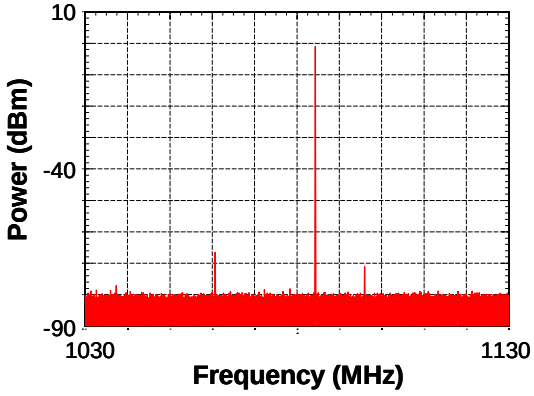
f_{out} = [23/64 + 1/(2^11)] * f_{clk}



f_{out} = [23/64 + 1/(2^10)] * f_{clk}



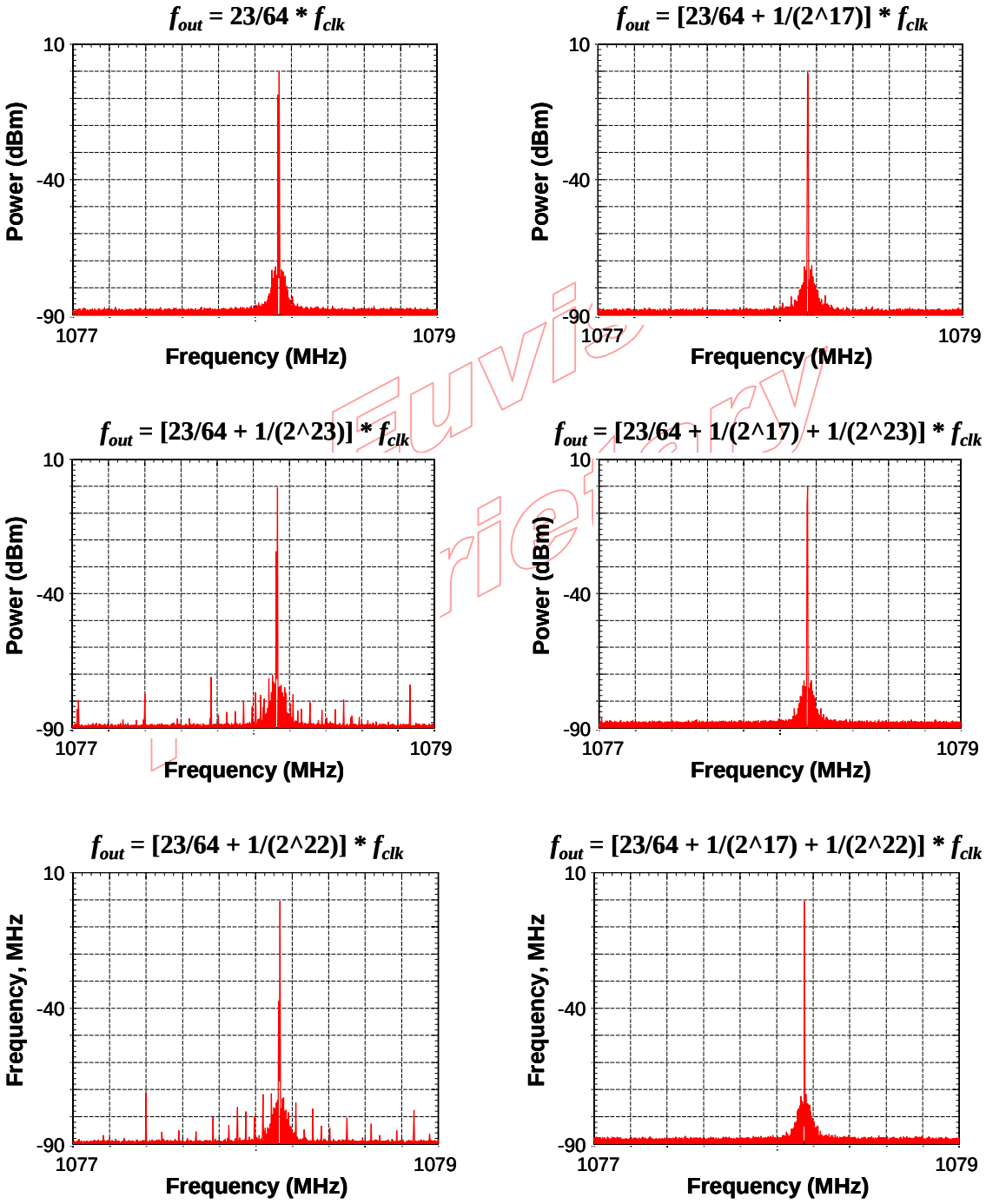
f_{out} = [23/64 + 1/(2^9)] * f_{clk}



Euvis proprietary

Narrow Band (2MHz Span) Spectrum with f_{clk} = 3.0 GHz

The following narrow band 2 MHz bandwidth spectra were measured at a clock rate of 3.0 GHz. The main frequency f_{out} is set at 17/64*f_{clk}. The left column has various single LSB turned on in addition to the main f_{out}. The right column has the same frequency word as the left column, in addition with **Vi15** bit turned on. These spectra should cover the worst spurs due to phase truncations and other dynamic effects beside harmonics.



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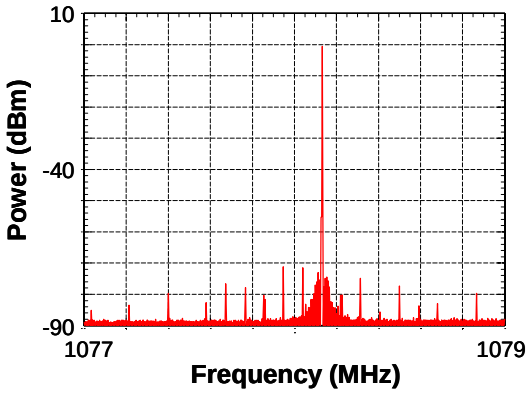
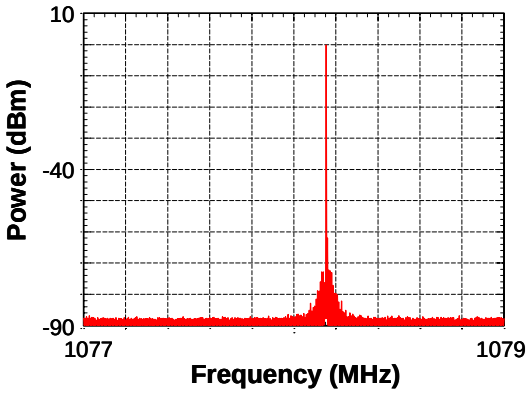
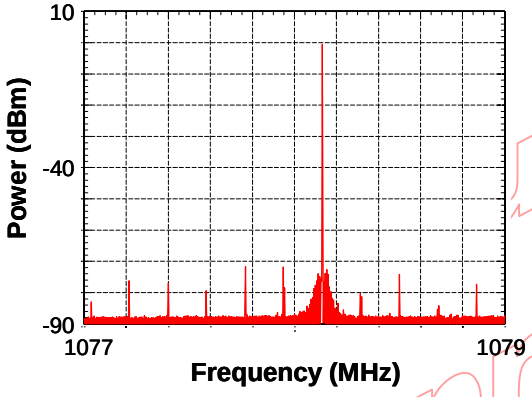
f_{out} = [23/64 + 1/(2^21)] * f_{clk}



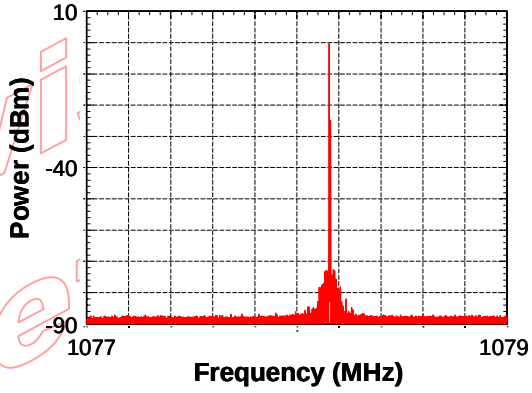
f_{out} = [23/64 + 1/(2^17) + 1/(2^21)] * f_{clk}



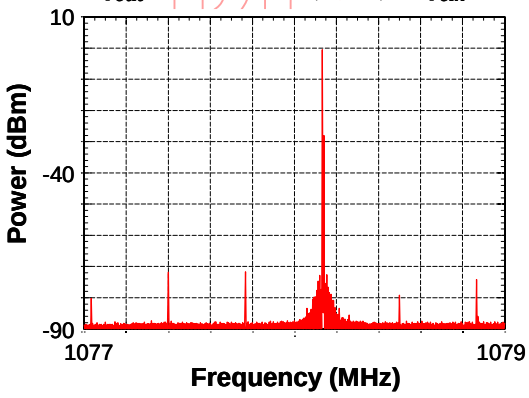
f_{out} = [23/64 + 1/(2^20)] * f_{clk}



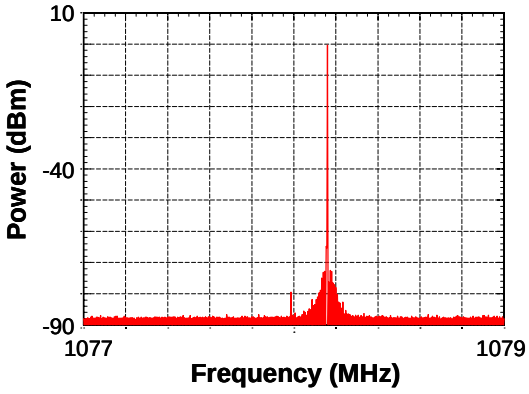
f_{out} = [23/64 + 1/(2^17) + 1/(2^20)] * f_{clk}



f_{out} = [23/64 + 1/(2^19)] * f_{clk}



f_{out} = [23/64 + 1/(2^17) + 1/(2^19)] * f_{clk}



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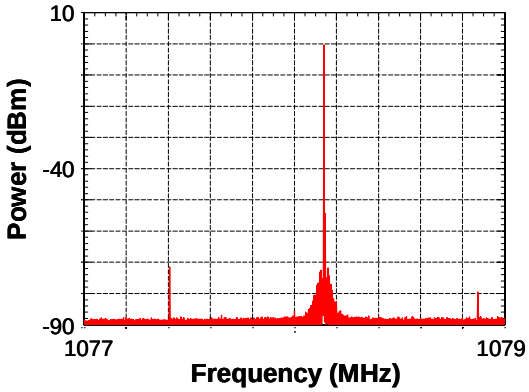
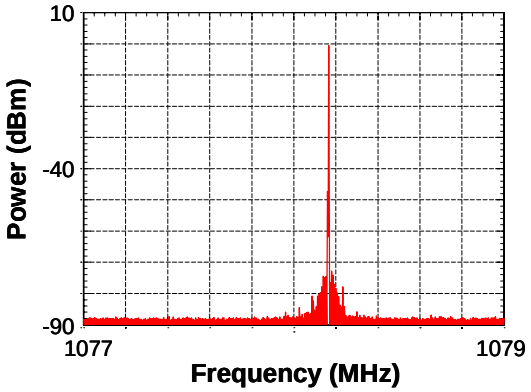
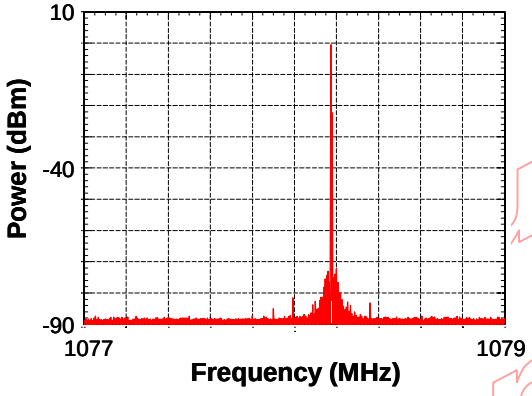
f_{out} = [23/64 + 1/(2^18)] * f_{clk}



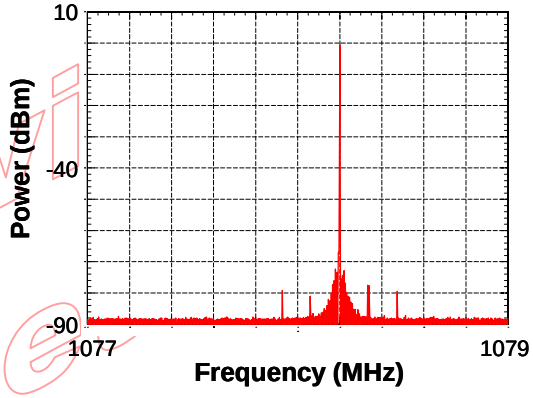
f_{out} = [23/64 + 1/(2^17) + 1/(2^18)] * f_{clk}



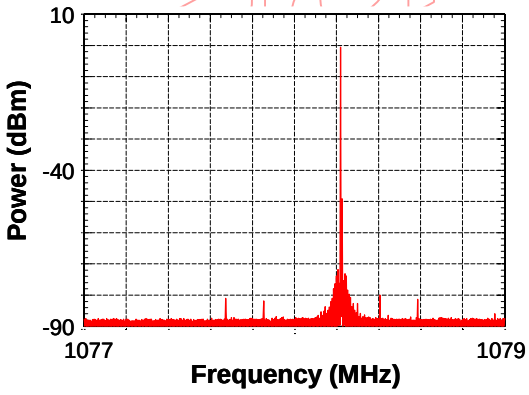
f_{out} = [23/64 + 1/(2^16)] * f_{clk}



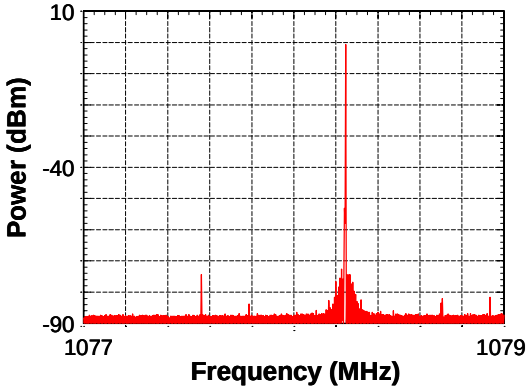
f_{out} = [23/64 + 1/(2^16) + 1/(2^17)] * f_{clk}



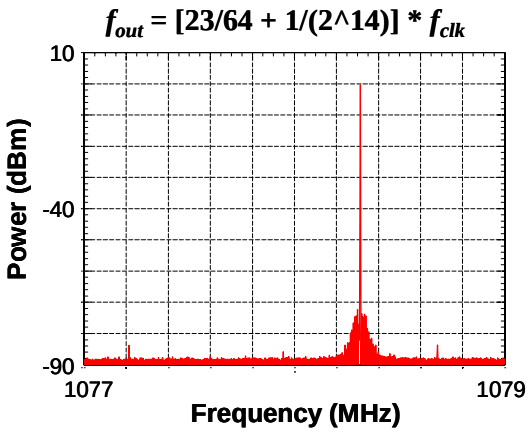
f_{out} = [23/64 + 1/(2^15)] * f_{clk}

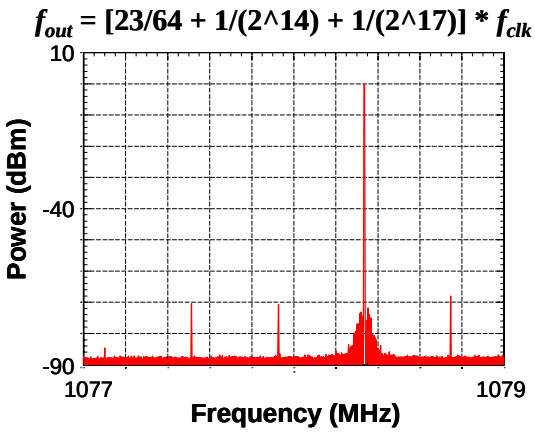


f_{out} = [23/64 + 1/(2^15) + 1/(2^17)] * f_{clk}



Preliminary





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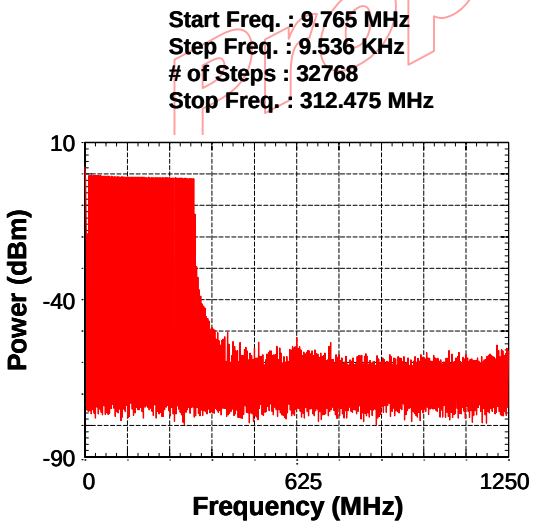
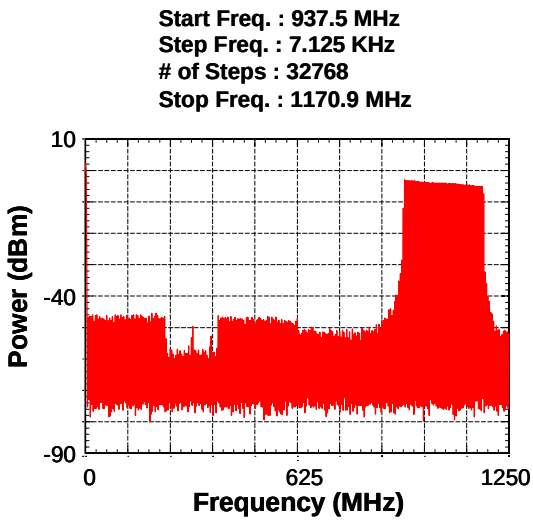
Broadband Band Chirping Spectrum with f_{clk} = 2.5 GHz

The following chirping spectra were measured with **Euvis** DDS module product **DSM301** with DS856 clocked at 2.5 GHz. The frequency was updated at every 8 clock cycles (i.e. every 3.2 ns) for 32768 steps.

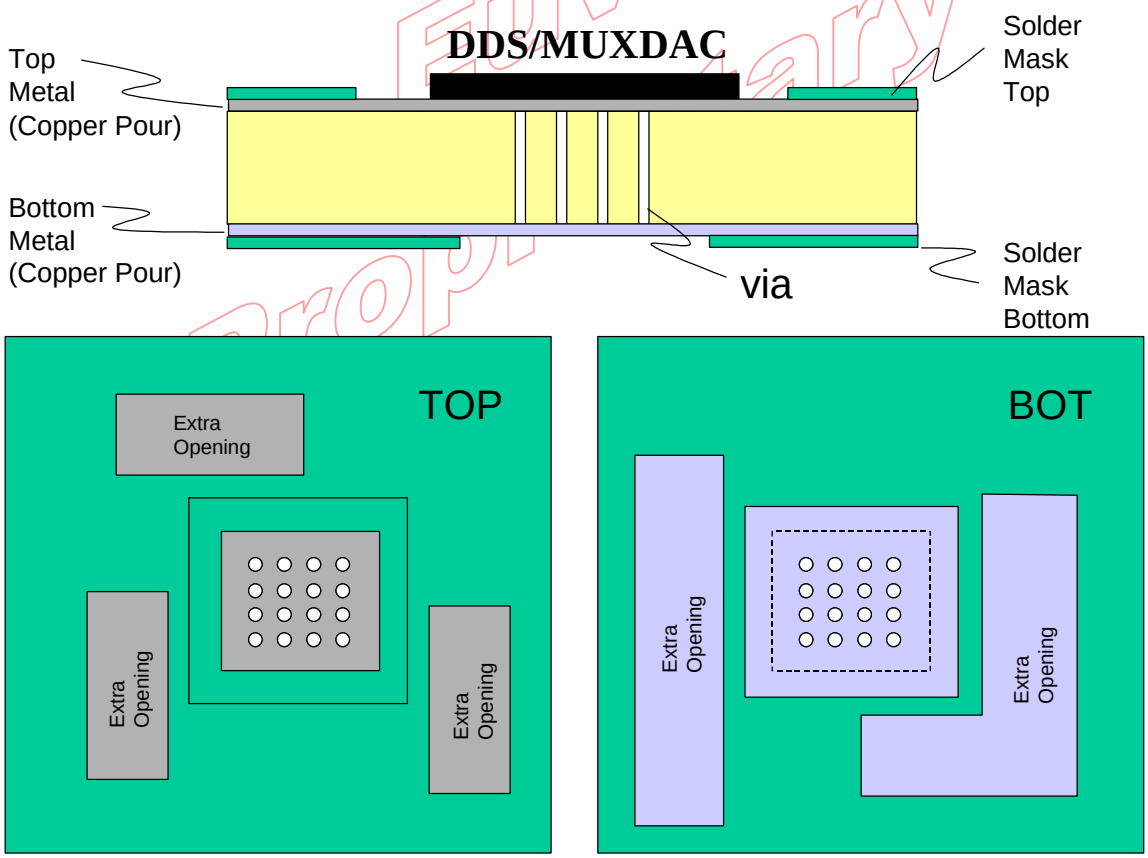




Appendix: PCB Layout – Thermal Performance Enhancement

The thermal resistances of the DDS QFN 9mm x 9mm is about 19 C/W. The major thermal flow is thru the DDS bottom exposed pad. The thermal flow thru the top of the package is also helpful but is only an assistant means.

In order to enhance the thermal performance in the PCB layout, enough vias should be located right under the exposed pad as shown in the following figure. The vias should be without thermal relief to maximize the thermal conduction. On the bottom (BOT), try to open the solder mask bottom (SMB) right under the exposed pad. In the neighbor of the bottom opening, try to add more SMB openings. These extra SMB openings will help thermal conduction and relieve the heat to the ambience. Extra openings on the solder mask top (SMT) help in the similar manner.



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Many heat sinks and joint compounds are available in the open market. The following heat sinks, epoxy and thermal grease are for reference.

1. Heat sink to be applied on top of QFN 9mm x 9mm package:
   www.thermaflo.com Part #: B101015B00000

2. Epoxy to attach heat sinks to plastic package QFN surface:
   Loctite 7387 (Activator) Part # 18861 and
   Loctite 384 (Adhesive) Part # 17099

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