National Semiconductor

DS8629 120 MHz Divide-by-100 Prescaler

General Description

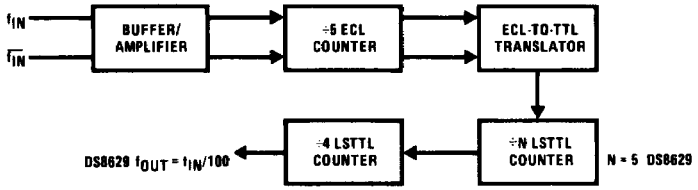
The DS8629 is a fixed ratio counter combining ECL and Low Power Schottky technology on a single monolithic substrate. This provides high frequency capability and TTL compatibility. A single 5.2V ±10% supply is needed.

The device can be operated in a single-ended or differential input mode, with the signal source typically capacitively coupled to the input. An input amplifier is included to allow use of extremely small amplitude, high frequency signals. The output of the device is a square wave of frequency $f_{OUT} = f_{IN}/100$ for the DS8629. The output is standard Low Power Schottky.

Features

- High Frequency, dc—120 MHz—small input amplitude
- Sine wave input 30 MHz < f_{IN} < 120 MHz
- TTL compatible output
- May be used with TTL input
- Single supply operation 5.2V ±10%
- Single ended or differential input modes
- Positive or negative-edge triggered
- Count down sequence avoids broadcast FM IF harmonics

Logic and Connection Diagrams



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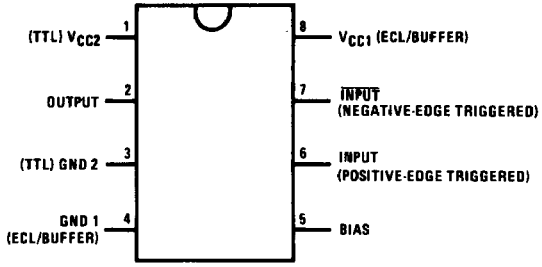
Dual-In-Line Package



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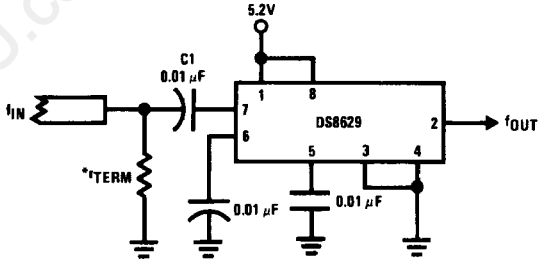
Order Number DS8629N
See NS Package Number N08E

Typical Applications

High Frequency—Single-Ended Input



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*r_{TERM} is the termination impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.68	5.72	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN1(p-p)}$	Input Voltage (Peak-To-Peak)	Single-Ended @ 120 MHz		200		1000	mV
$V_{IN2(p-p)}$	Input Voltage (Peak-To-Peak)	Differential @ 120 MHz		100		1000	mV
f_{SINE}	Input Frequency with Sine Wave	V_{IN} = 600 mVp-p		30		120	MHz
f_{TTL}	Input Frequency with TTL Input			0		120	MHz
dv	Minimum Slew Rate of Square Wave Input	V_{IN} = 600 mVp-p				100	V/μs
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OH} = −10 μA V_{CC} = Min, I_{OH} = −400 μA V_{CC} = Min, I_{OH} = −1.6 mA		2.9 2.4 2.0			V V V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max		−10		−40	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 8 mA DS8629			0.5	V
I_{CC}	Supply Current	V_{CC} = Max	DS8629		90	135	mA
Z_{IN}	Input Impedance	V_{IN} = 0.1 V_{p-p} to 1 V_{p-p} Freq. = 120 MHz		100	200	350	Ω

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 70°C range. All typical values are for T_A = 25°C and V_{CC} = 5.2V.

Note 3: All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Application Hints

OPERATING NOTES

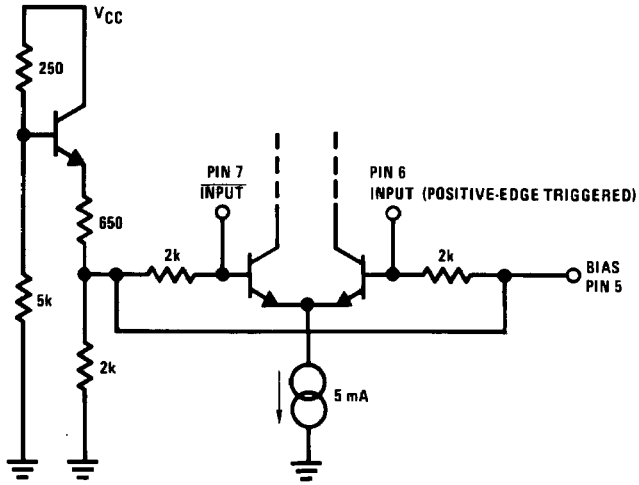
Two ground and two V_{CC} connections are provided separating the ECL and buffer/amplifier stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two grounds externally to a good ground plane and the V_{CC}'s to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimize stray inductance. A well by-passed voltage source should be used.

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.01 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.01 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 30 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 100 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided. If it is desired to use a TTL input signal source, the unused input should have a 10 kΩ resistor added to ground and the input coupling capacitor should be eliminated with the TTL source dc coupled to the input.

The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 160 MHz (typically).

Input Configuration



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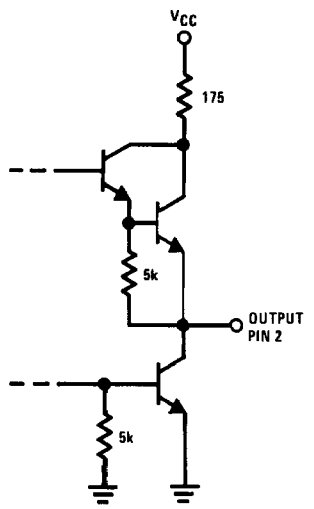
Output Configuration



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