National Semiconductor

# DS8T26A/DS8T26AM/DS8T28/DS8T28M 4-Bit Bidirectional Bus Transceivers

## General Description

The DS8T26A, DS8T28 consist of 4 pairs of TRI-STATE® logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the DS8T26A, DS8T28 from conventional multi-IC implementations. In addition, the DS8T26A, DS8T28's ultra high speed while driving heavy bus capacitance (300 pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

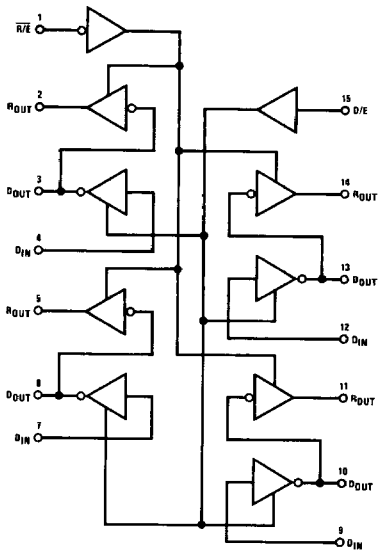
Both the driver and receiver gates have TRI-STATE outputs and low current PNP inputs. PNP inputs reduce input loading to 200 $\mu$A maximum.

## Features

- Inverting outputs in the DS8T26A
- Non-inverting outputs in the DS8T28
- TRI-STATE outputs
- Low current PNP inputs
- Fast switching times (20 ns)
- Advanced Schottky processing
- Driver glitch free power up/down
- Non-overlapping TRI-STATE

## Logic and Connection Diagrams

**DS8T26A**

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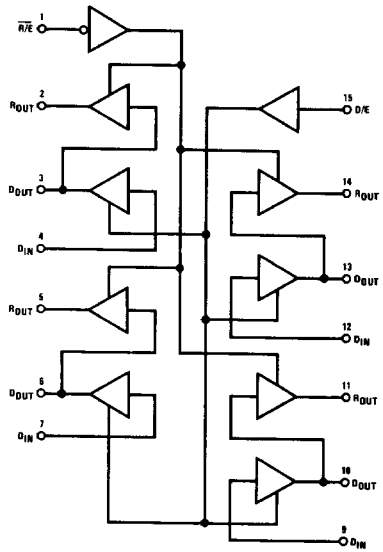
**DS8T28**

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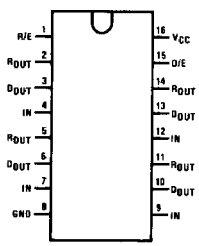
**Dual-In-Line Package**

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**Top View**

**Order Number DS8T26AJ, DS8T26AMJ, DS8T28J, DS8T28MJ, DS8T26AN or DS8T28N**

**See NS Package Number J16A or N16A**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| All Output and Supply Voltages | −0.5V to +7V |
| All Input Voltages | −1V to +5.5V |
| Output Currents | ±150 mA |
| Storage Temperature | −65°C to +150°C |
| Maximum Power Dissipation* at 25°C | |
| Cavity Package | 1509 mW |
| Molded Package | 1476 mW |
| Lead Temperature (Soldering, 4 seconds) | 260°C |

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | | |
| DS8T26A, DS8T28 | 4.75 | 5.25 | V |
| DS8T26AM, DS8T28M | 4.5 | 5.5 | V |
| Temperature ($T_A$) | | | |
| DS8T26A, DS8T28 | 0 | 70 | °C |
| DS8T26AM, DS8T28M | −55 | +125 | °C |

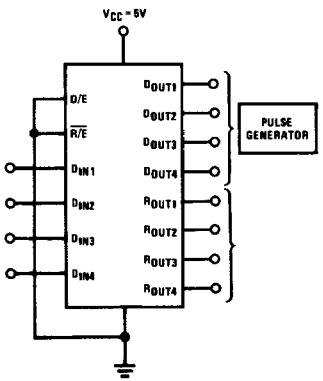
## Electrical Characteristics (Notes 2, 3 and 4)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DRIVER** | | | | | | |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0.4V | | | −200 | μA |
| $I_{IL}$ | Low Level Input Current (Disabled) | $V_{IN}$ = 0.4V | | | −25 | μA |
| $I_{IH}$ | High Level Input Current ($D_{IN}$, $D_E$) | $V_{IN}$ = $V_{CC}$ Max | | | 25 | μA |
| $V_{OL}$ | Low Level Output Voltage (Pins 3, 6, 10, 13) | $I_{OUT}$ = 48 mA | | | 0.5 | V |
| $V_{OH}$ | High Level Output Voltage, (Pins 3, 6, 10, 13) | $I_{OUT}$ = −10 mA | 2.4 | | | V |
| $I_{OS}$ | Short-Circuit Output Current, (Pins 3, 6, 10, 13) | $V_{OUT}$ = 0V, $V_{CC}$ = $V_{CC}$ Max | −50 | | −150 | mA |
| **RECEIVER** | | | | | | |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0.4V | | | −200 | μA |
| $I_{IH}$ | High Level Input Current ($R_E$) | $V_{IN}$ = $V_{CC}$ Max | | | 25 | μA |
| $V_{OL}$ | Low Level Output Voltage | $I_{OUT}$ = 20 mA | | | 0.5 | V |
| $V_{OH}$ | High Level Output Voltage, (Pins 2, 5, 11, 14) | $I_{OUT}$ = −100 μA | 3.5 | | | V |
| | | $I_{OUT}$ = −2 mA | 2.4 | | | V |
| $I_{OS}$ | Short-Circuit Output Current, (Pins 2, 5, 11, 14) | $V_{OUT}$ = 0V, $V_{CC}$ = $V_{CC}$ Max | −30 | | −75 | mA |
| **BOTH DRIVER AND RECEIVER** | | | | | | |
| $V_{TL}$ | Low Level Input Threshold Voltage | $V_{CC}$ = Min, $V_{IN}$ = 0.8V, $I_{OL}$ = Max | 0.85 | | | V |
| $V_{TH}$ | High Level Input Threshold Voltage | $V_{CC}$ = Max, $V_{IN}$ = 0.8V, $I_{OH}$ = Max | | | 2 | V |
| $I_{OZ}$ | Low Level Output OFF Leakage Current | $V_{OUT}$ = 0.5V | | | −100 | μA |
| $I_{OZ}$ | High Level Output OFF Leakage Current | $V_{OUT}$ = 2.4V | | | 100 | μA |
| $V_I$ | Input Clamp Voltage | $I_{IN}$ = −12 mA | | | −1.0 | V |

## Switching Characteristics $V_{CC}$ = 5V, $T_A$ = 25°C

| Symbol | Parameter | Conditions | DS8T26A Max | DS8T28 Max | Units |
|---|---|---|---|---|---|
| **Propagation Delay** | | | | | |
| $t_{ON}$ | $D_{OUT}$ to $R_{OUT}$, *(Figure 1)* | $C_L$ = 30 pF | 14 | 17 | ns |
| $t_{OFF}$ | $D_{OUT}$ to $R_{OUT}$, *(Figure 1)* | | 14 | 17 | ns |
| $t_{ON}$ | $D_{IN}$ to $D_{OUT}$, *(Figure 2)* | $C_L$ = 300 pF | 14 | 17 | ns |
| $t_{OFF}$ | $D_{IN}$ to $D_{OUT}$, *(Figure 2)* | | 14 | 17 | ns |
| **Data Enable to Data Output** | | | | | |
| $t_{PZL}$ | High Z to 0, *(Figure 3)* | $C_L$ = 300 pF | 25 | 28 | ns |
| $t_{PLZ}$ | 0 to High Z, *(Figure 3)* | | 20 | 23 | ns |
| **Receiver Enable to Receiver Output** | | | | | |
| $t_{PZL}$ | High Z to 0, *(Figure 4)* | $C_L$ = 30 pF | 20 | 23 | ns |
| $t_{PLZ}$ | 0 to High Z, *(Figure 4)* | | 15 | 18 | ns |

## AC Test Circuits and Switching Time Waveforms

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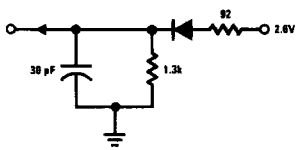


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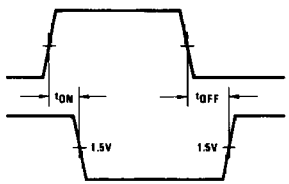


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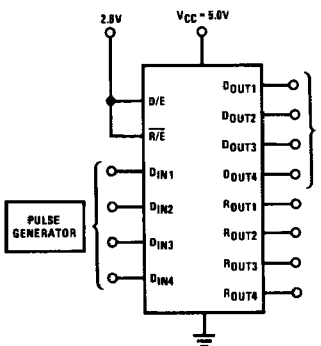
Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

**FIGURE 1. Propagation Delay ($D_{OUT}$ to $R_{OUT}$)**

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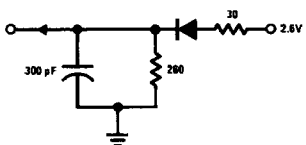


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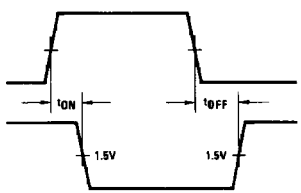


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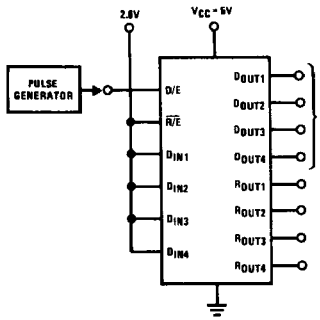
Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

**FIGURE 2. Propagation Delay ($D_{IN}$ to $D_{OUT}$)**

## AC Test Circuits and Switching Time Waveforms (Continued)

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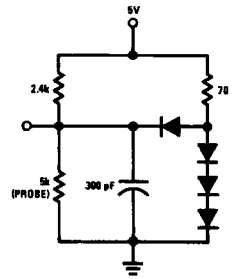


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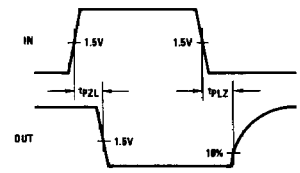


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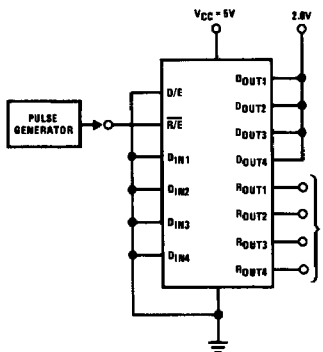
Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

**FIGURE 3. Propagation Delay (Data Enable to Data Output)**

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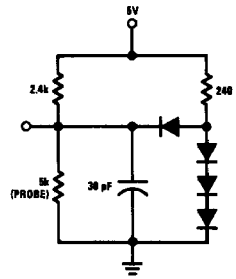


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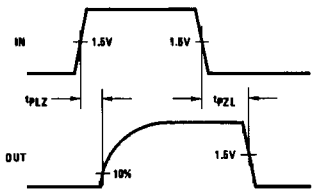


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Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

**FIGURE 4. Propagation Delay ($\overline{\text{Receive/Enable}}$ to Receive Output)**