

DS90C363/DS90CF364 +3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link—65 MHz, +3.3V LVDS Receiver 18-Bit Flat Panel Display (FPD) Link—65 MHz

General Description

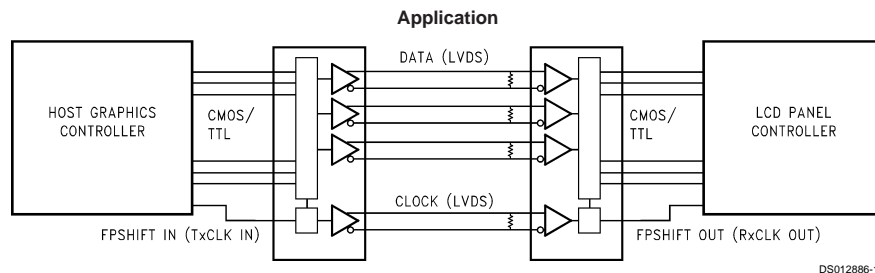
The DS90C363 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CF364 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 170 Mbytes/sec. The Transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphics controllers. The Transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge Transmitter will interoperate with a Falling edge Receiver (DS90CF364) without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

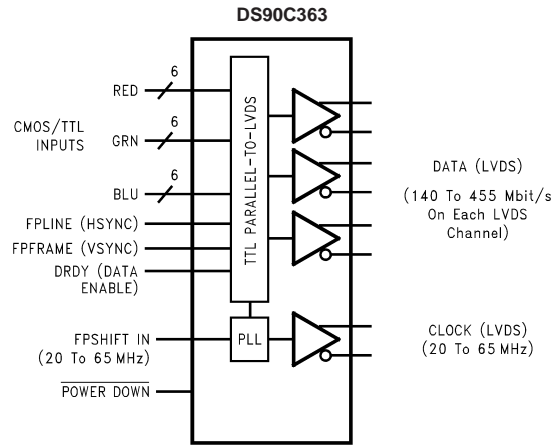
- 20 to 65 MHz shift clock support
- Programmable Transmitter (DS90C363) strobe select (Rising or Falling edge strobe)
- Single 3.3V supply
- Chipset (Tx + Rx) power consumption < 250 mW (typ)
- Power-down mode (< 0.5 mW total)
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and higher addressability.
- Up to 170 Megabyte/sec bandwidth
- Up to 1.3 Gbps throughput
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Falling edge data strobe Receiver
- Compatible with TIA/EIA-644 LVDS standard
- ESD rating > 7 kV
- Operating Temperature: -40°C to +85°C

Block Diagrams



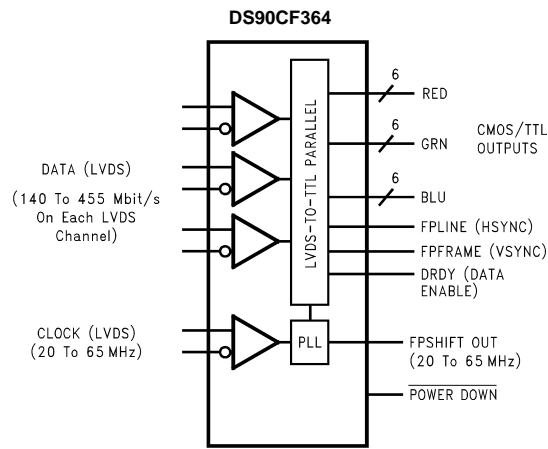
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Block Diagrams (Continued)



DS012886-1

Order Number DS90C363MTD
See NS Package Number MTD48



DS012886-24

Order Number DS90CF364MTD
See NS Package Number MTD48

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| | |
|--|------------------------------|
| Supply Voltage (V_{CC}) | -0.3V to +4V |
| CMOS/TTL Input Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| CMOS/TTL Output Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Receiver Input Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Driver Output Voltage | -0.3V to ($V_{CC} + 0.3V$) |
| LVDS Output Short Circuit Duration | Continuous |
| Junction Temperature | +150°C |
| Storage Temperature | -65°C to +150°C |
| Lead Temperature (Soldering, 4 sec) | +260°C |
| Maximum Package Power Dissipation Capacity 25°C MTD48 (TSSOP) Package: | |

| | |
|----------------------------------|----------------------|
| DS90C363 | 1.98 W |
| DS90CF364 | 1.89 W |
| Package Derating: | |
| DS90C363 | 16 mW/°C above +25°C |
| DS90CF364 | 15 mW/°C above +25°C |
| ESD Rating (HBM, 1.5 kΩ, 100 pF) | > 7 kV |

Recommended Operating Conditions

| | Min | Nom | Max | Units |
|--|-----|-----|-----|------------------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Operating Free Air Temperature (T_A) | -40 | +25 | +85 | °C |
| Receiver Input Range | 0 | | 2.4 | V |
| Supply Noise Voltage (V_{CC}) | | | 100 | mV _{PP} |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|-----------------------------------|--|--|----------------|-------|----------|-------|----|
| CMOS/TTL DC SPECIFICATIONS | | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{CC} | V | |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V | |
| V_{OH} | High Level Output Voltage | $I_{OH} = -0.4$ mA | 2.7 | 3.3 | | V | |
| V_{OL} | Low Level Output Voltage | $I_{OL} = 2$ mA | | 0.06 | 0.3 | V | |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18$ mA | | -0.79 | -1.5 | V | |
| I_{IN} | Input Current | $V_{IN} = V_{CC}$, GND, 2.5V or 0.4V | | ±5.1 | ±10 | μA | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0V$ | | -60 | -120 | mA | |
| LVDS DC SPECIFICATIONS | | | | | | | |
| V_{OD} | Differential Output Voltage | $R_L = 100\Omega$ | 250 | 345 | 450 | mV | |
| ΔV_{OD} | Change in V_{OD} between complimentary output states | | | | 35 | mV | |
| V_{OS} | Offset Voltage (Note 4) | | 1.125 | 1.25 | 1.375 | V | |
| ΔV_{OS} | Change in V_{OS} between complimentary output states | | | | 35 | mV | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0V$, $R_L = 100\Omega$ | | -3.5 | -5 | mA | |
| I_{OZ} | Output TRI-STATE® Current | $\overline{PWR\ DWN} = 0V$, $V_{OUT} = 0V$ or V_{CC} | | ±1 | ±10 | μA | |
| V_{TH} | Differential Input High Threshold | $V_{CM} = +1.2V$ | | | +100 | mV | |
| V_{TL} | Differential Input Low Threshold | | -100 | | | mV | |
| I_{IN} | Input Current | $V_{IN} = +2.4V$, $V_{CC} = 3.6V$ $V_{IN} = 0V$, $V_{CC} = 3.6V$ | | | ±10 | μA | |
| TRANSMITTER SUPPLY CURRENT | | | | | | | |
| ICCTW | Transmitter Supply Current, Worst Case | $R_L = 100\Omega$, $C_L = 5$ pF, Worst Case Pattern (Figures 1, 3), $T_A = -40^\circ C$ to +85°C | $f = 32.5$ MHz | | 31 | 45 | mA |
| | | | $f = 37.5$ MHz | | 32 | 50 | mA |
| | | | $f = 65$ MHz | | 42 | 55 | mA |
| ICCTG | Transmitter Supply Current, 16 Grayscale | $R_L = 100\Omega$, $C_L = 5$ pF, 16 Grayscale Pattern (Figures 2, 3), $T_A = -40^\circ C$ to +85°C | $f = 32.5$ MHz | | 23 | 35 | mA |
| | | | $f = 37.5$ MHz | | 28 | 40 | mA |
| | | | $f = 65$ MHz | | 31 | 45 | mA |

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|-----------------------------------|--|--|----------------|-----|-----|-------|----|
| TRANSMITTER SUPPLY CURRENT | | | | | | | |
| ICCTZ | Transmitter Supply Current Power Down | PWR DWN = Low Driver Outputs in TRI-STATE® under Power Down Mode | | 10 | 55 | μA | |
| RECEIVER SUPPLY CURRENT | | | | | | | |
| ICCRW | Receiver Supply Current, Worst Case | $C_L = 8$ pF, Worst Case Pattern (Figures 1, 4), $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | $f = 32.5$ MHz | | 49 | 65 | mA |
| | | | $f = 37.5$ MHz | | 53 | 70 | mA |
| | | | $f = 65$ MHz | | 78 | 105 | mA |
| ICCRG | Receiver Supply Current, 16 Grayscale | $C_L = 8$ pF, 16 Grayscale Pattern (Figures 2, 4), $T_A =$ -40°C to $+85^\circ\text{C}$ | $f = 32.5$ MHz | | 28 | 45 | mA |
| | | | $f = 37.5$ MHz | | 30 | 47 | mA |
| | | | $f = 65$ MHz | | 43 | 60 | mA |
| ICCRZ | Receiver Supply Current Power Down | PWR DWN = Low Receiver Outputs Stay Low during Power Down Mode | | 10 | 55 | μA | |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{CC} = 3.3\text{V}$ and $T_A = +25^\circ\text{C}$.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM} .

Transmitter Switching Characteristics

Over recommended operating supply and -40°C to $+85^{\circ}\text{C}$ ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Units | |
|--------|---|------------|------|-------|-------|----|
| LLHT | LVDS Low-to-High Transition Time (Figure 3) | | 0.75 | 1.5 | ns | |
| LHLT | LVDS High-to-Low Transition Time (Figure 3) | | 0.75 | 1.5 | ns | |
| TCIT | TxCLK IN Transition Time (Figure 5) | | | 5 | ns | |
| TCCS | TxOUT Channel-to-Channel Skew (Figure 6) | | 250 | | ps | |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 17) | f = 65 MHz | -0.4 | 0 | 0.3 | ns |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 | | 1.8 | 2.2 | 2.5 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 4.0 | 4.4 | 4.7 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | | 6.2 | 6.6 | 6.9 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 | | 8.4 | 8.8 | 9.1 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 | | 10.6 | 11.0 | 11.3 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 | | 12.8 | 13.2 | 13.5 | ns |
| TCIP | TxCLK IN Period (Figure 7) | 15 | T | 50 | ns | |
| TCIH | TxCLK IN High Time (Figure 7) | 0.35T | 0.5T | 0.65T | ns | |
| TCIL | TxCLK IN Low Time (Figure 7) | 0.35T | 0.5T | 0.65T | ns | |
| TSTC | TxIN Setup to TxCLK IN (Figure 7) | f = 65 MHz | 2.5 | | | ns |
| THTC | TxIN Hold to TxCLK IN (Figure 7) | | 0 | | | ns |
| TCCD | TxCLK IN to TxCLK OUT Delay 25°C , $V_{\text{CC}} = 3.3\text{V}$ (Figure 9) | 3.0 | 3.7 | 5.5 | ns | |
| TPLLS | Transmitter Phase Lock Loop Set (Figure 11) | | | 10 | ms | |
| TPDD | Transmitter Power Down Delay (Figure 15) | | | 100 | ns | |

Receiver Switching Characteristics

Over recommended operating supply and -40°C to $+85^{\circ}\text{C}$ ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Units | |
|--------|--|------------|------|------|---------------|----|
| CLHT | CMOS/TTL Low-to-High Transition Time (Figure 4) | | 2.2 | 5.0 | ns | |
| CHLT | CMOS/TTL High-to-Low Transition Time (Figure 4) | | 2.2 | 5.0 | ns | |
| RSPos0 | Receiver Input Strobe Position for Bit 0 (Figure 18) | f = 65 MHz | 0.7 | 1.1 | 1.4 | ns |
| RSPos1 | Receiver Input Strobe Position for Bit 1 | | 2.9 | 3.3 | 3.6 | ns |
| RSPos2 | Receiver Input Strobe Position for Bit 2 | | 5.1 | 5.5 | 5.8 | ns |
| RSPos3 | Receiver Input Strobe Position for Bit 3 | | 7.3 | 7.7 | 8.0 | ns |
| RSPos4 | Receiver Input Strobe Position for Bit 4 | | 9.5 | 9.9 | 10.2 | ns |
| RSPos5 | Receiver Input Strobe Position for Bit 5 | | 11.7 | 12.1 | 12.4 | ns |
| RSPos6 | Receiver Input Strobe Position for Bit 6 | | 13.9 | 14.3 | 14.6 | ns |
| RSKM | RxIN Skew Margin (Note 5) (Figure 19) | f = 65 MHz | 400 | | ps | |
| RCOP | RxCLK OUT Period (Figure 8) | 15 | T | 50 | ns | |
| RCOH | RxCLK OUT High Time (Figure 8) | f = 65 MHz | 7.3 | 8.6 | ns | |
| RCOL | RxCLK OUT Low Time (Figure 8) | f = 65 MHz | 3.45 | 4.9 | ns | |
| RSRC | RxOUT Setup to RxCLK OUT (Figure 8) | f = 65 MHz | 2.5 | 6.9 | ns | |
| RHRC | RxOUT Hold to RxCLK OUT (Figure 8) | f = 65 MHz | 2.5 | 5.7 | ns | |
| RCCD | RxCLK IN to RxCLK OUT Delay 25°C , $V_{\text{CC}} = 3.3\text{V}$ (Figure 10) | 5.0 | 7.1 | 9.0 | ns | |
| RPLLS | Receiver Phase Lock Loop Set (Figure 12) | | | 10 | ms | |
| RPDD | Receiver Power Down Delay (Figure 16) | | | 1 | μs | |

Note 5: Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

AC Timing Diagrams

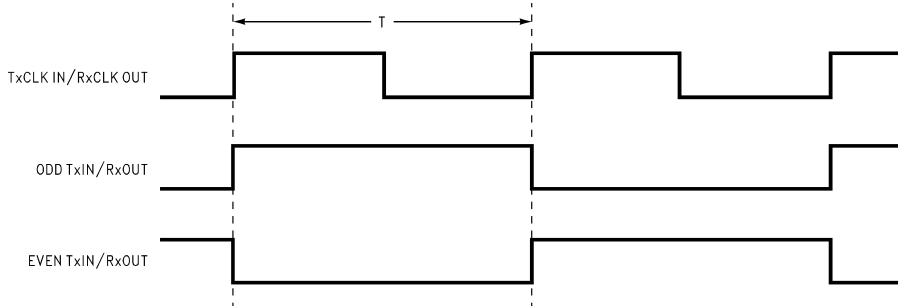


FIGURE 1. "Worst Case" Test Pattern

DS012886-2

AC Timing Diagrams (Continued)

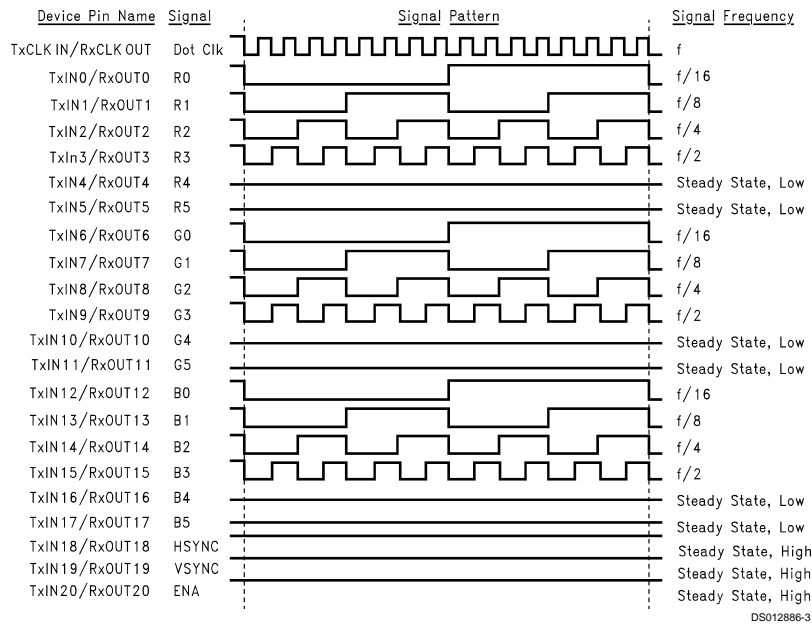


FIGURE 2. "16 Grayscale" Test Pattern (Notes 6, 7, 8, 9)

Note 6: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 7: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 8: Figures 1, 2 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Note 9: Recommended pin to signal mapping. Customer may choose to define differently.

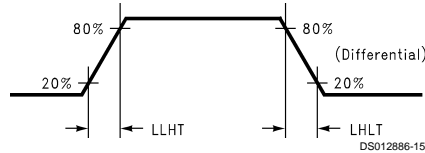


FIGURE 3. DS90C363 (Transmitter) LVDS Output Load and Transition Times

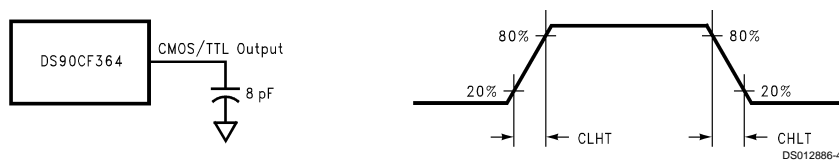


FIGURE 4. DS90CF364 (Receiver) CMOS/TTL Output Load and Transition Times

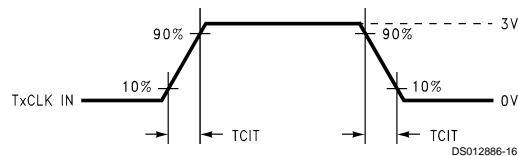
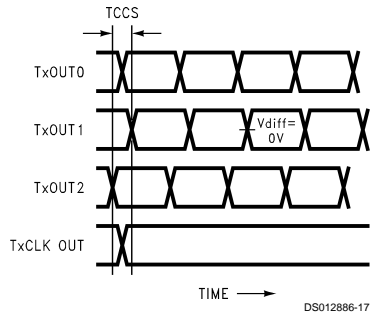


FIGURE 5. DS90C363 (Transmitter) Input Clock Transition Time

AC Timing Diagrams (Continued)



Measurements at $V_{diff}=0V$
 TCCS measured between earliest and latest LVDS edges
 TxCLK Differential Low \rightarrow High Edge

FIGURE 6. DS90C363 (Transmitter) Channel-to-Channel Skew

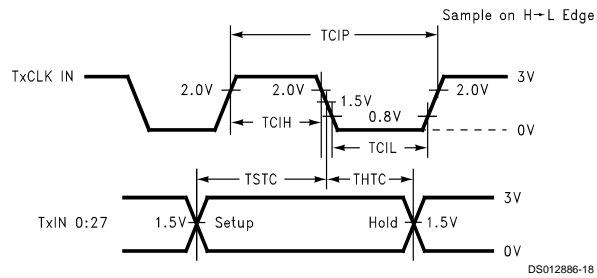


FIGURE 7. DS90C363 (Transmitter) Setup/Hold and High/Low Times

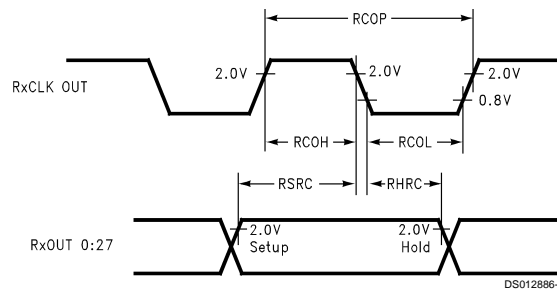


FIGURE 8. DS90CF364 (Receiver) Setup/Hold and High/Low Times

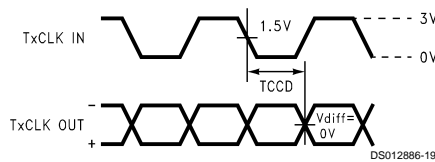


FIGURE 9. DS90C363 (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

AC Timing Diagrams (Continued)

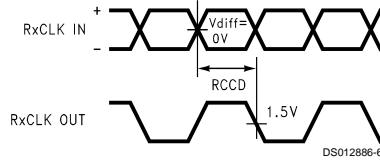


FIGURE 10. DS90CF364 (Receiver) Clock In to Clock Out Delay

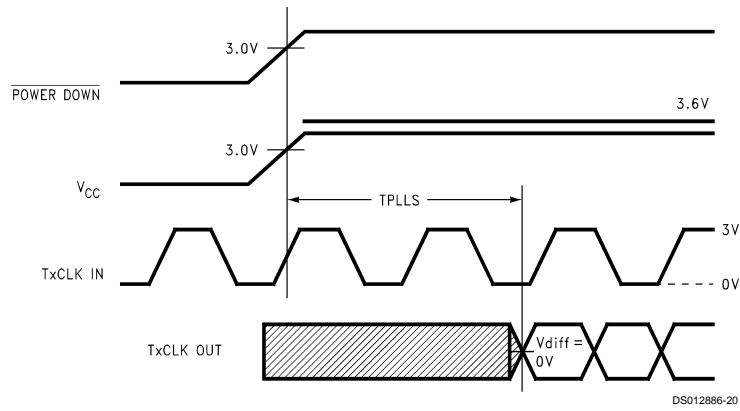


FIGURE 11. DS90C363 (Transmitter) Phase Lock Loop Set Time

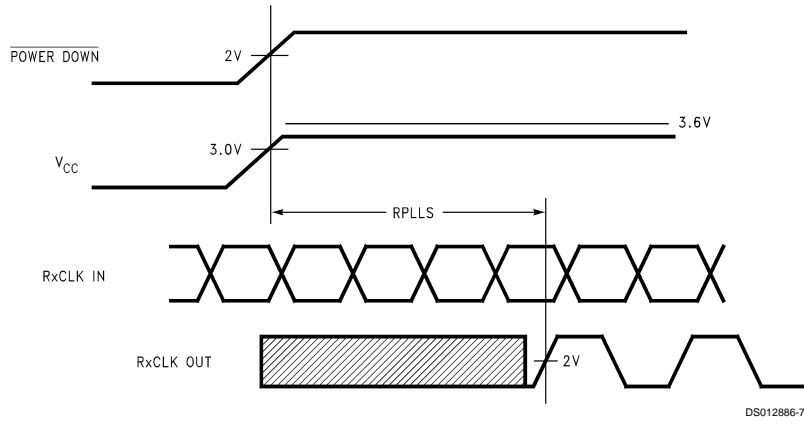


FIGURE 12. DS90CF364 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

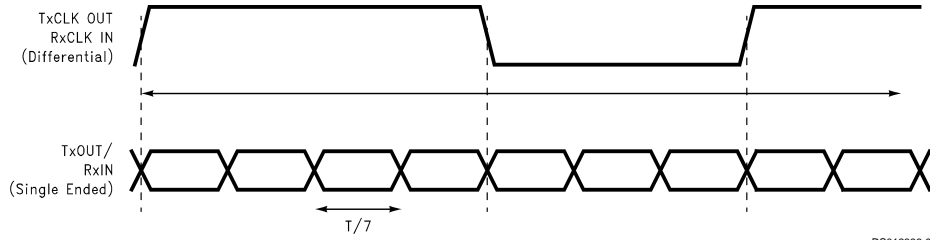


FIGURE 13. Seven Bits of LVDS in One Clock Cycle

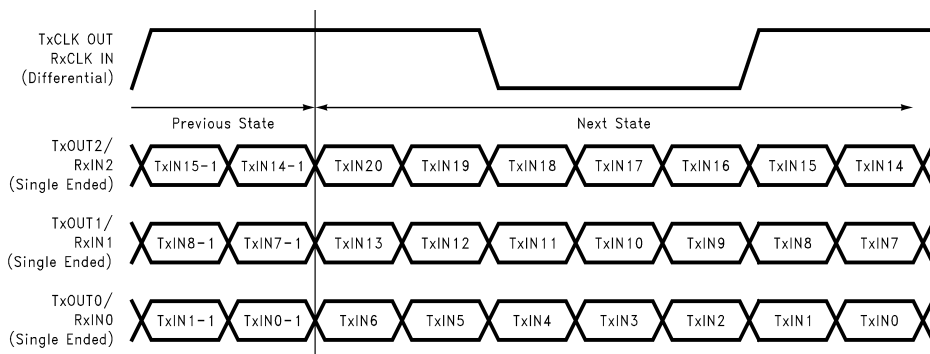


FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

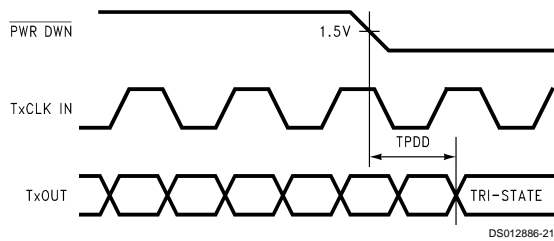


FIGURE 15. Transmitter Power Down Delay

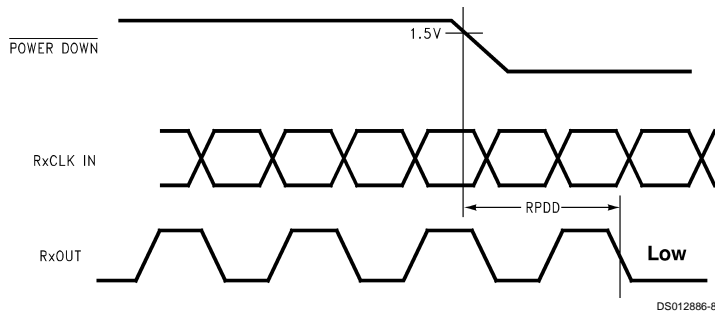
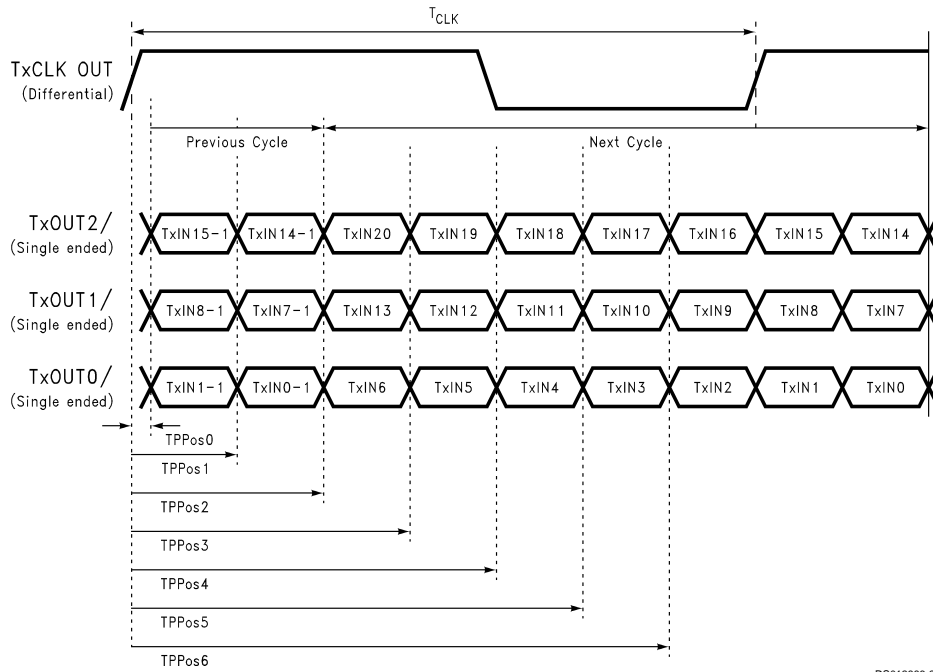


FIGURE 16. Receiver Power Down Delay

AC Timing Diagrams (Continued)



DS012886-22

FIGURE 17. Transmitter LVDS Output Pulse Position Measurement

AC Timing Diagrams (Continued)

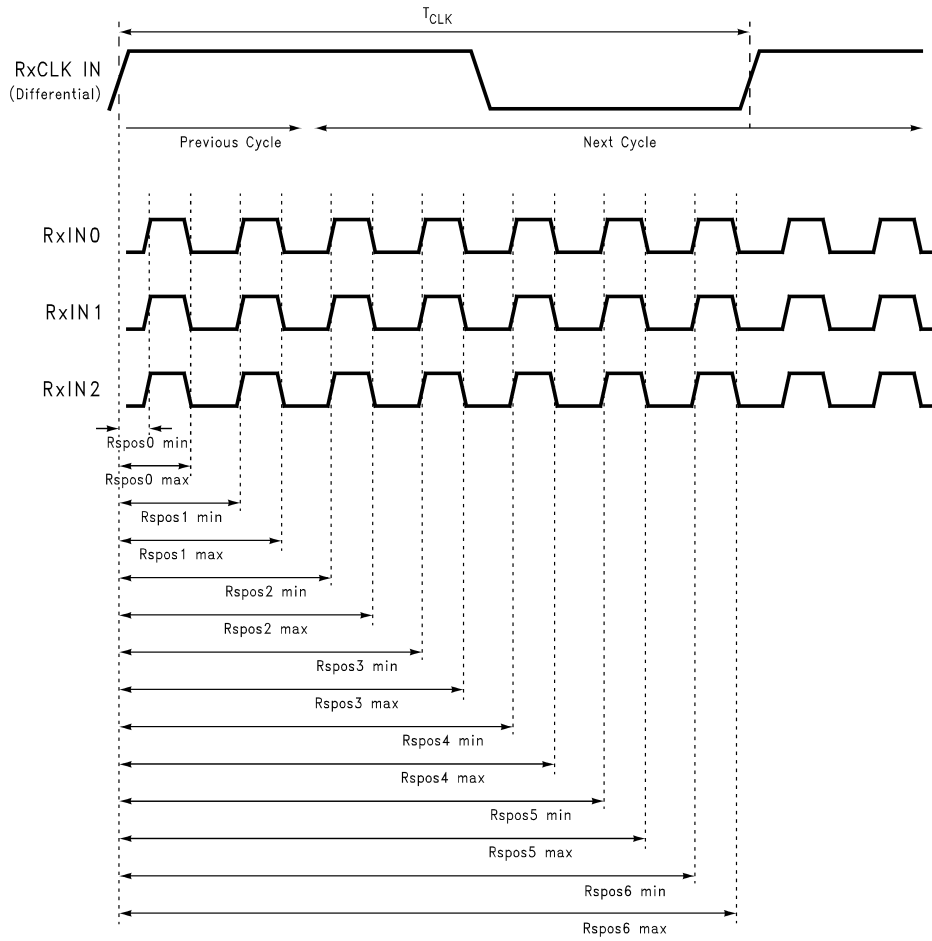
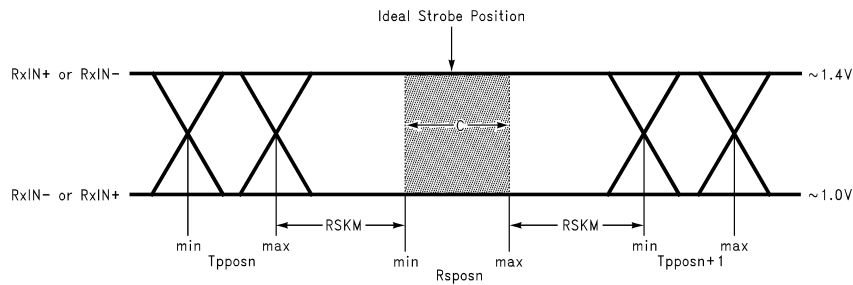


FIGURE 18. Receiver LVDS Input Strobe Position

DS012886-25

AC Timing Diagrams (Continued)



DS012896-11

C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
 Tppos — Transmitter output pulse position (min and max)

RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) (Note 10) + ISI (Inter-symbol interference) (Note 11)
 Cable Skew — typically 10 ps–40 ps per foot, media dependent

Note 10: Cycle-to-cycle jitter is less than 250 ps at 65 MHz.

Note 11: ISI is dependent on interconnect length; may be zero.

FIGURE 19. Receiver LVDS Input Skew Margin

DS90C363 Pin Description—FPD Link Transmitter

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|--|
| TxIN | I | 21 | TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines — FPLINE, FPFFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable). |
| TxOUT+ | O | 3 | Positive LVDS differential data output. |
| TxOUT- | O | 3 | Negative LVDS differential data output. |
| FPSHIFT IN | I | 1 | TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN. |
| R_FB | I | 1 | Programmable strobe select. |
| RTxCLK OUT+ | O | 1 | Positive LVDS differential clock output. |
| TxCLK OUT- | O | 1 | Negative LVDS differential clock output. |
| PWR DWN | I | 1 | TTL level input. When asserted (low input) TRI-STATES the outputs, ensuring low current at power down. |
| V _{CC} | I | 3 | Power supply pins for TTL inputs. |
| GND | I | 4 | Ground pins for TTL inputs. |
| PLL V _{CC} | I | 1 | Power supply pin for PLL. |
| PLL GND | I | 2 | Ground pins for PLL. |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS outputs. |
| LVDS GND | I | 3 | Ground pins for LVDS outputs. |

DS90CF364 Pin Description—FPD Link Receiver

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|--|
| RxIN+ | I | 3 | Positive LVDS differential data inputs. |
| RxIN- | I | 3 | Negative LVDS differential data inputs. |
| RxOUT | O | 21 | TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable). |
| RxCLK IN+ | I | 1 | Positive LVDS differential clock input. |
| RxCLK IN- | I | 1 | Negative LVDS differential clock input. |
| FPSHIFT OUT | O | 1 | TTL level clock output. The falling edge acts as data strobe. Pin name RxCLK OUT. |
| PWR DWN | I | 1 | TTL level input. When asserted (low input) the receiver outputs are low. |
| V _{CC} | I | 4 | Power supply pins for TTL outputs. |
| GND | I | 5 | Ground pins for TTL outputs. |
| PLL V _{CC} | I | 1 | Power supply for PLL. |
| PLL GND | I | 2 | Ground pin for PLL. |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS inputs. |
| LVDS GND | I | 3 | Ground pins for LVDS inputs. |

Applications Information

The DS90C363 and DS90CF364 are backward compatible with the existing 5V FPD Link transmitter/receiver pair (DS90CF563 and DS90CF564). To upgrade from a 5V to a 3.3V system the following must be addressed:

- Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of both the transmitter and receiver devices. This change may enable the removal of a 5V supply from the system, and power may be supplied from an existing 3V power source.
- The DS90C363 (transmitter) incorporates a rise/fall strobe select pin. This select function is on pin 14, formerly a V_{CC} connection on the 5V products. When the rise/fall strobe select pin is connected to V_{CC}, the part is configured with a rising edge strobe. In a system currently using a 5V rising edge strobe transmitter (DS90CR563), no layout changes are required to accommodate the new rise/fall select pin on the 3.3V transmitter. The V_{CC} signal may remain at pin 14, and the device will be configured with a rising edge strobe.
When converting from a 5V falling edge transmitter (DS90CF563) to the 3V transmitter a minimal board layout change is necessary. The 3.3V transmitter will not be configured with a falling edge strobe if V_{CC} remains connected to the select pin. To guarantee the 3.3V transmitter functions with a falling edge strobe pin 14 should be connected to ground OR left unconnected. When not connected (left open) and internal pull-down resistor ties pin 14 to ground, thus configuring the transmitter with a falling edge strobe.
- The DS90C363 transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.

Pin Diagram

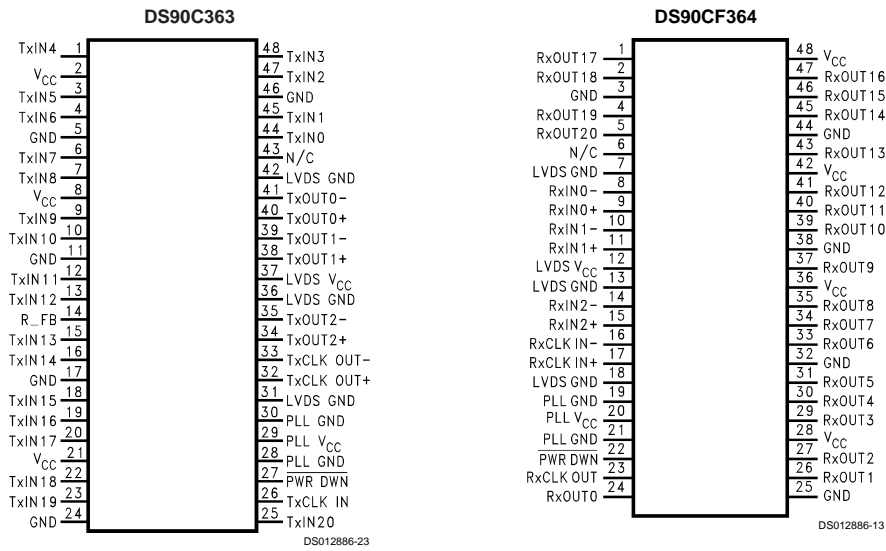
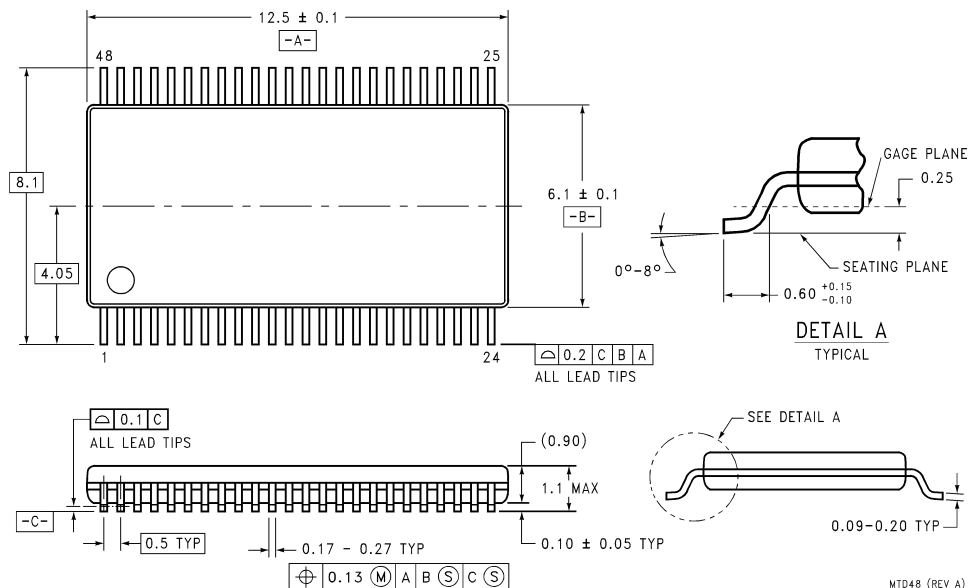


TABLE 1. Programmable Transmitter

| Pin | Condition | Strobe Status |
|------|------------------------|---------------------|
| R_FB | R_FB = V _{CC} | Rising edge strobe |
| R_FB | R_FB = GND | Falling edge strobe |

DS90C363/DS90CF364 +3.3V Programmable LVDS 18-Bit-Color Flat Panel Display (FPD) Link— 65 MHz

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Molded Thin Shrink Small Outline Package, JEDEC
 Dimensions show in millimeters
 Order Number DS90C363MTD and DS90CF364MTD
 NS Package Number MTD48

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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