+3.3V Programmable LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link -65 MHz

Check for Samples: DS90CF363B

FEATURES

- **No Special Start-up Sequence Required between Clock/Data and /PD Pins. Input Signal (Clock and Data) can be Applied Either Before or After the Device is Powered.**
- **Support Spread Spectrum Clocking up to 100KHz Frequency Modulation & Deviations of ±2.5% Center Spread or −5% Down Spread.**
- **"Input Clock Detection" Feature will Pull all LVDS Pairs to Logic Low when Input Clock is Missing and when /PD Pin is Logic High.**
- **18 to 68 MHz Shift Clock Support**
- **Best–in–Class Set & Hold Times on TxINPUTs**
- **Tx Power Consumption < 130 mW (typ) @65MHz Grayscale**
- **40% Less Power Dissipation than BiCMOS Alternatives**
- **Tx Power-Down Mode < 37µW (typ)**
- **Supports VGA, SVGA, XGA and Dual Pixel SXGA.**
- **Narrow Bus Reduces Cable Size and Cost**
- **Up to 1.3 Gbps Throughput**
- **Up to 170 Megabytes/sec Bandwidth**
- **345 mV (typ) Swing LVDS Devices for Low EMI**
- **PLL Requires no External Components**
- **Compatible with TIA/EIA-644 LVDS Standard**
- **Low Profile 48-lead TSSOP Package**
- **Improved Replacement for:**
  - **SN75LVDS84, DS90CF363A**

DESCRIPTION

The DS90CF363B transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 170 Mbytes/sec. The DS90CF363B is fixed as a Falling edge strobe transmitter and will interoperate with a Falling edge strobe Receiver (DS90CF366) without any translation logic.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Block Diagram

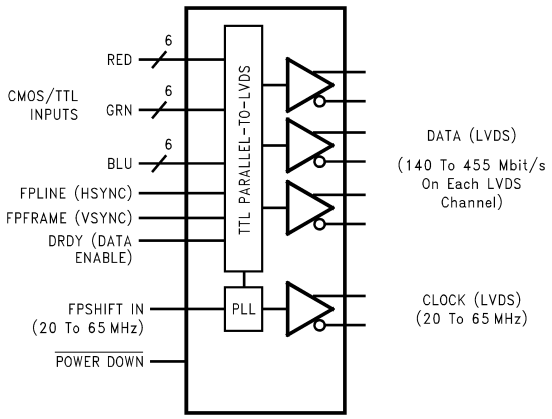


Figure 1. DS90CF363B
See Package Number DGG0048A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

	Value	Unit
Supply Voltage (V_{CC})	−0.3 to +4	V
CMOS/TTL Input Voltage	−0.3 to (V_{CC} + 0.3)	V
LVDS Driver Output Voltage	−0.3 to (V_{CC} + 0.3)	V
LVDS Output Short Circuit Duration	Continuous	
Junction Temperature	+150	°C
Storage Temperature	−65 to +150	°C
Lead Temperature (Soldering, 4 sec)	+260	°C
Maximum Package Power Dissipation Capacity @ 25°C		
DGG-48 (TSSOP) Package: DS90CF363B	1.98	W
Package Derating: DS90CF363B	16 mW/°C above +25°C	
ESD Rating (HBM, 1.5 kΩ, 100 pF)	7	kV
ESD Rating (EIAJ, 0Ω, 200 pF)	500	V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. Electrical Characteristics specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Supply Noise Voltage (V_{CC})			200	mV_{PP}
TxCLKIN frequency	18		68	MHz

Electrical Characteristics (1)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+10	µA
		V_{IN} = GND	−10	0		µA
LVDS DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states				35	mV
V_{OS}	Offset Voltage (3)		1.13	1.25	1.38	V
ΔV_{OS}	Change in V_{OS} between complimentary output states				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		−3.5	−5	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).
(2) Typical values are given for V_{CC} = 3.3V and T_A = +25°C unless specified otherwise.
(3) V_{OS} previously referred as V_{CM}.

Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Units
I_{OZ}	Output TRI-STATE Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 2 and Figure 5) " Typ " values are given for V_{CC} = 3.6V and T_A = +25°C, " Max " values are given for V_{CC} = 3.6V and T_A = −10°C	f = 25 MHz		29	40	mA
			f = 40 MHz		34	45	mA
			f = 65 MHz		42	55	mA
ICCTG	Transmitter Supply Current 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern (Figure 3 and Figure 5) " Typ " values are given for V_{CC} = 3.6V and T_A = +25°C, " Max " values are given for V_{CC} = 3.6V and T_A = −10°C	f = 25 MHz		28	40	mA
			f = 40 MHz		32	45	mA
			f = 65 MHz		39	50	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE under Power Down Mode			11	150	µA

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time (Figure 6)			5	ns
TCIP	TxCLK IN Period (Figure 7)	14.7	T	50.0	ns
TCIH	TxCLK IN High Time (Figure 7)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 7)	0.35T	0.5T	0.65T	ns
TXIT	TxIN, and $\overline{\text{Power Down}}$ pin transition Time	1.5		6.0	ns
TXPD	Minimum pulse width for $\overline{\text{Power Down}}$ pin signal	1			us

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 5)			0.75	1.4	ns
LHLT	LVDS High-to-Low Transition Time (Figure 5)			0.75	1.4	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)[1]	f = 65 MHz	−0.20	0	+0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		2.00	2.20	2.40	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.20	4.40	4.60	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.39	6.59	6.79	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.59	8.79	8.99	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.70	10.99	11.19	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.99	13.19	13.39	ns

(1) The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)(1)	f = 40 MHz	−0.25	0	+0.25	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		3.32	3.57	3.82	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.89	7.14	7.39	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		10.46	10.71	10.96	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		14.04	14.29	14.54	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17.61	17.86	18.11	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		21.18	21.43	21.68	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)(1)	f = 25MHz	−0.45	0	+0.45	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		5.26	5.71	6.16	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		10.98	11.43	11.88	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		16.69	17.14	17.59	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		22.41	22.86	23.31	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		28.12	28.57	29.02	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		33.84	34.29	34.74	ns
TSTC	TxIN Setup to TxCLK IN (Figure 7)		2.5			ns
THTC	TxIN Hold to TxCLK IN (Figure 7)		0.5			ns
TCCD	TxCLK IN to TxCLK OUT Delay (Figure 8) 50% duty cycle input clock is assumed, T_A= −10°C, and 65MHz for " Min ", T_A = 70°C, and 25MHz for " Max ", V_{CC} = 3.6V		3.011		6.082	ns
SSCG	Spread Spectrum Clock support; Modulation frequency with a linear profile (2)	f = 25 MHz		100KHz ± 2.5%/−5%		
		f = 40 MHz		100KHz ± 2.5%/−5%		
		f = 65 MHz		100KHz ± 2.5%/−5%		
TPLLS	Transmitter Phase Lock Loop Set (Figure 9)				10	ms
TPDD	Transmitter Power Down Delay (Figure 11)				100	ns

(2) Care must be taken to ensure TSTC and THTC are met so input data are sampling correctly. This SSCG parameter only shows the performance of tracking Spread Spectrum Clock applied to TxCLK IN pin, and reflects the result on TxCLKOUT+ and TxCLK− pins.

AC Timing Diagrams

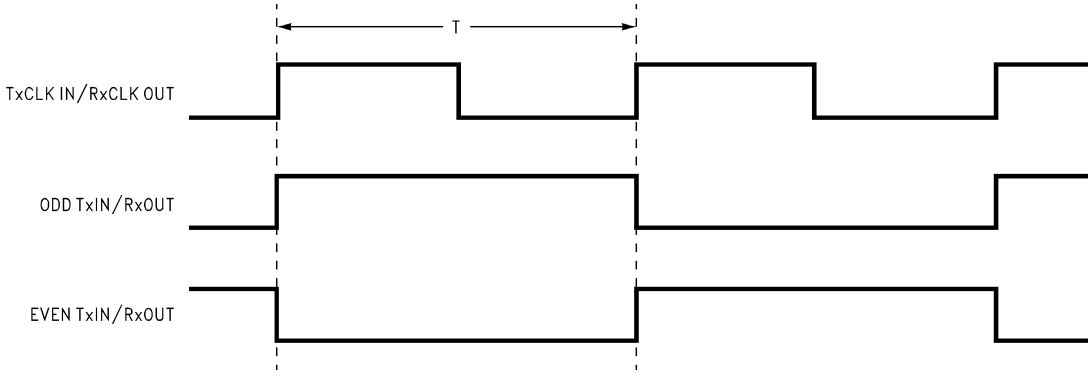
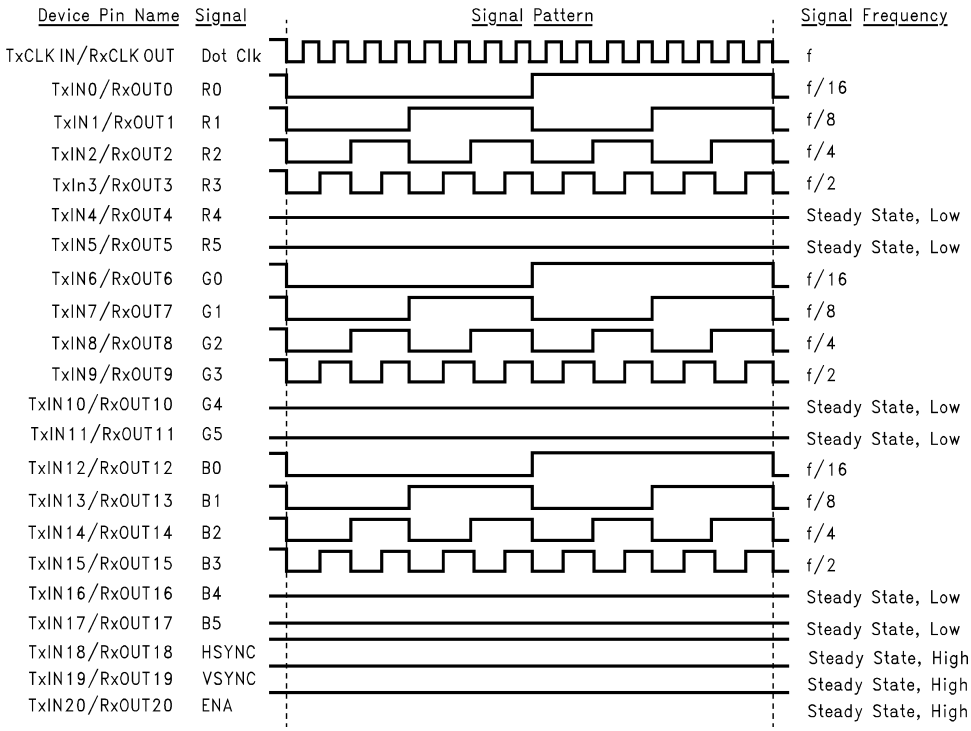


Figure 2. “Worst Case” Test Pattern



The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Figure 2 and Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Recommended pin to signal mapping. Customer may choose to define differently.

Figure 3. “16 Grayscale” Test Pattern

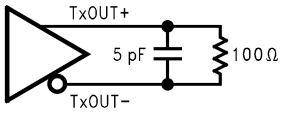


Figure 4. DS90CF363B (Transmitter) LVDS Output Load

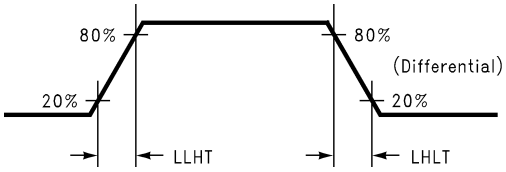


Figure 5. DS90CF363B (Transmitter) LVDS Transition Times

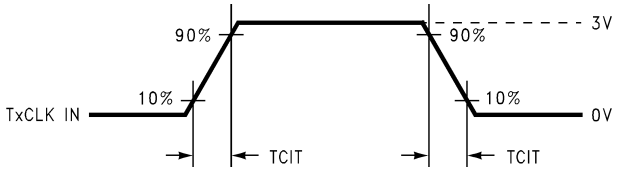


Figure 6. DS90CF363B (Transmitter) Input Clock Transition Time

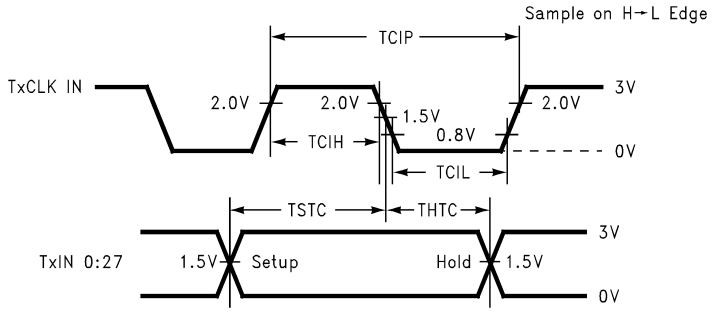


Figure 7. DS90CF363B (Transmitter) Setup/Hold and High/Low Times (Falling Edge Strobe)

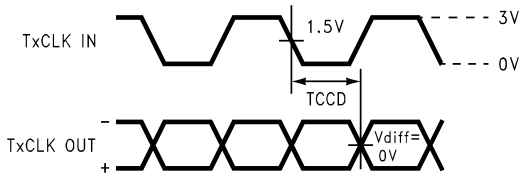


Figure 8. DS90CF363B (Transmitter) Clock In to Clock Out Delay (Falling Edge Strobe)

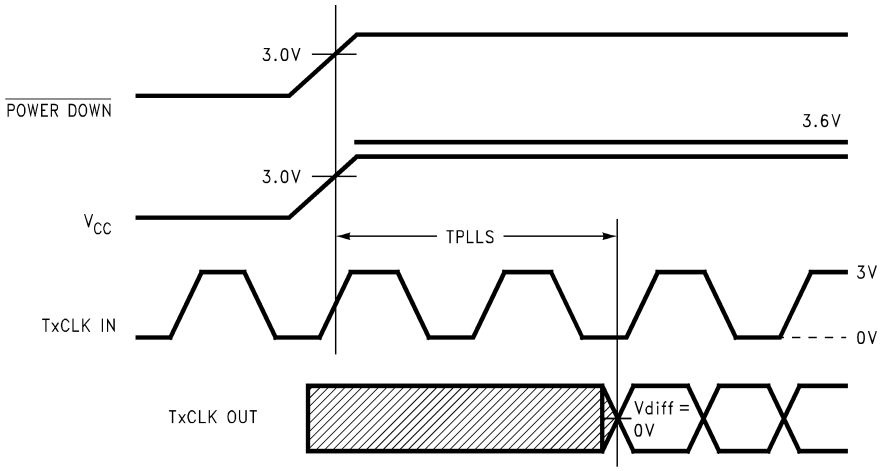


Figure 9. DS90CF363B (Transmitter) Phase Lock Loop Set Time

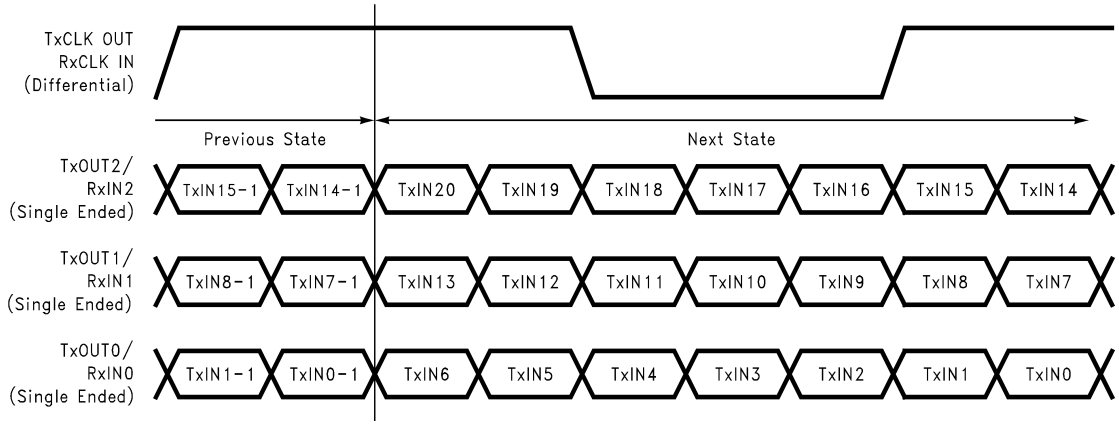


Figure 10. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs

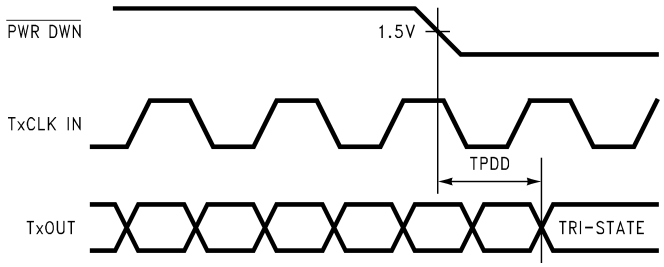


Figure 11. Transmitter Power Down Delay

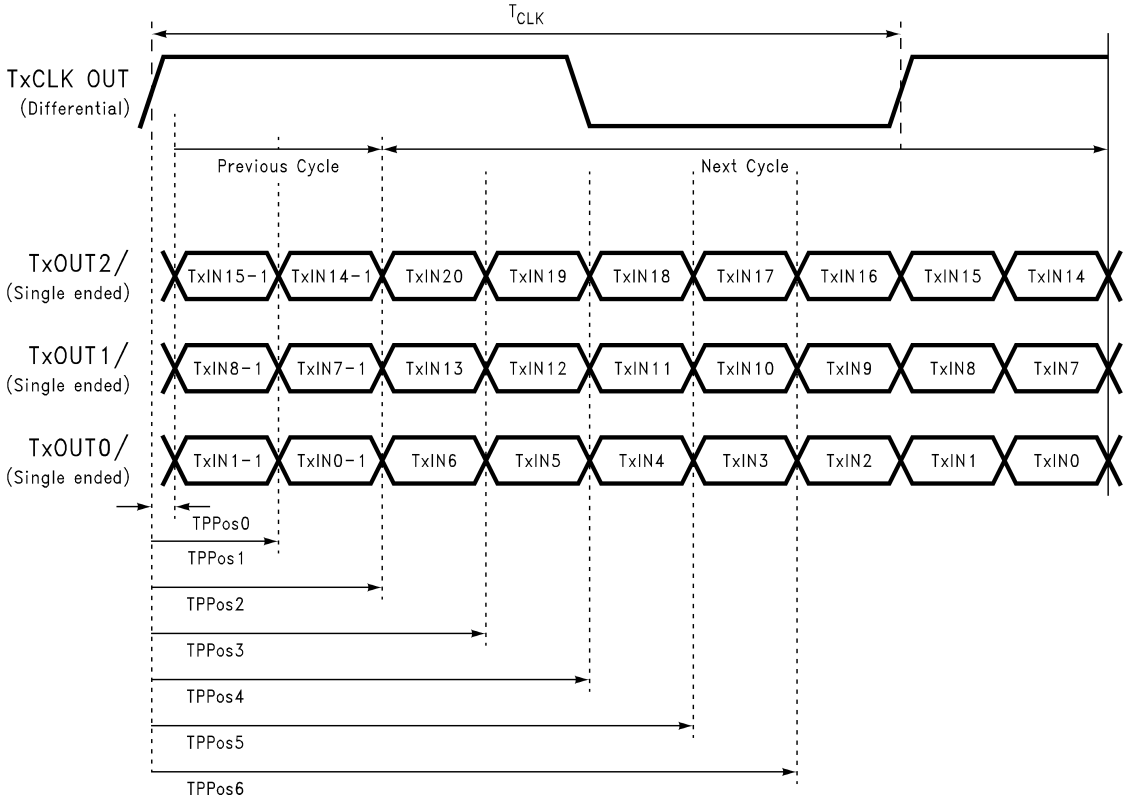


Figure 12. Transmitter LVDS Output Pulse Position Measurement

DS90CF363B PIN DESCRIPTIONS — FPD LINK TRANSMITTER

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME and DRDY (also referred to as HSYNC, VSYNC, Data Enable).
TxOUT+	O	3	Positive LVDS differential data output.
TxOUT−	O	3	Negative LVDS differential data output.
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. See Applications Information .
V_{CC}	I	4	Power supply pins for TTL inputs.
GND	I	4	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pin for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.
NC		1	No connect

APPLICATIONS INFORMATION

The DS90CF363B are backward compatible with the DS90C363/DS90CF363A and are a pin-for-pin replacement.

This device may also be used as a replacement for the DS90CF563 (5V, 65MHz) and DS90CF561 (5V, 40MHz) FPD-Link Transmitters with certain considerations/modifications:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of the transmitter.

TRANSMITTER INPUT PINS

The DS90CF363B transmitter input and control inputs accept 3.3V LVTTL/LVCMOS levels. They are not 5V tolerant.

TRANSMITTER INPUT CLOCK/DATA SEQUENCING

The DS90CF363B does not require any special requirement for sequencing of the input clock/data and PD (PowerDown) signal. The DS90CF363B offers a more robust input sequencing feature where the input clock/data can be inserted after the release of the PD signal. In the case where the clock/data is stopped and reapplied, such as changing video mode within Graphics Controller, it is not necessary to cycle the PD signal. However, there are in certain cases where the PD may need to be asserted during these mode changes. In cases where the source (Graphics Source) may be supplying an unstable clock or spurious noisy clock output to the LVDS transmitter, the LVDS Transmitter may attempt to lock onto this unstable clock signal but is unable to do so due the instability or quality of the clock source. The PD signal in these cases should then be asserted once a stable clock is applied to the LVDS transmitter. Asserting the $\overline{\text{PWR DOWN}}$ pin will effectively place the device in reset and disable the PLL, enabling the LVDS Transmitter into a power saving standby mode. However, it is still generally a good practice to assert the $\overline{\text{PWR DOWN}}$ pin or reset the LVDS transmitter whenever the clock/data is stopped and reapplied but it is not mandatory for the DS90CF363B.

SPREAD SPECTRUM CLOCK SUPPORT

The DS90CF363B can support Spread Spectrum Clocking signal type inputs. The DS90CF363B outputs will accurately track Spread Spectrum Clock/Data inputs with modulation frequencies of up to 100KHz (max.)with either center spread of ±2.5% or down spread -5% deviations.

POWER SOURCES SEQUENCE

In typical applications, it is recommended to have V_{CC}, LVDS V_{CC} and PLL V_{CC} from the same power source with three separate de-coupling bypass capacitor groups. There is no requirement on which VCC entering the device first.

Pin Diagram

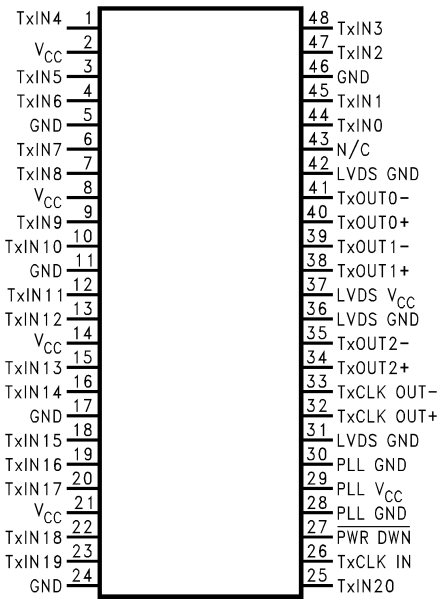
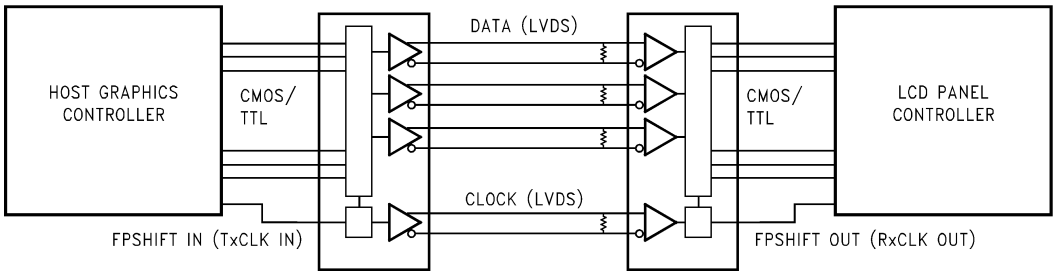


Figure 13.

Typical Application



REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CF363BMT/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF363BMT	Samples
DS90CF363BMTX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF363BMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

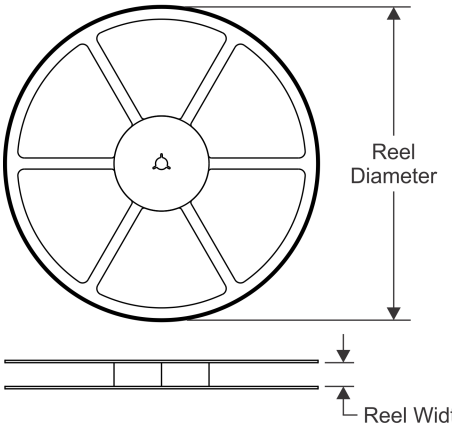
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

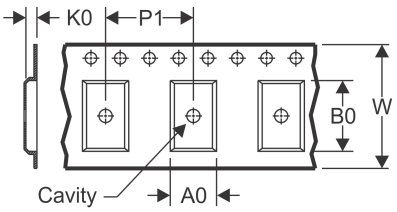
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

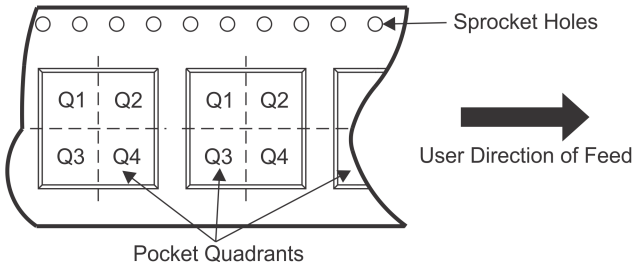


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

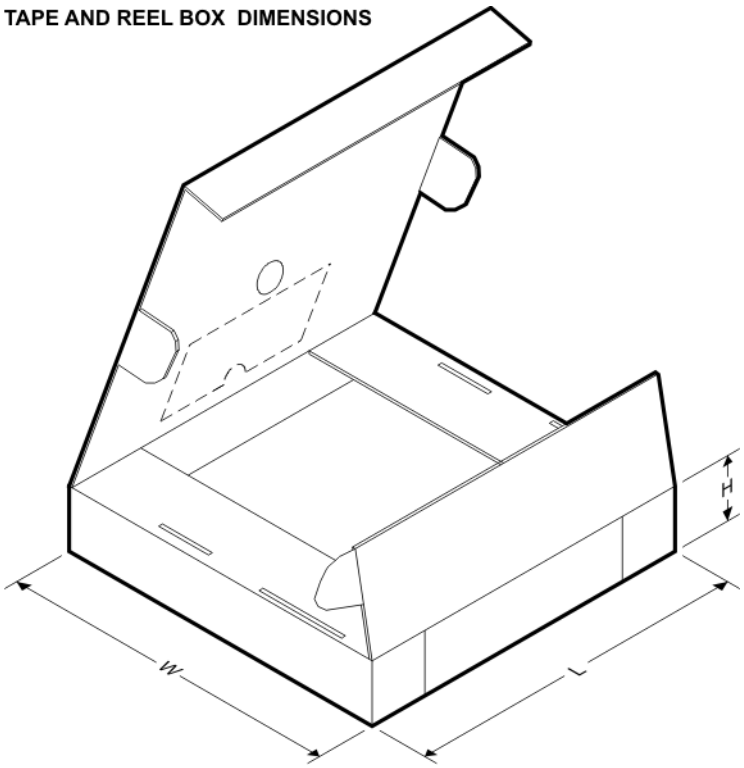
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CF363BMTX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

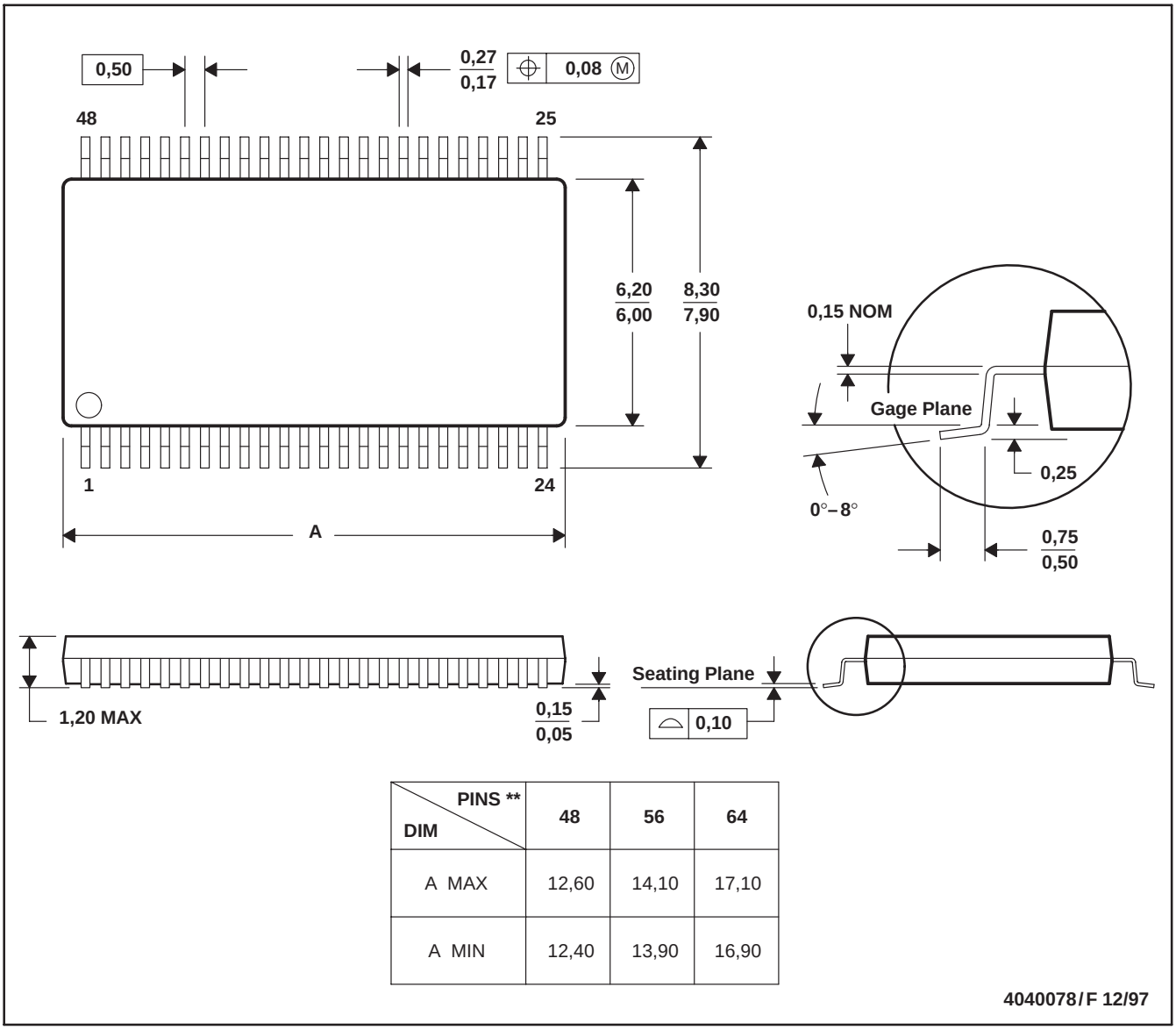


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CF363BMTX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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