

DS91D180/DS91C180 Multipoint LVDS (M-LVDS) Line Driver/Receiver

General Description

The DS91D180 and DS91C180 are high-speed differential M-LVDS single drivers/receivers designed for multipoint applications with multiple drivers or receivers. Multipoint LVDS (M-LVDS) is a new bus interface standard (TIA/EIA-899) based on LVDS but including several enhancements to improve multipoint performance. M-LVDS devices have superior drive capability and can support up to 32 loads. Along with increased drive, M-LVDS devices are required to have a controlled edge rate to minimize reflections and EMI. The 1 nSec minimum edge rate is tolerant of stub lengths up to 2 inches in length. M-LVDS devices also have a very large common mode range for additional noise margin in heavily loaded and noisy backplane environments.

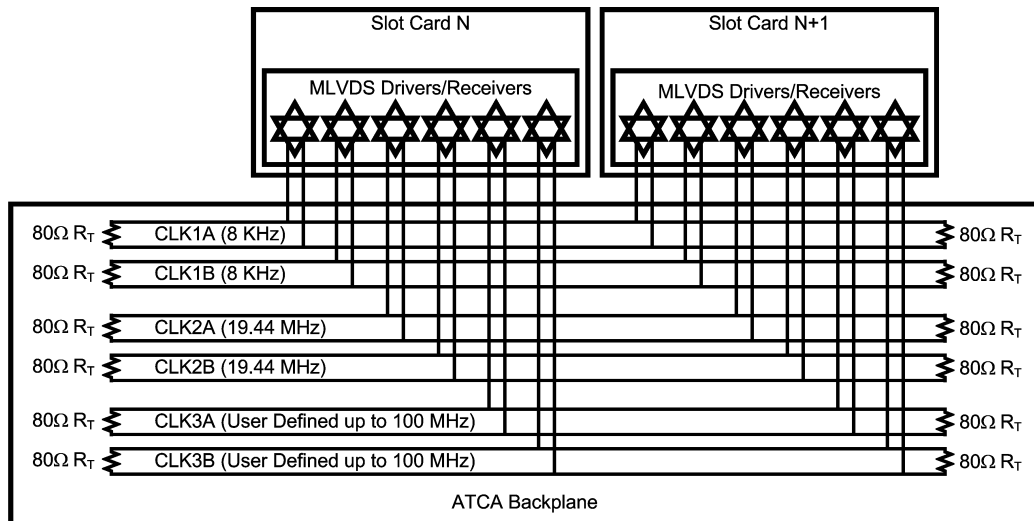
The DS91D180/DS91C180 driver input accepts LVTTTL/LVCMOS signals and converts them to differential M-LVDS signal levels. The DS91D180/DS91C180 receiver accepts low voltage differential signals (LVDS, B-LVDS, M-LVDS,

LV-PECL) and converts them to 3V LVCMOS signals. The DS91D180 has a M-LVDS type 1 receiver input with no offset. The DS91C180 receiver contains an M-LVDS "type 2" failsafe circuit with an internal 100 mV offset that provides a LOW output for both short and open input conditions.

Features

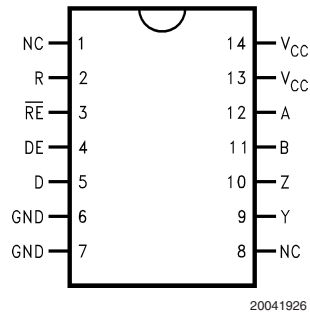
- Meets TIA/EIA-899 M-LVDS Standard
- Capable of driving 32 M-LVDS loads
- Controlled edge rates tolerant to stubs
- Wide Common Mode for Increased Noise Immunity
- DS91D180 has type 1 receiver input
- DS91C180 has type 2 Fail-safe support
- Up to 200 Mbps operation
- Industrial temperature range
- Single 3.3 V Supply
- 14L SOIC Package (JEDEC MS-012)

Typical Application in AdvancedTCA Clock Distribution



20041930

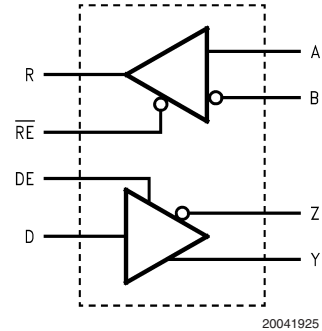
Connection Diagram



Top View

Order Number DS91D180TMA, DS91C180TMA
See NS Package Number M14A

Logic Diagram



Ordering Information

Order Number	Receiver Input	Function	Package Type
DS91D180TMA	type 1	Data (0V threshold receiver)	SOIC/M14A
DS91C180TMA	type 2	Control (offset fail-safe receiver)	SOIC/M14A

M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater than $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.

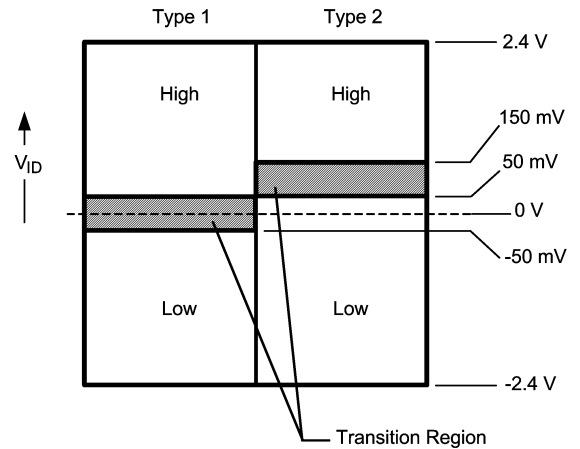


FIGURE 1. M-LVDS Receiver Input Thresholds

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	-0.3V to +4V
Control Input Voltages	-0.3V to ($V_{CC} + 0.3V$)
Driver Input Voltage	-0.3V to ($V_{CC} + 0.3V$)
Driver Output Voltages	-1.8V to +4.1V
Receiver Input Voltages	-1.8V to +4.1V
Receiver Output Voltage	-0.3V to ($V_{CC} + 0.3V$)
Maximum Package Power Dissipation at +25°C	
SOIC Package	1.1 W
Derate SOIC Package	8.8 mW/°C above +25°C
Thermal Resistance	
θ_{JA}	113.7 °C/W
θ_{JC}	36.9 °C/W
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
(Soldering, 4 seconds)	260°C

ESD Ratings:

(HBM 1.5k Ω , 100pF)	≥ 5 kV
(EIAJ 0 Ω , 200pF)	≥ 1000 V
(CDM 0 Ω , 0pF)	≥ 250 V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	-1.4		+3.8	V
Differential Input Voltage V_{ID}			2.4	V
High Level Input Voltage V_{IH}	2.0		V_{CC}	V
Low Level Input Voltage V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	-40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3, 4, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
M-LVDS Driver							
$ V_{YZ} $	Differential output voltage magnitude	$R_L = 50\Omega$, $C_L = 5pF$	480		650	mV	
ΔV_{YZ}	Change in differential output voltage magnitude between logic states	Figure 2 and Figure 4	-50	0	+50	mV	
$V_{OS(SS)}$	Steady-state common-mode output voltage	$R_L = 50\Omega$, $C_L = 5pF$	0.3	1.8	2.1	V	
$ \Delta V_{OS(SS)} $	Change in steady-state common-mode output voltage between logic states	Figure 2 and Figure 3	0		+50	mV	
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage	($V_{OS(PP)}$ @ 500KHz clock)		143		mV	
$V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	Figure 5	0		2.4	V	
$V_{Z(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V	
$V_{P(H)}$	Voltage overshoot, low-to-high level output	$R_L = 50\Omega$, $C_L = 5pF$, $C_D = 0.5pF$			1.2 V_{SS}	V	
$V_{P(L)}$	Voltage overshoot, high-to-low level output	Figure 7 and Figure 8 (Note 9)	-0.2 V_{SS}			V	
I_{IH}	High-level input current (LVTTTL inputs)	$V_{IH} = 2.0V$	-15		15	μA	
I_{IL}	Low-level input current (LVTTTL inputs)	$V_{IL} = 0.8V$	-15		15	μA	
V_{IKL}	Input Clamp Voltage (LVTTTL inputs)	$I_{IN} = -18$ mA	-1.5			V	
I_{OS}	Differential short-circuit output current	Figure 6	-43		43	mA	
M-LVDS Receiver							
V_{IT+}	Positive-going differential input voltage threshold	See Function Tables	Type 1		20	50	mV
			Type 2		94	150	mV
V_{IT-}	Negative-going differential input voltage threshold	See Function Tables	Type 1	-50	20		mV
			Type 2	50	94		mV
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	2.4	2.7		V	
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA		0.28	0.4	V	
I_{OZ}	TRI-STATE output current	$V_O = 0V$ or 3.6V	-10		10	μA	
I_{OSR}	Short circuit Receiver output current (LVTTTL Output)	$V_O = 0V$	-90	-48		mA	

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3, 4, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
M-LVDS Bus (Input and Output) Pins						
I_A, I_Y	Receiver input or driver high-impedance output current	$V_{A,Y} = 3.8V, V_{B,Z} = 1.2V,$ DE = GND			32	μA
		$V_{A,Y} = 0V \text{ or } 2.4V, V_{B,Z} = 1.2V,$ DE = GND	-20		+20	μA
		$V_{A,Y} = -1.4V, V_{B,Z} = 1.2V,$ DE = GND	-32			μA
I_B, I_Z	Receiver input or driver high-impedance output current	$V_{B,Z} = 3.8V, V_{A,Y} = 1.2V,$ DE = GND			32	μA
		$V_{B,Z} = 0V \text{ or } 2.4V, V_{A,Y} = 1.2V,$ DE = GND	-20		+20	μA
		$V_{B,Z} = -1.4V, V_{A,Y} = 1.2V,$ DE = GND	-32			μA
I_{AB}, I_{YZ}	Receiver input or driver high-impedance output differential current ($I_A - I_B$ or $I_Y - I_Z$)	$V_{A,Y} = V_{B,Z}, -1.4V \leq V \leq 3.8V,$ DE = GND	-4		+4	μA
$I_{A(OFF)}, I_{Y(OFF)}$	Receiver input or driver high-impedance output power-off current	$V_{A,Y} = 3.8V, V_{B,Z} = 1.2V,$ DE = $V_{CC} = 1.5V$			32	μA
		$V_{A,Y} = 0V \text{ or } 2.4V, V_{B,Z} = 1.2V,$ DE = $V_{CC} = 1.5V$	-20		+20	μA
		$V_{A,Y} = -1.4V, V_{B,Z} = 1.2V,$ DE = $V_{CC} = 1.5V$	-32			μA
$I_{B(OFF)}, I_{Z(OFF)}$	Receiver input or driver high-impedance output power-off current	$V_{B,Z} = 3.8V, V_{A,Y} = 1.2V,$ DE = $V_{CC} = 1.5V$			32	μA
		$V_{B,Z} = 0V \text{ or } 2.4V, V_{A,Y} = 1.2V,$ DE = $V_{CC} = 1.5V$	-20		+20	μA
		$V_{B,Z} = -1.4V, V_{A,Y} = 1.2V,$ DE = $V_{CC} = 1.5V$	-32			μA
$I_{AB(OFF)}, I_{YZ(OFF)}$	Receiver input or driver high-impedance output power-off differential current ($I_{A(OFF)} - I_{B(OFF)}$ or $I_{Y(OFF)} - I_{Z(OFF)}$)	$V_{A,Y} = V_{B,Z}, -1.4V \leq V \leq 3.8V,$ $V_{CC} = 1.5V, DE = 1.5V$	-4		+4	μA
C_A, C_B	Receiver input capacitance	$V_{CC} = \text{OPEN}$		5.1		pF
C_Y, C_Z	Driver output capacitance			8.5		pF
C_{AB}	Receiver input differential capacitance			2.5		pF
C_{YZ}	Driver output differential capacitance			5.5		pF
$C_{A/B}, C_{Y/Z}$	Receiver input or driver output capacitance balance (C_A/C_B or C_Y/C_Z)				1.0	
SUPPLY CURRENT (V_{CC})						
I_{CCD}	Driver Supply Current	$R_L = 50\Omega, DE = V_{CC}, \overline{RE} = V_{CC}$		17	29.5	mA
I_{CCZ}	TRI-STATE Supply Current	DE = GND, $\overline{RE} = V_{CC}$		7	9.0	mA
I_{CCR}	Receiver Supply Current	DE = GND, $\overline{RE} = \text{GND}$		14	18.5	mA
I_{CCB}	Supply Current, Driver and Receiver Enabled	DE = $V_{CC}, \overline{RE} = \text{GND}$		20	29.5	mA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 3, 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AC SPECIFICATION						
t_{PLH}	Differential Propagation Delay Low to High	$R_L = 50\Omega$, $C_L = 5\text{ pF}$, $C_D = 0.5\text{ pF}$ <i>Figure 7 and Figure 8</i>	1.0	3.4	5.5	ns
t_{PHL}	Differential Propagation Delay High to Low		1.0	3.1	5.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $ t_{PLHD} - t_{PHLD} $ (Notes 5, 9)			300	420	ps
t_{SKD3}	Part-to-Part Skew (Notes 6, 9)				1.9	ns
t_{TLH} (t_r)	Rise Time (Note 9)		1.0	1.8	3.0	ns
t_{THL} (t_f)	Fall Time (Note 9)		1.0	1.8	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	$R_L = 50\Omega$, $C_L = 5\text{ pF}$, $C_D = 0.5\text{ pF}$ <i>Figure 9 and Figure 10</i>			8	ns
t_{PZL}	Enable Time (Z to Active Low)				8	ns
t_{PLZ}	Disable Time (Active Low to Z)				8	ns
t_{PHZ}	Disable Time (Active High to Z)				8	ns
t_{JIT}	Random Jitter, RJ (Note 9)		100MHz clock pattern (Note 7)		2.5	5.5
f_{MAX}	Maximum Data Rate		200			Mbps
RECEIVER AC SPECIFICATION						
t_{PLH}	Propagation Delay Low to High	$C_L = 15\text{ pF}$ <i>Figures 11, 12 and Figure 13</i>	2.0	4.7	7.5	ns
t_{PHL}	Propagation Delay High to Low		2.0	5.3	7.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $ t_{PLHD} - t_{PHLD} $ (Notes 5, 9)			0.6	1.9	ns
t_{SKD3}	Part-to-Part Skew (Notes 6, 9)				1.5	ns
t_{TLH} (t_r)	Rise Time (Note 9)		0.5	1.2	3.0	ns
t_{THL} (t_f)	Fall Time (Note 9)		0.5	1.2	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	$R_L = 500\Omega$, $C_L = 15\text{ pF}$ <i>Figure 14 and Figure 15</i>			10	ns
t_{PZL}	Enable Time (Z to Active Low)				10	ns
t_{PLZ}	Disable Time (Active Low to Z)				10	ns
t_{PHZ}	Disable Time (Active High to Z)				10	ns
f_{MAX}	Maximum Data Rate			200		

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 3.3V$ and $T_A = 25^\circ C$.

Note 4: The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this datasheet.

Note 5: t_{SKD1} , $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

Note 6: t_{SKD3} , Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within $5^\circ C$ of each other within the operating temperature range.

Note 7: Stimulus and fixture jitter has been subtracted.

Note 8: C_L includes fixture capacitance and C_D includes probe capacitance.

Note 9: Not production tested. Guaranteed by a statistical analysis on a sample basis at the time of characterization.

Test Circuits and Waveforms

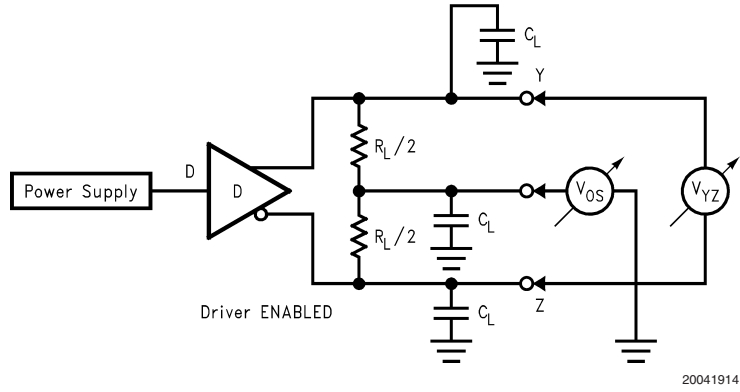


FIGURE 2. Differential Driver Test Circuit

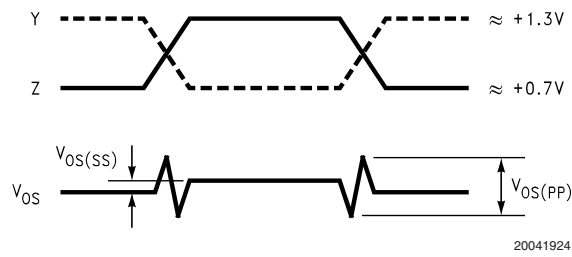


FIGURE 3. Differential Driver Waveforms

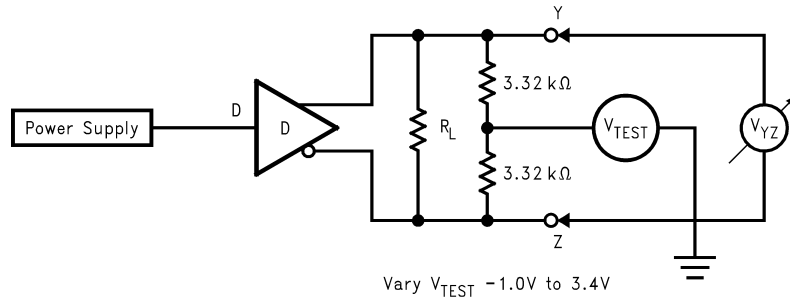


FIGURE 4. Differential Driver Full Load Test Circuit

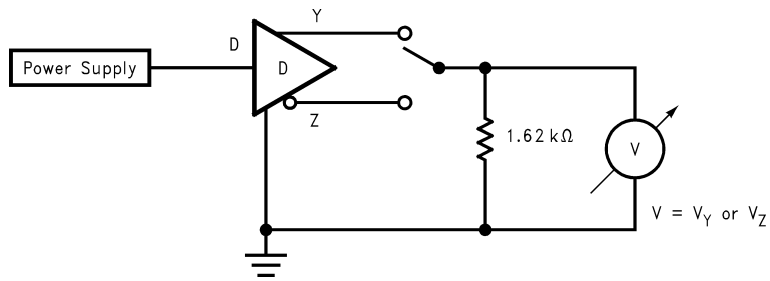
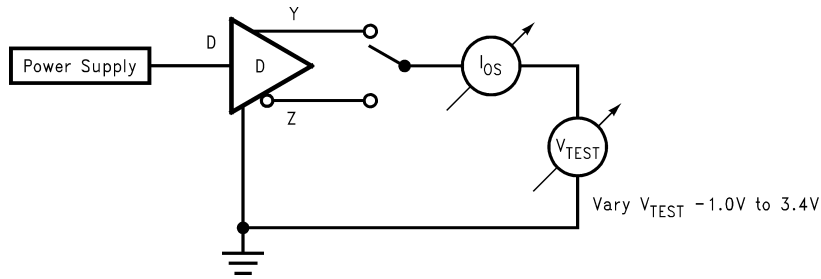


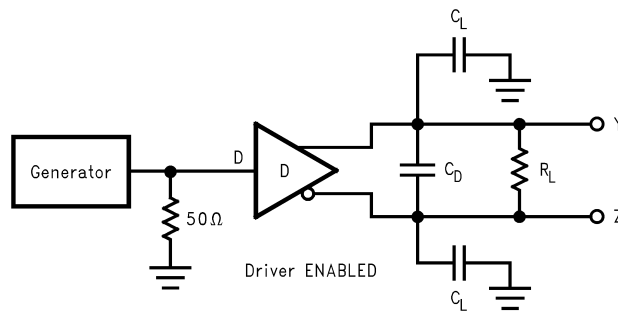
FIGURE 5. Differential Driver DC Open Test Circuit

Test Circuits and Waveforms (Continued)



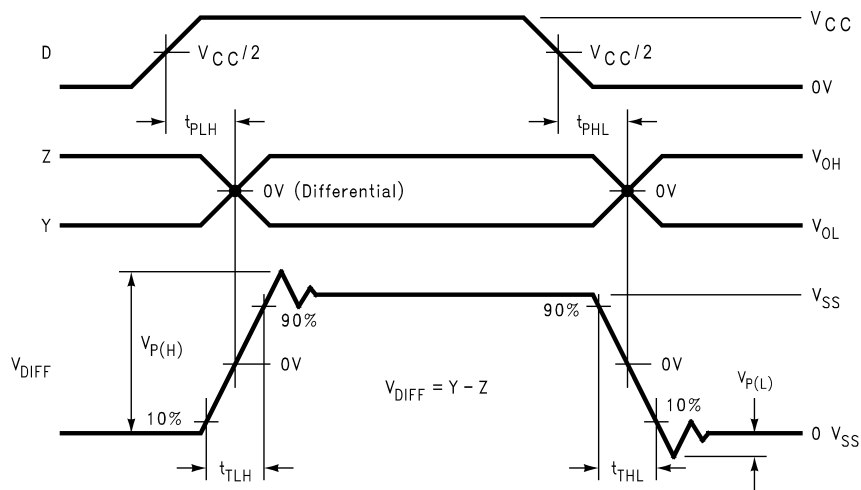
20041927

FIGURE 6. Differential Driver Short-Circuit Test Circuit



20041916

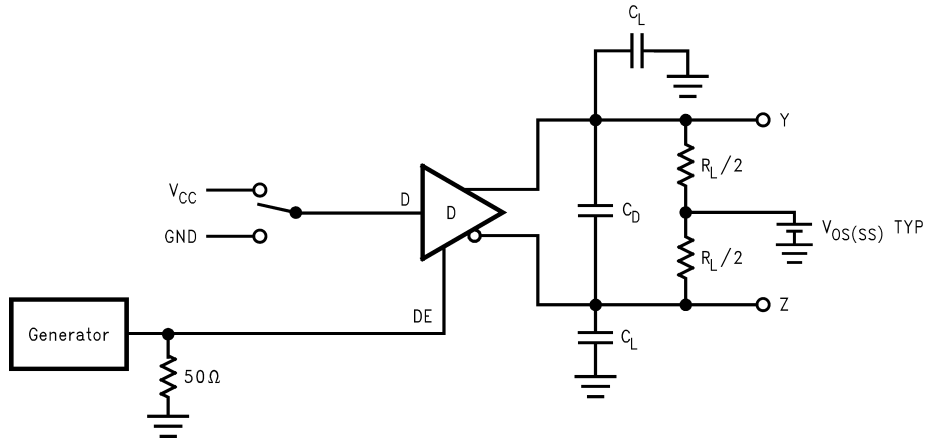
FIGURE 7. Driver Propagation Delay and Transition Time Test Circuit



20041918

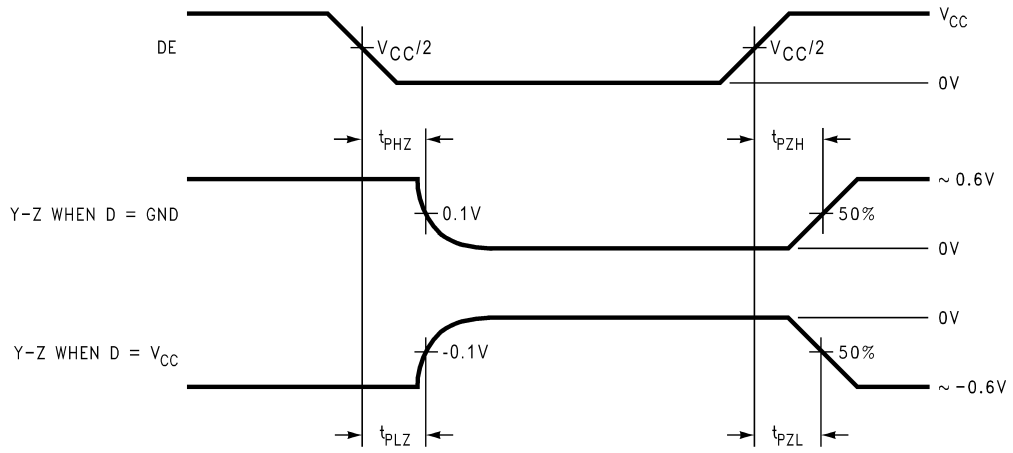
FIGURE 8. Driver Propagation Delays and Transition Time Waveforms

Test Circuits and Waveforms (Continued)



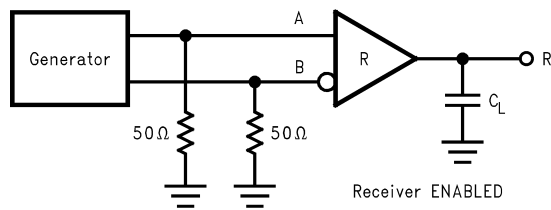
20041919

FIGURE 9. Driver TRI-STATE Delay Test Circuit



20041921

FIGURE 10. Driver TRI-STATE Delay Waveforms



20041915

FIGURE 11. Receiver Propagation Delay and Transition Time Test Circuit

Test Circuits and Waveforms (Continued)

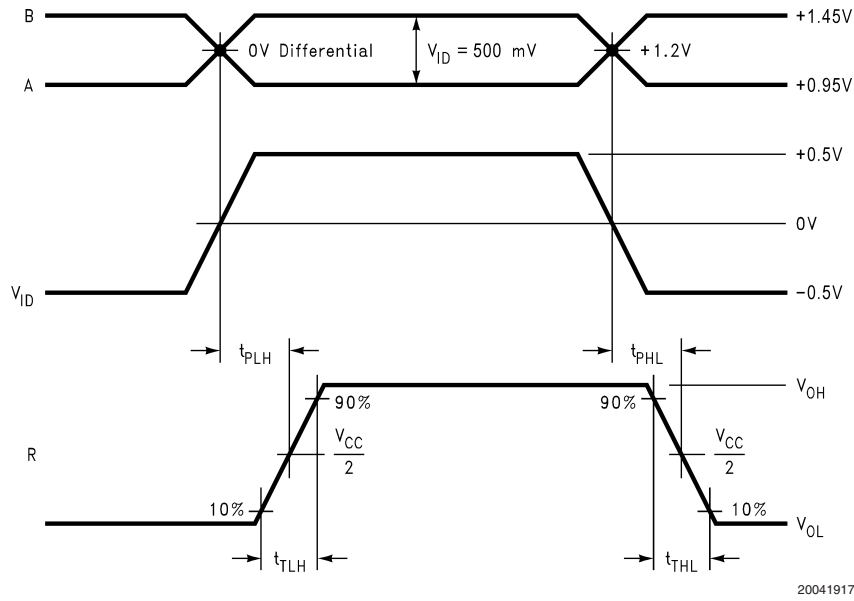


FIGURE 12. Type 1 Receiver Propagation Delay and Transition Time Waveforms

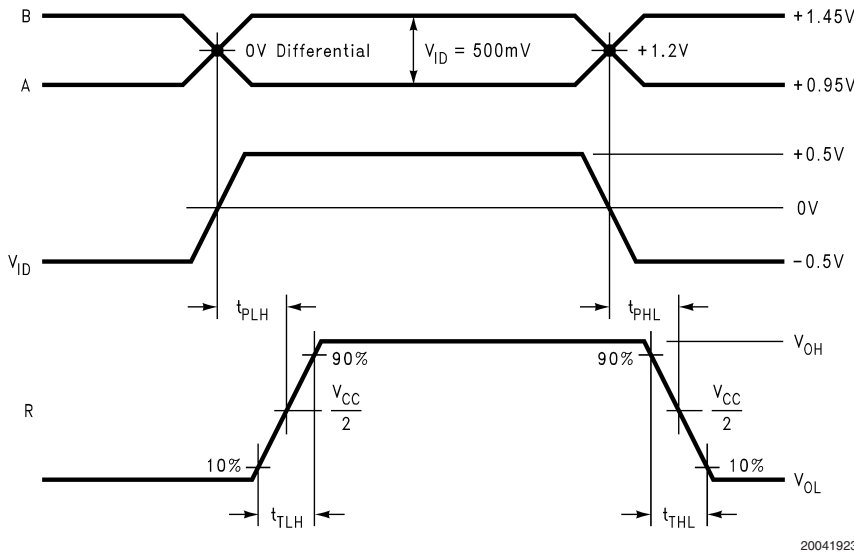


FIGURE 13. Type 2 Receiver Propagation Delay and Transition Time Waveforms

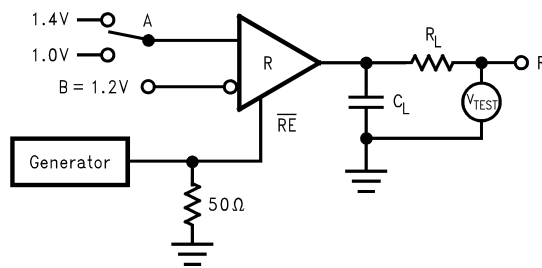


FIGURE 14. Receiver TRI-STATE Delay Test Circuit

Test Circuits and Waveforms (Continued)

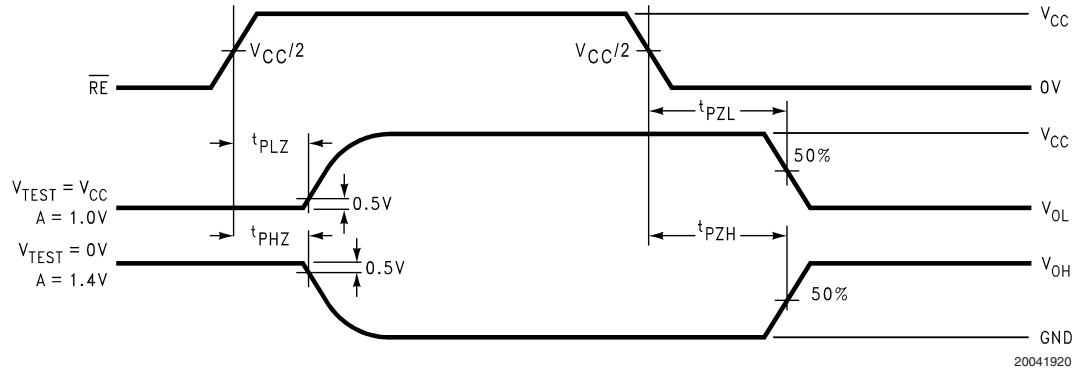


FIGURE 15. Receiver TRI-STATE Delay Waveforms

Function Tables

DS91D180/DS91C180 Transmitting

Inputs		Outputs	
DE	D	Z	Y
2.0V	2.0V	L	H
2.0V	0.8V	H	L
0.8V	X	Z	Z

X — Don't care condition
Z — High impedance state

DS91D180 Receiving

Inputs		Output
\overline{RE}	A - B	R
0.8V	$\geq +0.05V$	H
0.8V	$\leq -0.05V$	L
0.8V	0V	X
2.0V	X	Z

X — Don't care condition
Z — High impedance state

DS91C180 Receiving

Inputs		Output
\overline{RE}	A - B	R
0.8V	$\geq +0.15V$	H
0.8V	$\leq +0.05V$	L
0.8V	0V	L
2.0V	X	Z

X — Don't care condition
Z — High impedance state

DS91D180 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	-2.400V	1.200V	L
3.800V	3.750V	0.050V	3.775V	H
3.750V	3.800V	-0.050V	3.775V	L
-1.400V	-1.350V	-0.050V	-1.375V	H
-1.350V	-1.400V	0.050V	-1.375V	L

H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE} = L$)

DS91C180 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V_{IA}	V_{IB}	V_{ID}	V_{IC}	R
2.400V	0.000V	2.400V	1.200V	H
0.000V	2.400V	-2.400V	1.200V	L
3.800V	3.650V	0.150V	3.725V	H
3.800V	3.750V	0.050V	3.775V	L
-1.250V	-1.400V	0.150V	-1.325V	H
-1.350V	-1.400V	0.050V	-1.375V	L

H — High Level
L — Low Level
Output state assumes that the receiver is enabled ($\overline{RE} = L$)

Pin Descriptions

Pin No.	Name	Description
1, 8	NC	No connect.
2	R	Receiver output pin
3	\overline{RE}	Receiver enable pin: When \overline{RE} is high, the receiver is disabled. When \overline{RE} is low or open, the receiver is enabled.
4	DE	Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled.
5	D	Driver input pin
6, 7	GND	Ground pin
9	Y	Non-inverting driver output pin
10	Z	Inverting driver output pin
11	B	Inverting receiver input pin
12	A	Non-inverting receiver input pin
13, 14	V_{CC}	Power supply pin, +3.3V \pm 0.3V

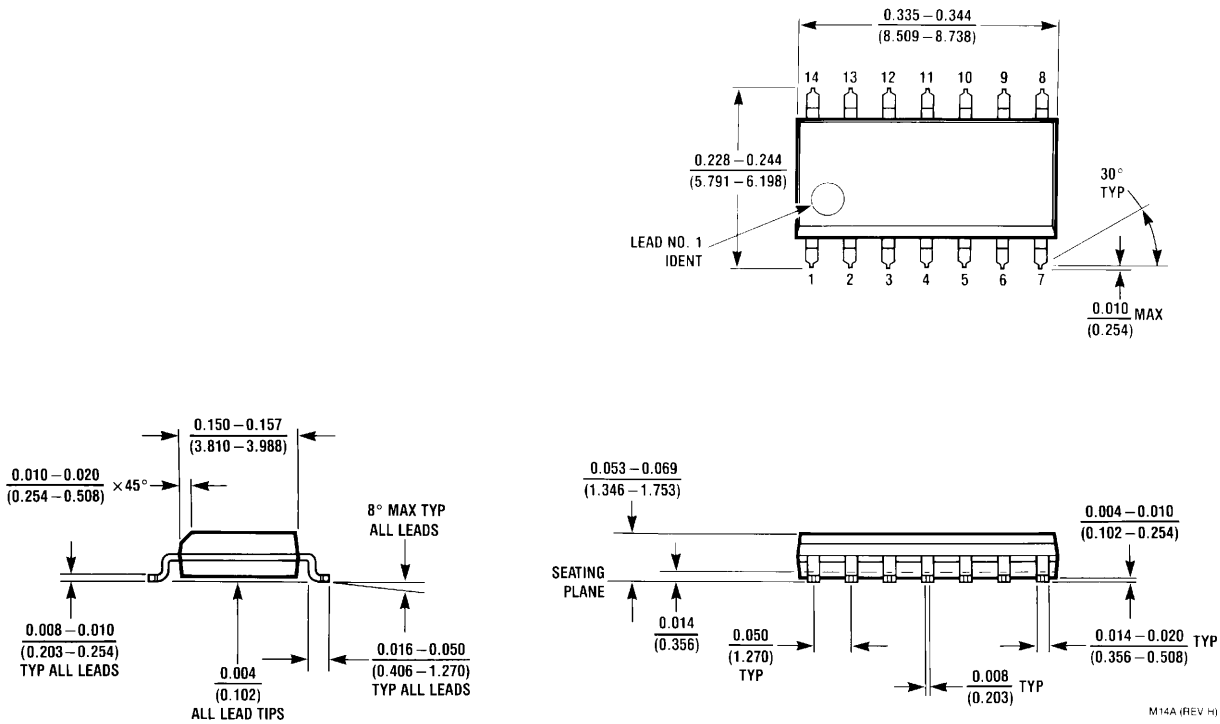
Application Information

STUB LENGTH

Stub lengths should be kept to a minimum. The typical transition time of the DS91D180/DS91C180 driver output is 1.8 ns (10% to 90%). The 100% time is 1.8 ns/0.8 or 2.25 ns. For a general approximation, if the electrical length of a trace is greater than 1/5 of the transition edge, then the trace is considered a transmission line. For example, 2.25 ns/5 is

450ps. If the velocity equals 160 ps per inch for a typical loaded backplane, then the maximum stub length is 450 ps/160 ps/inch or 2.8 inches (approximately 3 inches). To determine the maximum stub for your backplane, the propagation velocity for the backplane is required (refer to application notes AN-905 and AN-808).

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number DS91D180TMA, DS91C180TMA
See NS package Number M14A

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.
For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor follows the provisions of the Product Stewardship Guide for Customers (CSP-9-111C2) and Banned Substances and Materials of Interest Specification (CSP-9-111S2) for regulatory environmental compliance. Details may be found at: www.national.com/quality/green.

Lead free products are RoHS compliant.



National Semiconductor
Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560