

Bus LVDS 3.3/5.0V Single Transceiver

General Description

The DS92LV010AEP is one in a series of transceivers designed specifically for the high speed, low power proprietary bus backplane interfaces. The device operates from a single 3.3V or 5.0V power supply and includes one differential line driver and one receiver. To minimize bus loading the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility as 4 separate lines are provided (DIN, DE, RE, and ROUT). The device also features flow through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10 mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27 Ohms.

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of $\pm 1V$.

The receiver threshold is $\pm 100mV$ over a $\pm 1V$ common mode range and translates the low voltage differential levels to standard (CMOS/TTL) levels.

ENHANCED PLASTIC

- Extended Temperature Performance of $-40^{\circ}C$ to $+85^{\circ}C$
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard
- Enhanced Diminishing Manufacturing Sources (DMS) Support

Features

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Balanced Output Impedance
- Lite Bus Loading 5pF typical
- Glitch free power up/down (Driver disabled)
- 3.3V or 5.0V Operation
- $\pm 1V$ Common Mode Range
- $\pm 100mV$ Receiver Sensitivity
- High Signaling Rate Capability (above 100 Mbps)
- Low Power CMOS design
- Product offered in 8 lead SOIC package

Applications

- Selected Military Applications
- Selected Avionics Applications

Ordering Information

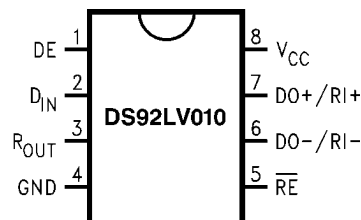
PART NUMBER	VID PART NUMBER	NS PACKAGE NUMBER (Note 3)
DS92LV010ATMEP	V62,04740-01	M08A
(Notes 1, 2)	TBD	TBD

Note 1: For the following (Enhanced Plastic) version, check for availability: - DS92LV010ATMXEP Parts listed with an "X" are provided in Tape & Reel and parts without an "X" are in Rails.

Note 2: FOR ADDITIONAL ORDERING AND PRODUCT INFORMATION, PLEASE VISIT THE ENHANCED PLASTIC WEB SITE AT: www.national.com/mil

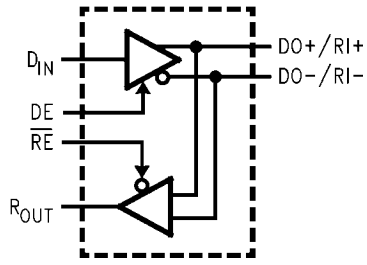
Note 3: Refer to package details under Physical Dimensions

Connection Diagram



See NS Package Number **M08A**

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Absolute Maximum Ratings (Notes 4, 5)

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If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.0V
Enable Input Voltage (DE, \overline{RE})	-0.3V to ($V_{CC} + 0.3V$)
Driver Input Voltage (DIN)	-0.3V to ($V_{CC} + 0.3V$)
Receiver Output Voltage (R_{OUT})	-0.3V to ($V_{CC} + 0.3V$)
Bus Pin Voltage (DO/RI \pm)	-0.3V to +3.9V
Driver Short Circuit Current	Continuous
ESD (HBM 1.5 k Ω , 100 pF)	>2.0 kV
Maximum Package Power Dissipation at 25°C	
SOIC	1025 mW

Derate SOIC Package	8.2 mW/°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}), or	3.0	3.6	V
Supply Voltage (V_{CC})	4.5	5.5	V
Receiver Input Voltage	0.0	2.9	V
Operating Free Air Temperature	-40	+85	°C

DC Electrical Characteristics (Notes 5, 6, 12)

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted, $V_{CC} = 3.3V \pm 0.3V$

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units	
V_{OD}	Output Differential Voltage	$R_L = 27\Omega$, Figure 1	DO+/RI+, DO-/RI-	140	250	360	mV	
ΔV_{OD}	V_{OD} Magnitude Change				3	30	mV	
V_{OS}	Offset Voltage			1	1.25	1.65	V	
ΔV_{OS}	Offset Magnitude Change				5	50	mV	
I_{OSD}	Output Short Circuit Current	$V_O = 0V$, $DE = V_{CC}$			-12	-20	mA	
V_{OH}	Voltage Output High	$V_{ID} = +100\text{ mV}$	R_{OUT}				V	
		Inputs Open						$I_{OH} = -400\ \mu\text{A}$
		Inputs Shorted						
		Inputs Terminated, $R_L = 27\Omega$						
V_{OL}	Voltage Output Low	$I_{OL} = 2.0\text{ mA}$, $V_{ID} = -100\text{ mV}$			0.1	0.4	V	
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$, $V_{ID} = +100\text{ mV}$		-5	-35	-85	mA	
V_{TH}	Input Threshold High	$DE = 0V$	DO+/RI+, DO-/RI-			+100	mV	
V_{TL}	Input Threshold Low			-100			mV	
I_{IN}	Input Current	$DE = 0V$, $V_{IN} = +2.4V$, or $0V$		-20	± 1	+20	μA	
		$V_{CC} = 0V$, $V_{IN} = +2.4V$, or $0V$		-20	± 1	+20	μA	
V_{IH}	Minimum Input High Voltage		DIN, DE, RE	2.0		V_{CC}	V	
V_{IL}	Maximum Input Low Voltage			GND		0.8	V	
I_{IH}	Input High Current	$V_{IN} = V_{CC}$ or $2.4V$				± 1	± 10	μA
I_{IL}	Input Low Current	$V_{IN} = \text{GND}$ or $0.4V$				± 1	± 10	μA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -18\text{ mA}$		-1.5	-0.8		V	
I_{CCD}	Power Supply Current	$DE = \overline{RE} = V_{CC}$, $R_L = 27\Omega$	V_{CC}		13	20	mA	
I_{CCR}		$DE = \overline{RE} = 0V$			5	8	mA	
I_{CCZ}		$DE = 0V$, $\overline{RE} = V_{CC}$			3	7.5	mA	
I_{CC}		$DE = V_{CC}$, $\overline{RE} = 0V$, $R_L = 27\Omega$			16	22	mA	
C_{output}	Capacitance @ BUS Pins		DO+/RI+, DO-/RI-		5		pF	

DC Electrical Characteristics (Notes 5, 6, 12)

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted, $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	$R_L = 27\Omega$, Figure 1	DO+/RI+, DO-/RI-	145	270	390	mV
ΔV_{OD}	V_{OD} Magnitude Change				3	30	mV
V_{OS}	Offset Voltage			1	1.35	1.65	V
ΔV_{OS}	Offset Magnitude Change				5	50	mV
I_{OSD}	Output Short Circuit Current	$V_O = 0\text{V}$, $DE = V_{CC}$		-12	-20	mA	
V_{OH}	Voltage Output High	$V_{ID} = +100\text{ mV}$	R_{OUT}	4.3	5.0		V
		Inputs Open					
		Inputs Shorted					
		Inputs Terminated, $R_L = 27\Omega$					
V_{OL}	Voltage Output Low	$I_{OL} = 2.0\text{ mA}$, $V_{ID} = -100\text{ mV}$			0.1	0.4	V
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0\text{V}$, $V_{ID} = +100\text{ mV}$		-35	-90	-130	mA
V_{TH}	Input Threshold High	$DE = 0\text{V}$	DO+/RI+, DO-/RI-			+100	mV
V_{TL}	Input Threshold Low			-100			mV
I_{IN}	Input Current	$DE = 0\text{V}$, $V_{IN} = +2.4\text{V}$, or 0V		-20	± 1	+20	μA
		$V_{CC} = 0\text{V}$, $V_{IN} = +2.4\text{V}$, or 0V		-20	± 1	+20	μA
V_{IH}	Minimum Input High Voltage		DIN, DE, RE	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{CC}$ or 2.4V			± 1	± 10	μA
I_{IL}	Input Low Current	$V_{IN} = \text{GND}$ or 0.4V			± 1	± 10	μA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -18\text{ mA}$		-1.5	-0.8		V
I_{CCD}	Power Supply Current	$DE = \overline{RE} = V_{CC}$, $R_L = 27\Omega$	V_{CC}		17	25	mA
I_{CCR}		$DE = \overline{RE} = 0\text{V}$			6	10	mA
I_{CCZ}		$DE = 0\text{V}$, $\overline{RE} = V_{CC}$			3	8	mA
I_{CC}		$DE = V_{CC}$, $\overline{RE} = 0\text{V}$, $R_L = 27\Omega$			20	25	mA
C_{output}	Capacitance @ BUS Pins		DO+/RI+, DO-/RI-		5		pF

AC Electrical Characteristics (Notes 9, 12)

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	$R_L = 27\Omega$, Figures 2, 3 $C_L = 10\text{ pF}$	1.0	3.0	5.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		1.0	2.8	5.0	ns
t_{SKD}	Differential SKEW $ t_{PHLD} - t_{PLHD} $			0.2	1.0	ns
t_{TLH}	Transition Time Low to High			0.3	2.0	ns
t_{THL}	Transition Time High to Low			0.3	2.0	ns
t_{PHZ}	Disable Time High to Z	$R_L = 27\Omega$, Figures 4, 5 $C_L = 10\text{ pF}$	0.5	4.5	9.0	ns
t_{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t_{PZH}	Enable Time Z to High		2.0	5.0	7.0	ns
t_{PZL}	Enable Time Z to Low		1.0	4.5	9.0	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Prop. Delay High to Low	<i>Figures 6, 7</i> $C_L = 10 \text{ pF}$	2.5	5.0	12.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		2.5	5.5	10.0	ns
t_{SKD}	Differential SKEW $ t_{PHLD} - t_{PLHD} $			0.5	2.0	ns
t_r	Rise Time			1.5	4.0	ns
t_f	Fall Time			1.5	4.0	ns
t_{PHZ}	Disable Time High to Z	$R_L = 500\Omega$, <i>Figures 8, 9</i> $C_L = 10 \text{ pF}$ (Note 11)	2.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		2.0	5.0	7.0	ns
t_{PZH}	Enable Time Z to High		2.0	7.0	13.0	ns
t_{PZL}	Enable Time Z to Low		2.0	6.0	10.0	ns

AC Electrical Characteristics (Notes 9, 12)

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	$R_L = 27\Omega$, <i>Figures 2, 3</i> $C_L = 10 \text{ pF}$	0.5	2.7	4.5	ns
t_{PLHD}	Differential Prop. Delay Low to High		0.5	2.5	4.5	ns
t_{SKD}	Differential SKEW $ t_{PHLD} - t_{PLHD} $			0.2	1.0	ns
t_{TLH}	Transition Time Low to High			0.3	2.0	ns
t_{THL}	Transition Time High to Low			0.3	2.0	ns
t_{PHZ}	Disable Time High to Z	$R_L = 27\Omega$, <i>Figures 4, 5</i> $C_L = 10 \text{ pF}$	0.5	3.0	7.0	ns
t_{PLZ}	Disable Time Low to Z		0.5	5.0	10.0	ns
t_{PZH}	Enable Time Z to High		2.0	4.0	7.0	ns
t_{PZL}	Enable Time Z to Low		1.0	4.0	9.0	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low	<i>Figures 6, 7</i> $C_L = 10 \text{ pF}$	2.5	5.0	12.0	ns
t_{PLHD}	Differential Prop. Delay Low to High		2.5	4.6	10.0	ns
t_{SKD}	Differential SKEW $ t_{PHLD} - t_{PLHD} $			0.4	2.0	ns
t_r	Rise Time			1.2	2.5	ns
t_f	Fall Time			1.2	2.5	ns
t_{PHZ}	Disable Time High to Z	$R_L = 500\Omega$, <i>Figures 8, 9</i> $C_L = 10 \text{ pF}$ (Note 11)	2.0	4.0	6.0	ns
t_{PLZ}	Disable Time Low to Z		2.0	4.0	6.0	ns
t_{PZH}	Enable Time Z to High		2.0	5.0	9.0	ns
t_{PZL}	Enable Time Z to Low		2.0	5.0	7.0	ns

Electrical Characteristics

Note 4: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 5: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground except V_{OD} , V_{ID} , V_{TH} and V_{TL} unless otherwise specified.

Note 6: All typicals are given for $V_{CC} = +3.3V$ or $5.0V$ and $T_A = +25^\circ C$, unless otherwise stated.

Note 7: ESD Rating: HBM (1.5 k Ω , 100 pF) > 2.0 kV EAT (0 Ω , 200 pF) > 300V.

Note 8: C_L includes probe and fixture capacitance.

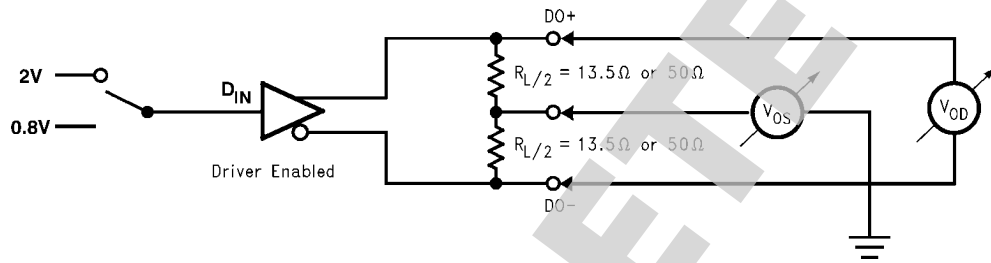
Note 9: Generator waveforms for all tests unless otherwise specified: $f = 1MHz$, $Z_O = 50\Omega$, $t_r, t_f \leq 6.0ns$ (0%–100%) on control pins and $\leq 1.0ns$ for RI inputs.

Note 10: The DS92LV010AEP is a current mode device and only function with datasheet specification when a resistive load is applied between the driver outputs.

Note 11: For receiver TRI-STATE[®] delays, the switch is set to V_{CC} for t_{PZL} and t_{PLZ} and to GND for t_{PZH} and t_{PHZ} .

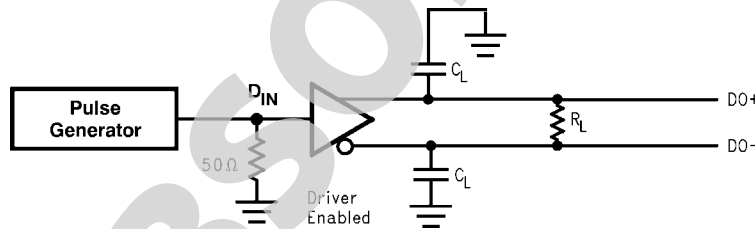
Note 12: "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."

Test Circuits and Timing Waveforms



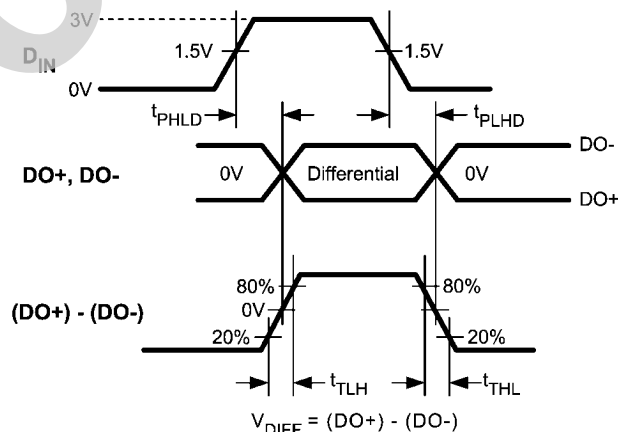
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FIGURE 1. Differential Driver DC Test Circuit



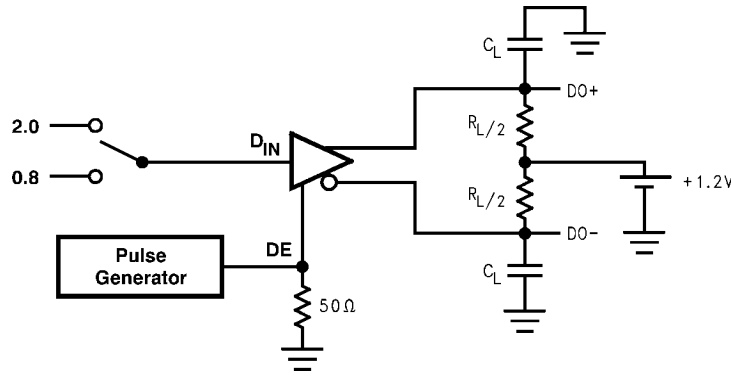
20119304

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit



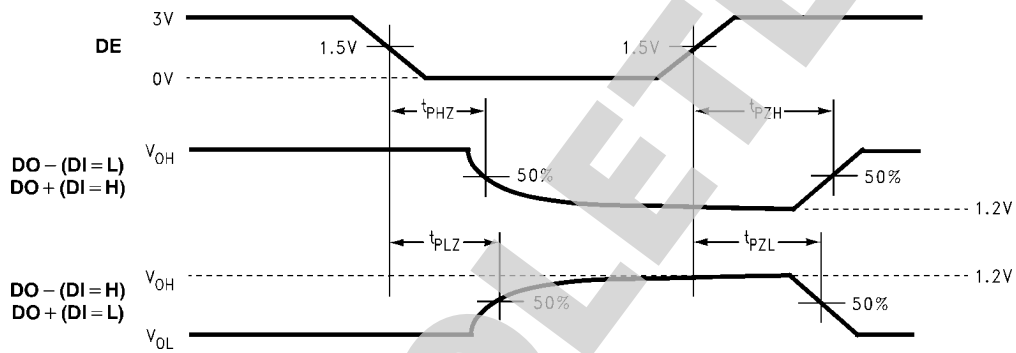
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FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms



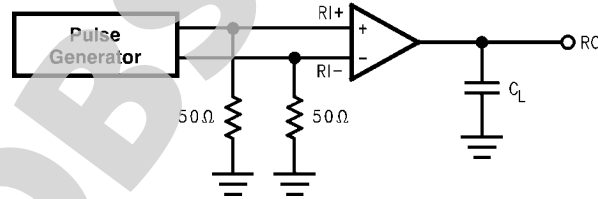
20119306

FIGURE 4. Driver TRI-STATE Delay Test Circuit



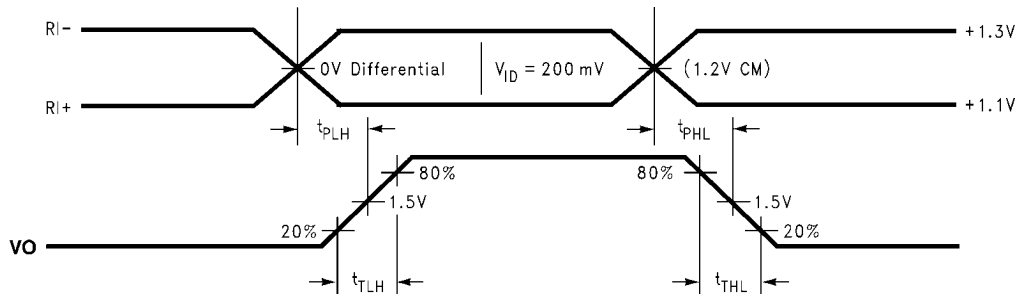
20119307

FIGURE 5. Driver TRI-STATE Delay Waveforms



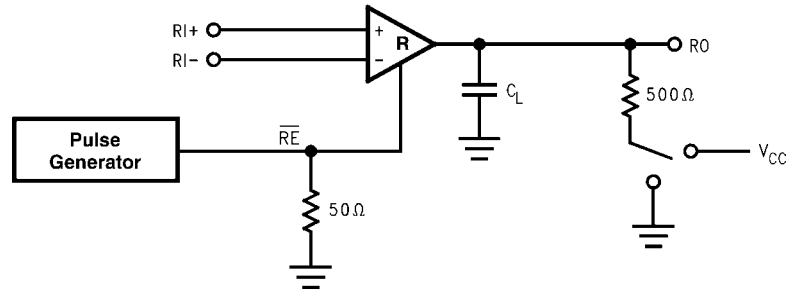
20119308

FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit



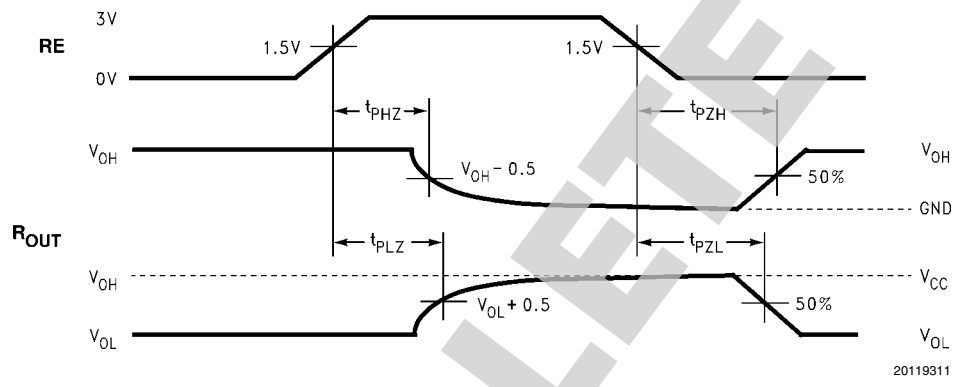
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FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms



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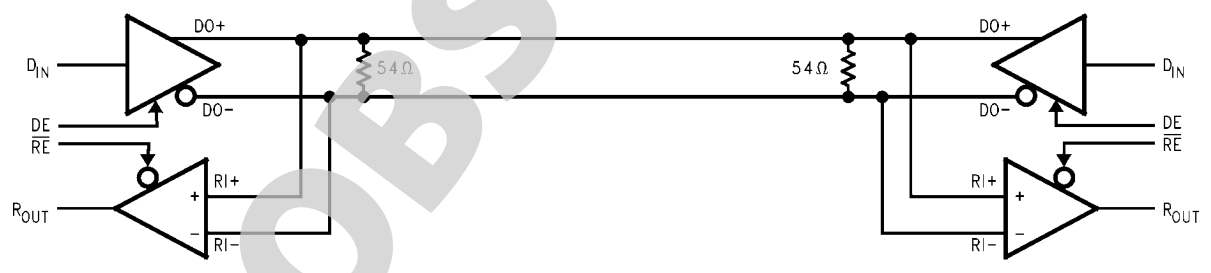
FIGURE 8. Receiver TRI-STATE Delay Test Circuit



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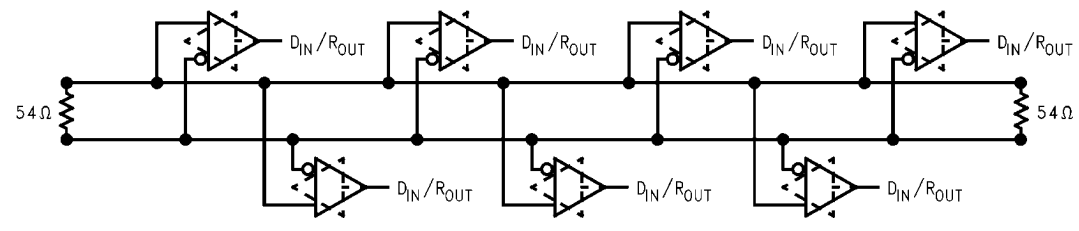
FIGURE 9. Receiver TRI-STATE Delay Waveforms

Typical Bus Application Configurations



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Bi-Directional Half-Duplex Point-to-Point Applications



20119313

Multi-Point Bus Applications

Application Information

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There are a few common practices which should be implied when designing PCB for BLVDS signaling. Recommended practices are:

- Use at least 4 layer PCB board (BLVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (BLVDS port side) connector as possible.
- Bypass each BLVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to

power and ground pins work best. Two or three multi-layer ceramic (MLC) surface mount capacitors (0.1 μF , and 0.01 μF in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin.

- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused LVDS receiver inputs open (floating)

TABLE 1. Functional Table

MODE SELECTED	DE	$\overline{\text{RE}}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
LOOP BACK MODE	H	L

TABLE 2. Transmitter Mode

INPUTS		OUTPUTS	
DE	DI	DO+	DO-
H	L	L	H
H	H	H	L
H	$2 > \& > 0.8$	X	X
L	X	Z	Z

L = Low state
H = High state

TABLE 3. Receiver Mode

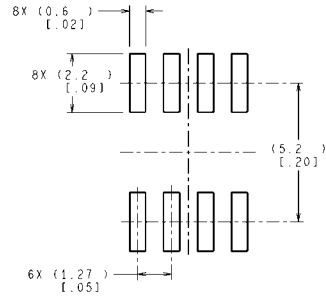
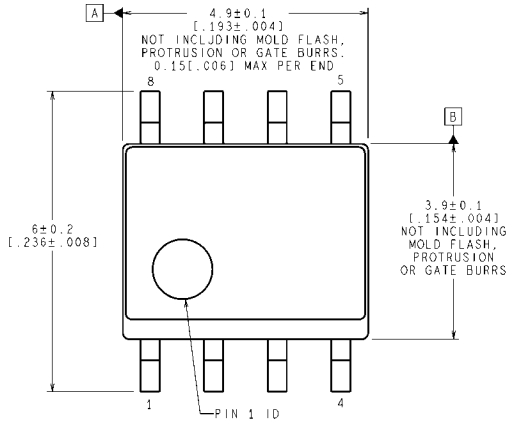
INPUTS		OUTPUT
$\overline{\text{RE}}$	(RI+)-(RI-)	
L	L (< -100 mV)	L
L	H (> +100 mV)	H
L	100 mV > & > -100 mV	X
H	X	Z

X = High or Low logic state
Z = High impedance state
L = Low state
H = High state

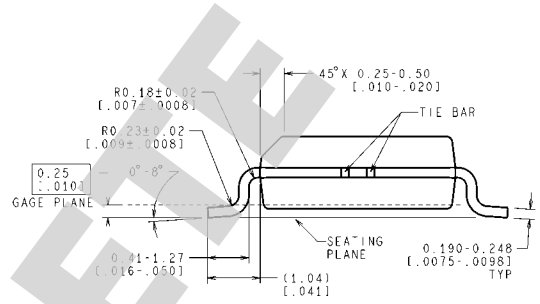
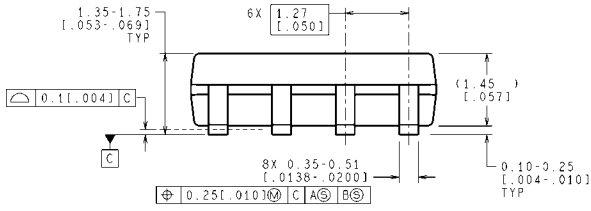
TABLE 4. Device Pin Description

Pin Name	Pin #	Input/Output	Description
DIN	2	I	TTL Driver Input
DO \pm /RI \pm	6, 7	I/O	LVDS Driver Outputs/LVDS Receiver Inputs
R _{OUT}	3	O	TTL Receiver Output
$\overline{\text{RE}}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
V _{CC}	8	NA	Power Supply

Physical Dimensions inches (millimeters) unless otherwise noted



RECOMMENDED LAND PATTERN



CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [] ARE INCHES
DIMENSIONS IN () FOR REFERENCE ONLY

See NS Package Number M08A

M08A (Rev M)

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Notes

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Notes

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Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempensors	SolarMagic™	www.national.com/solarmagic
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