# DSA1103/23

## Low-Jitter Precision LVDS Oscillator for Automotive

## Features

- Automotive AEC-Q100 Qualified
- Wide Frequency Range: 2.3 MHz to 460 MHz (LVDS)
- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability: ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Automotive Grade 1: –40°C to +125°C
  - Automotive Grade 2: –40°C to +105°C
  - Automotive Grade 3: –40°C to +85°C
- High Supply Noise Rejection: –50 dBc
- Small Industry Standard Footprints
  - 2.5 mm x 2.0 mm (VDFN)
  - 3.2 mm x 2.5 mm (VDFN & Wettable Flank)
  - 5.0 mm x 3.2 mm (CDFN)
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTBF than Quartz Oscillators
- Low Current Consumption
- Supply Range of 2.25 to 3.63V
- Standby and Output Enable Function
- Lead-Free and RoHS Compliant

## Applications

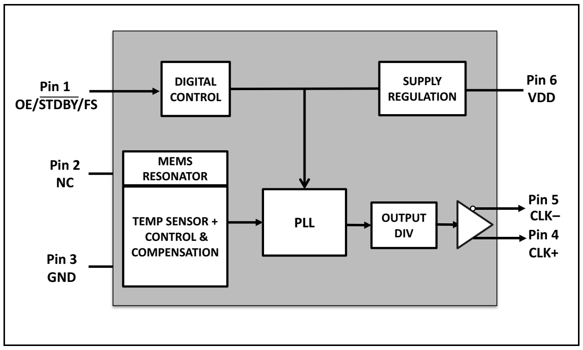
- Automotive Infotainment
- Automotive ADAS
- In-Vehicle Networking
- Autonomous Driving

## General Description

The DSA1103 and DSA1123 series of high performance oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of automotive applications like in-vehicle networking and autonomous driving.

DSA1103 has a standby feature that allows it to completely power-down when pin 1 is pulled low. For DSA1123, only the outputs are disabled when pin 1 is low. Both oscillators are available in industry standard packages, including the small 2.5 mm x 2.0 mm, and are drop-in replacements for standard 6-pin LVDS crystal oscillators. The wettable flank package improves solderability and visual inspection.

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Input Voltage, $V_{IN}$ ........ –0.3V to $V_{DD}$ +0.3V
Supply Voltage ........ –0.3V to + 4.0V
ESD Protection (HBM) ........ 4 kV
ESD Protection (MM) ........ 400V
ESD Protection (CDM) ........ 1.5 kV

**† Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{DD}$ = 3.3V; $T_A$ = +25°C unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage (Note 1) | $V_{DD}$ | 2.25 | — | 3.6 | V | — |
| Supply Current | $I_{DD}$ | — | — | 0.095 | mA | DSA1103, EN pin low. Output is disabled and device is in standby |
| | | — | 20 | 22 | | DSA1123, EN pin low, output is disabled |
| Frequency Stability | Δf | — | — | ±20 | ppm | Includes frequency variations due to initial tolerance, temp. and power supply voltage. |
| | | — | — | ±25 | | |
| | | — | — | ±50 | | |
| Aging - First year | $\Delta f_{Y1}$ | — | — | ±5 | ppm | One year @ 25°C |
| Aging - After first year | $\Delta f_{Y2}$ | — | — | <±1 | ppm/yr | Year two and beyond at +25°C |
| Startup Time (Note 2) | $t_{SU}$ | — | — | 5 | ms | T = +25°C |
| Input Logic Levels | $V_{IH}$ | 0.75 x $V_{DD}$ | — | — | V | Input logic high |
| | $V_{IL}$ | — | — | 0.25 x $V_{DD}$ | V | Input logic low |
| Output Disable Time (Note 3) | $t_{DS}$ | — | — | 5 | ns | — |
| Output Enable Time | $t_{EN}$ | — | — | 5 | ms | DSA1103 |
| | | | | 20 | ns | DSA1123 |
| Enable Pull-Up Resistor (Note 4) | — | — | 40 | — | kΩ | Internally pulled-up |
| **LVDS Output** | | | | | | |
| Supply Current | $I_{DD}$ | — | 29 | 32 | mA | Output enabled, $R_L$ = 100Ω |
| Output Offset Voltage | $V_{OS}$ | 1.125 | — | 1.4 | V | R = 100Ω differential |
| Delta Offset Voltage | $\Delta V_{OS}$ | — | — | 50 | mV | — |
| Peak-to-Peak Output Swing | $V_{PP}$ | — | 350 | — | mV | Single-ended |
| Output Logic Level High | $V_{OH}$ | 0.9 x $V_{DD}$ | — | — | V | I = ±6 mA |
| Output Logic Level Low | $V_{OL}$ | — | — | 0.1 x $V_{DD}$ | V | |
| Output Transition Rise Time (Note 3) | $t_R$ | — | 200 | — | ps | 20% to 80%, $R_L$ = 50Ω, $C_L$ = 2 pF |
| Output Transition Fall Time (Note 3) | $t_F$ | — | | — | | |
| Frequency | $f_O$ | 2.3 | — | 460 | MHz | –40°C to +85°C |
| | | 3.3 | — | 460 | | –40°C to +105°C and –40°C to +125°C |
| Output Duty Cycle | SYM | 48 | — | 52 | % | — |

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:** $V_{DD}$ = 3.3V; $T_A$ = +25°C unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Period Jitter | $J_{PER}$ | — | 2.5 | — | $ps_{RMS}$ | — |
| Integrated Phase Noise | $J_{PH}$ | — | 0.28 | — | $ps_{RMS}$ | 200 kHz to 20 MHz @ 156.25 MHz |
| | | — | 0.4 | — | | 100 kHz to 20 MHz @ 156.25 MHz |
| | | — | 1.7 | 2 | | 12 kHz to 20 MHz @ 125 MHz |

**Note 1:** Pin 6 $V_{DD}$ should be filtered with 0.1 µF capacitor.

**2:** $t_{SU}$ is time to 100 ppm of output frequency after $V_{DD}$ is applied and outputs are enabled.

**3:** Output Waveform and Test Circuit figures define the parameters.

**4:** Output is enabled if pad is floated or not connected.

## TEMPERATURE SPECIFICATIONS (Note 1)

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Operating Temperature Range (T) | $T_A$ | –40 | — | +85 | °C | Ordering Option I |
| | $T_A$ | –40 | — | +105 | °C | Ordering Option L |
| | $T_A$ | –40 | — | +125 | °C | Ordering Option A |
| Junction Operating Temperature | $T_J$ | — | — | +150 | °C | — |
| Storage Temperature Range | $T_A$ | –40 | — | +150 | °C | — |
| Soldering Temperature Range | $T_S$ | — | — | +260 | °C | 40 sec. max. |
| **Package Thermal Resistance** | | | | | | |
| 6-Lead CDFN 5.0 mm x 3.0 mm (B) | $R_{\theta JA}$ | — | — | 26 | °C/W | — |
| 6-Lead VDFN 3.2 mm x 2.5 mm (C) | | — | — | 45 | | — |
| 6-Lead VDFN 2.5 mm x 2.0 mm (D) | | — | — | 258 | | — |

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: DSA1103/DSA1123 PIN FUNCTION TABLE**

| Pin Number | Pin Name | Pin Type | Description |
|---|---|---|---|
| 1 | OE | I | Output Enable (DSA1123)<br>H = Specified frequency output.<br>L = Output is high impedance. |
| | $\overline{\text{STDBY}}$ | | Standby: (DSA1103)<br>H = Specified frequency output.<br>L = Output is high impedance.<br>Device in low power mode; Supply current = $I_{STDBY}$. |
| 2 | NC | No Connect | Do not connect. |
| 3 | GND | Power | Power supply ground. |
| 4 | CLK+ | O | Clock output. |
| 5 | CLK– | | |
| 6 | VDD | Power | Power supply. |

## 3.0 NOMINAL PERFORMANCE CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Unless otherwise specified, T = +25°C, $V_{DD}$ = 3.3V.

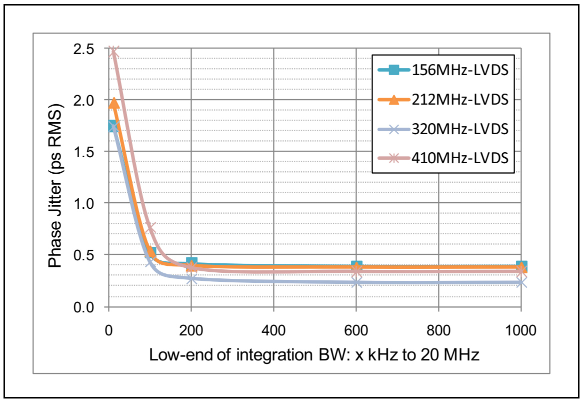


***FIGURE 3-1:*** *Phase Jitter (Integrated Phase Noise).*

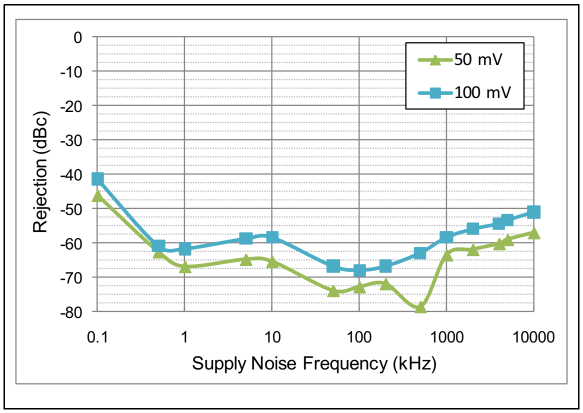


***FIGURE 3-2:*** *Power Supply Rejection Ratio.*

## 4.0 OUTPUT WAVEFORM

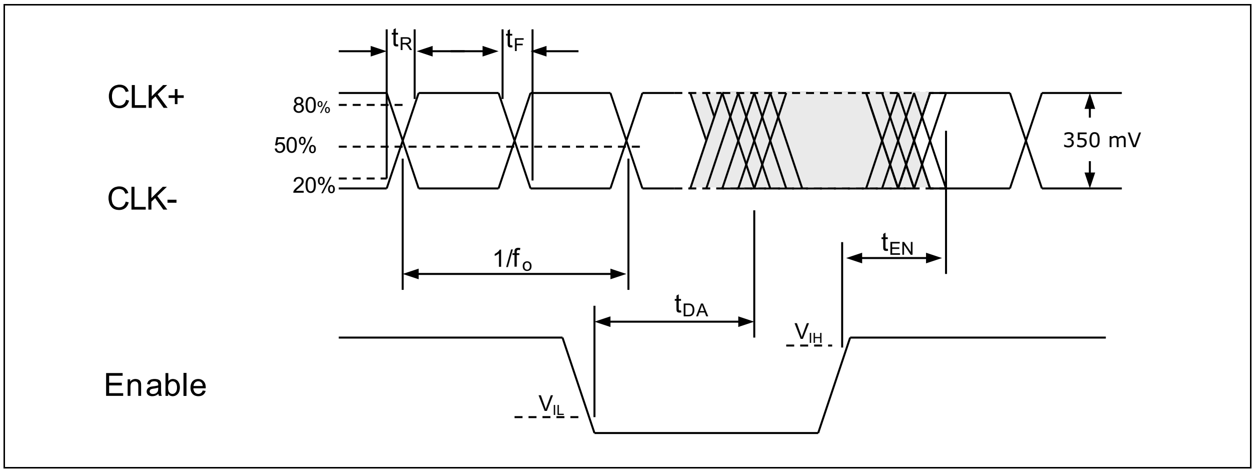


***FIGURE 4-1:*** *DSA1103/23 Output Waveform.*

## 5.0 TYPICAL TERMINATION SCHEME

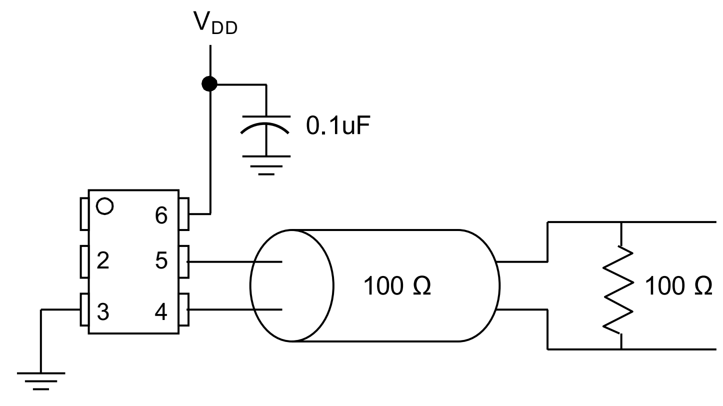


***FIGURE 5-1:*** *Typical Termination Scheme for DSA1103/23.*

## 6.0 BOARD LAYOUT (RECOMMENDED)

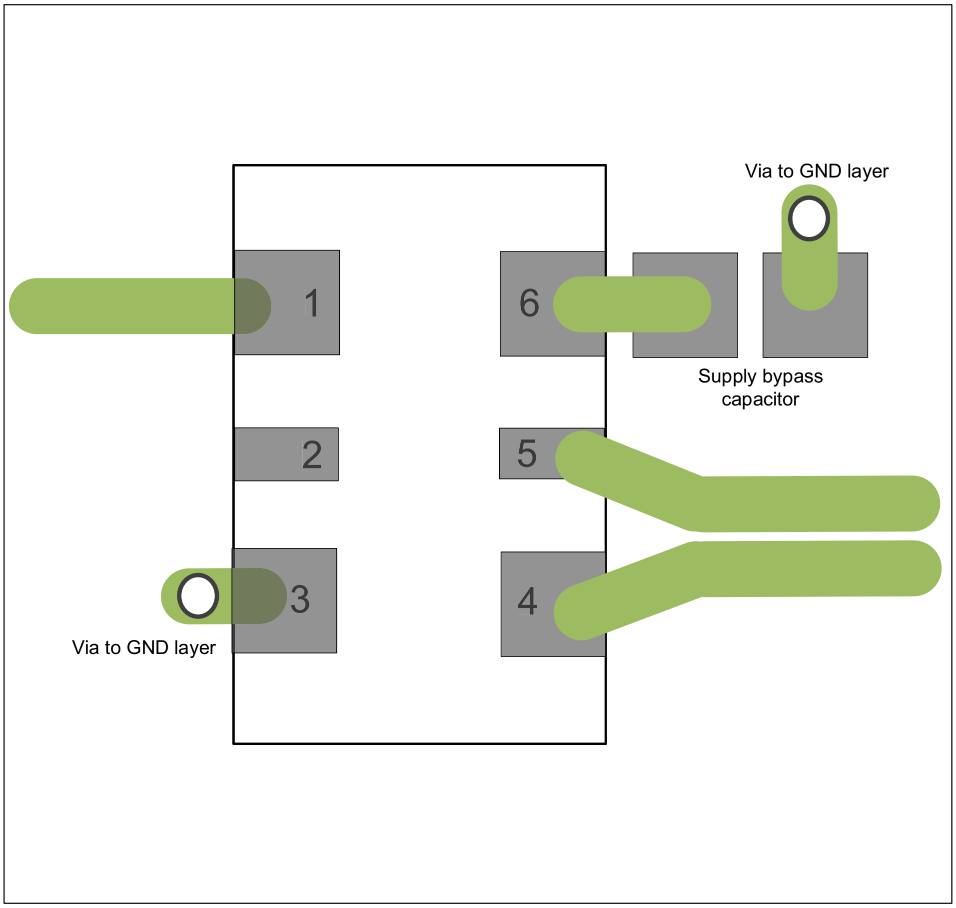


***FIGURE 6-1:*** *DSA1103/23 Recommended Board Layout.*

**Note:** Ferrite beads in series with the power supply are not recommended, since they can prevent device start-up by limiting start-up current. If a ferrite bead is used, a tantalum bypass capacitor of at least 20 µF at pin 6 is recommended and correct start-up verified.

## 7.0 SOLDER REFLOW PROFILE

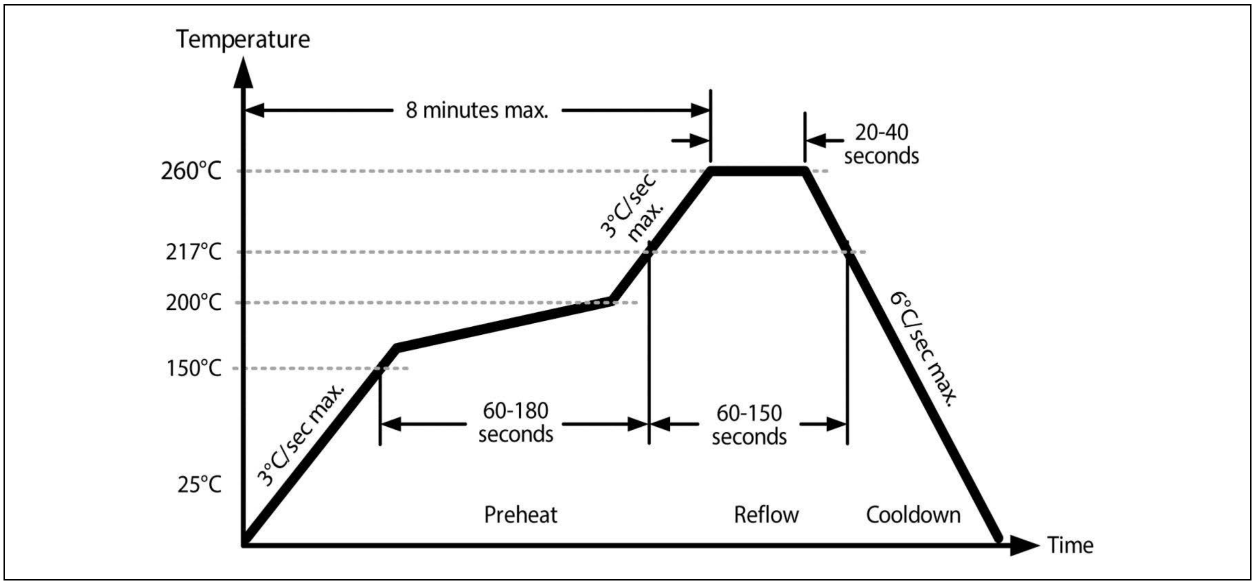


**FIGURE 7-1:** *Solder Reflow Profile.*

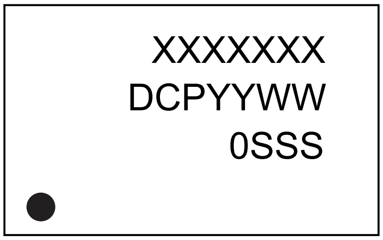
**TABLE 7-1: SOLDER REFLOW**

| **MSL 1 @ 260°C Refer to JSTD-020C** | |
|---|---|
| Ramp-Up Rate (200°C to Peak Temp.) | 3°C/sec. max. |
| Preheat Time 150°C to 200°C | 60 to 180 sec. |
| Time Maintained above 217°C | 60 to 150 sec. |
| Peak Temperature | 255°C to 260°C |
| Time within 5°C of Actual Peak | 20 to 40 sec. |
| Ramp-Down Rate | 6°C/sec. max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

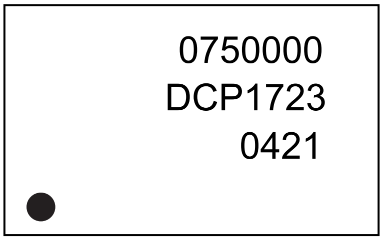
# 8.0 PACKAGING INFORMATION

## 8.1 Package Marking Information

6-Pin CDFN/VDFN*



Example



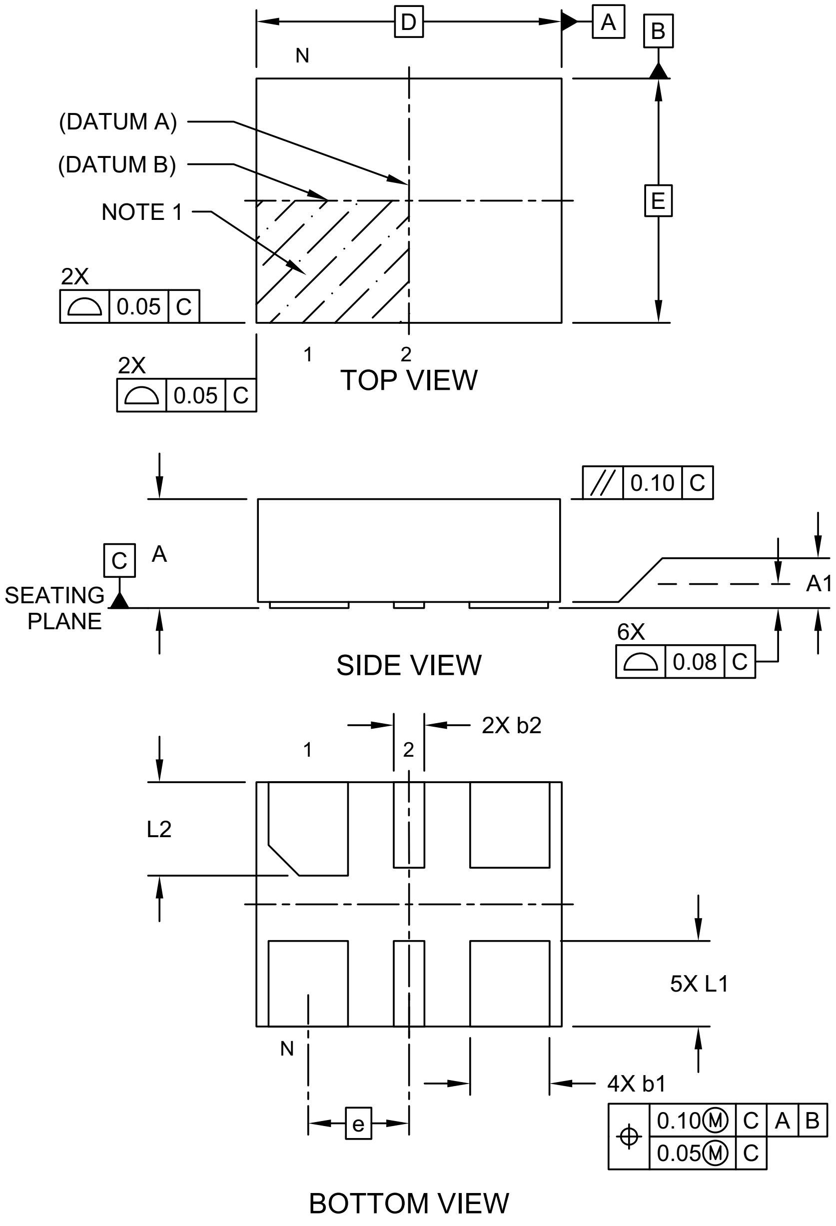
| | | |
|---|---|---|
| **Legend:** | XX...X | Product code, customer-specific information, or frequency in MHz without printed decimal point |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | SSS | Alphanumeric traceability code |
| | e3 | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

## 6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

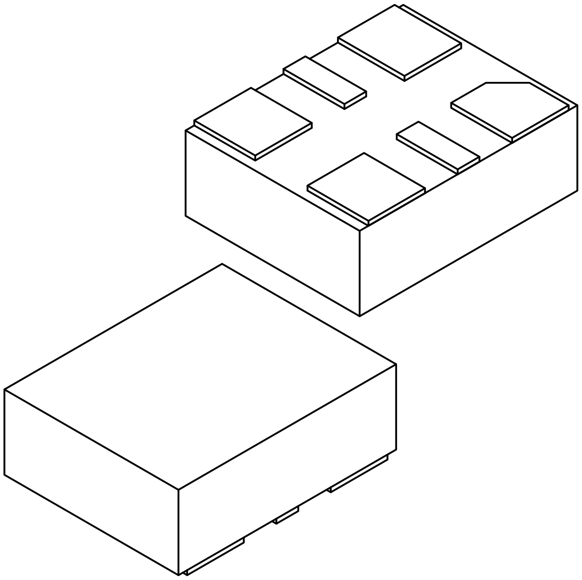
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1005 Rev C Sheet 1 of 2

## 6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 6 | |
| Pitch | e | | 0.825 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Overall Length | D | | 2.50 BSC | |
| Overall Width | E | | 2.00 BSC | |
| Terminal Width | b1 | 0.60 | 0.65 | 0.70 |
| Terminal Width | b2 | 0.20 | 0.25 | 0.30 |
| Terminal Length | L1 | 0.60 | 0.70 | 0.80 |
| Terminal Length | L2 | 0.665 | 0.765 | 0.865 |

Notes:

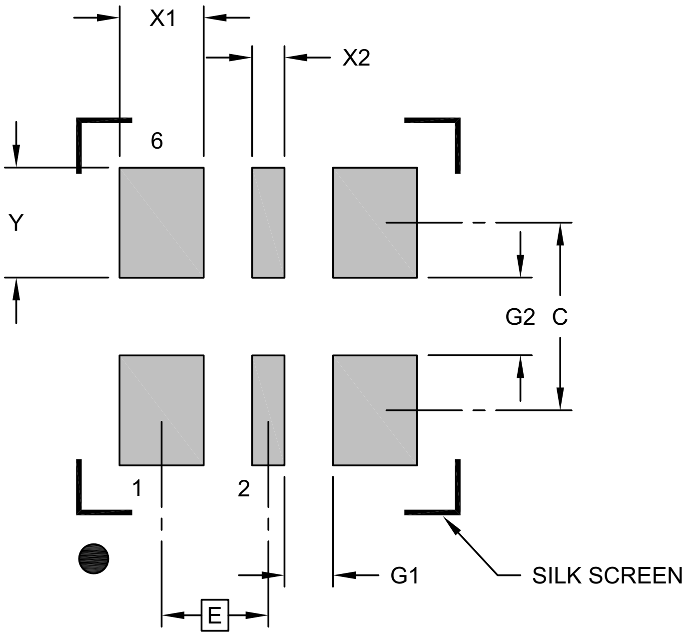
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005 Rev C Sheet 2 of 2

## 6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.825 BSC | | |
| Contact Pad Width (X4) | X1 | | | 0.65 |
| Contact Pad Width (X2) | X2 | | | 0.25 |
| Contact Pad Length (X6) | Y | | | 0.85 |
| Contact Pad Spacing | C | | 1.45 | |
| Space Between Contacts (X4) | G1 | 0.38 | | |
| Space Between Contacts (X3) | G2 | 0.60 | | |

Notes:

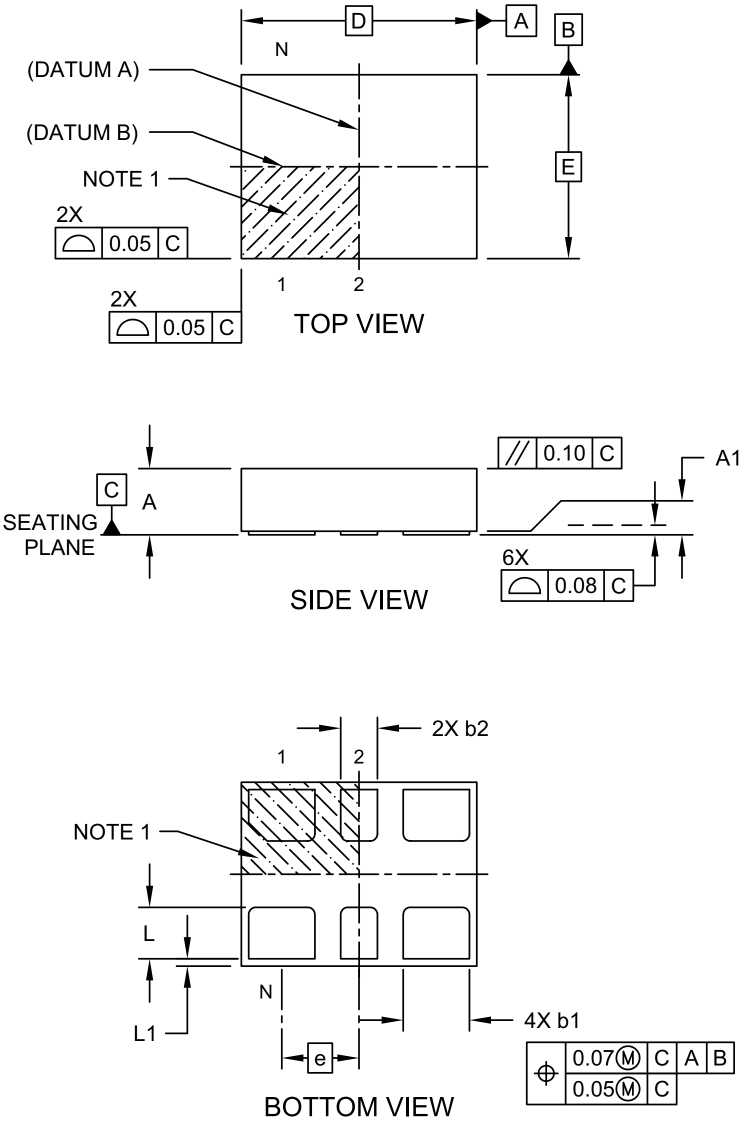
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3005 Rev C

## 6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

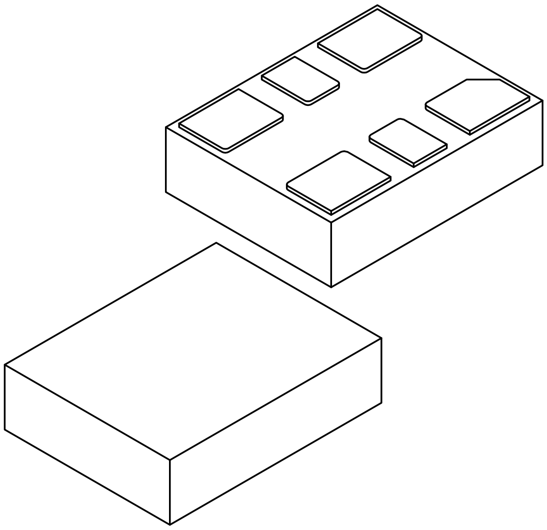
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



Microchip Technology Drawing C04-1007A Sheet 1 of 2

## 6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| | Dimension Limits | MIN | NOM | MAX |
| Number of Terminals | N | | 6 | |
| Pitch | e | | 1.05 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Overall Length | D | | 3.20 BSC | |
| Overall Width | E | | 2.50 BSC | |
| Terminal Width | b1 | 0.85 | 0.90 | 0.95 |
| Terminal Width | b2 | 0.45 | 0.50 | 0.55 |
| Terminal Length | L | 0.65 | 0.70 | 0.75 |
| Terminal Pullback | L1 | | 0.10 REF | |

Notes:

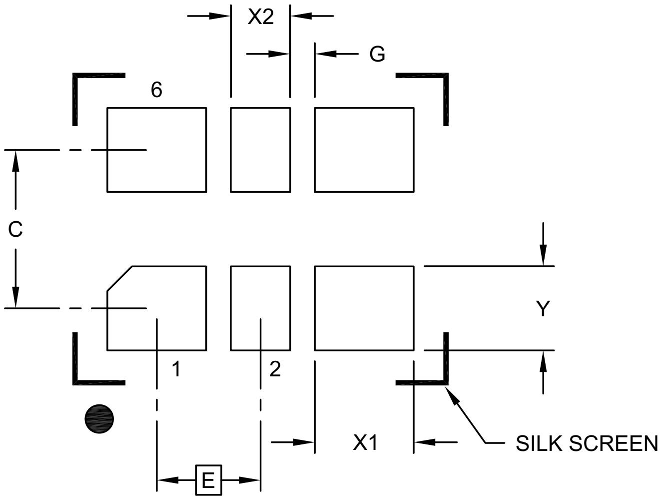
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1007A Sheet 2 of 2

## 6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.05 BSC | |
| Contact Pad Spacing | C | | 1.60 | |
| Contact Pad Width (X4) | X1 | | | 1.00 |
| Contact Pad Width (X2) | X2 | | | 0.60 |
| Contact Pad Length (X6) | Y | | | 0.85 |
| Space Between Contacts (X4) | G1 | 0.25 | | |

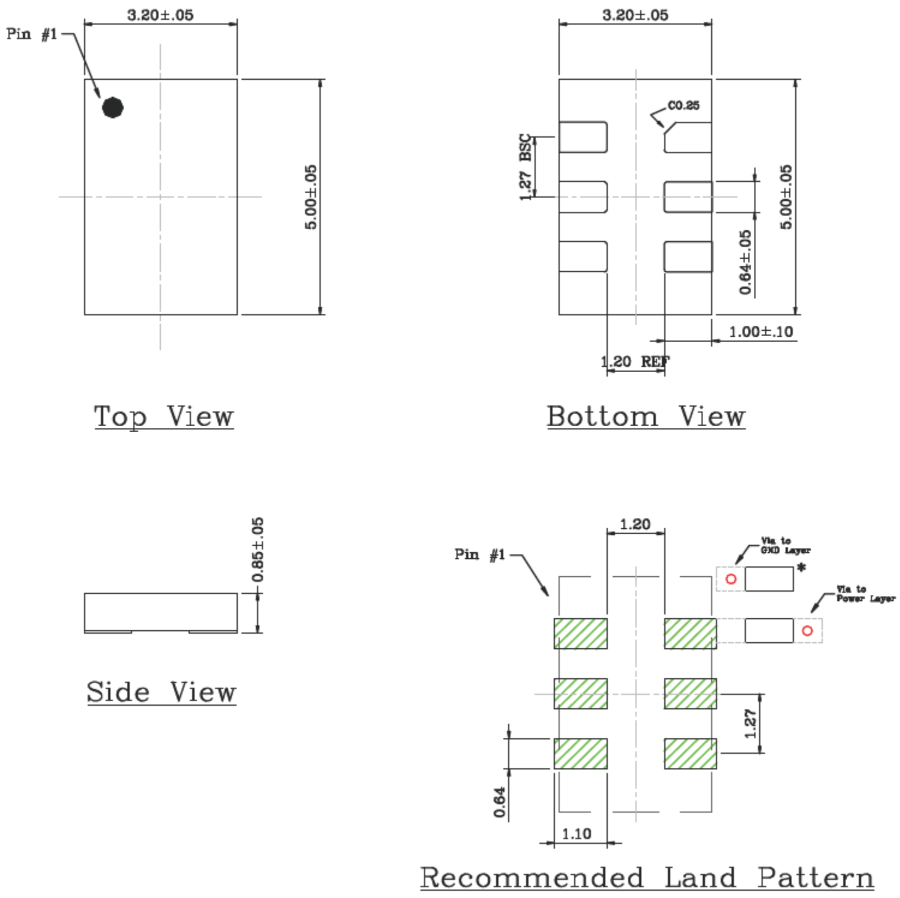
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007A

**TITLE**
6 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| **DRAWING #** | CDFN5032-6LD-PL-1 | **UNIT** | MM |
|---|---|---|---|



Top View

Bottom View

Side View

Recommended Land Pattern

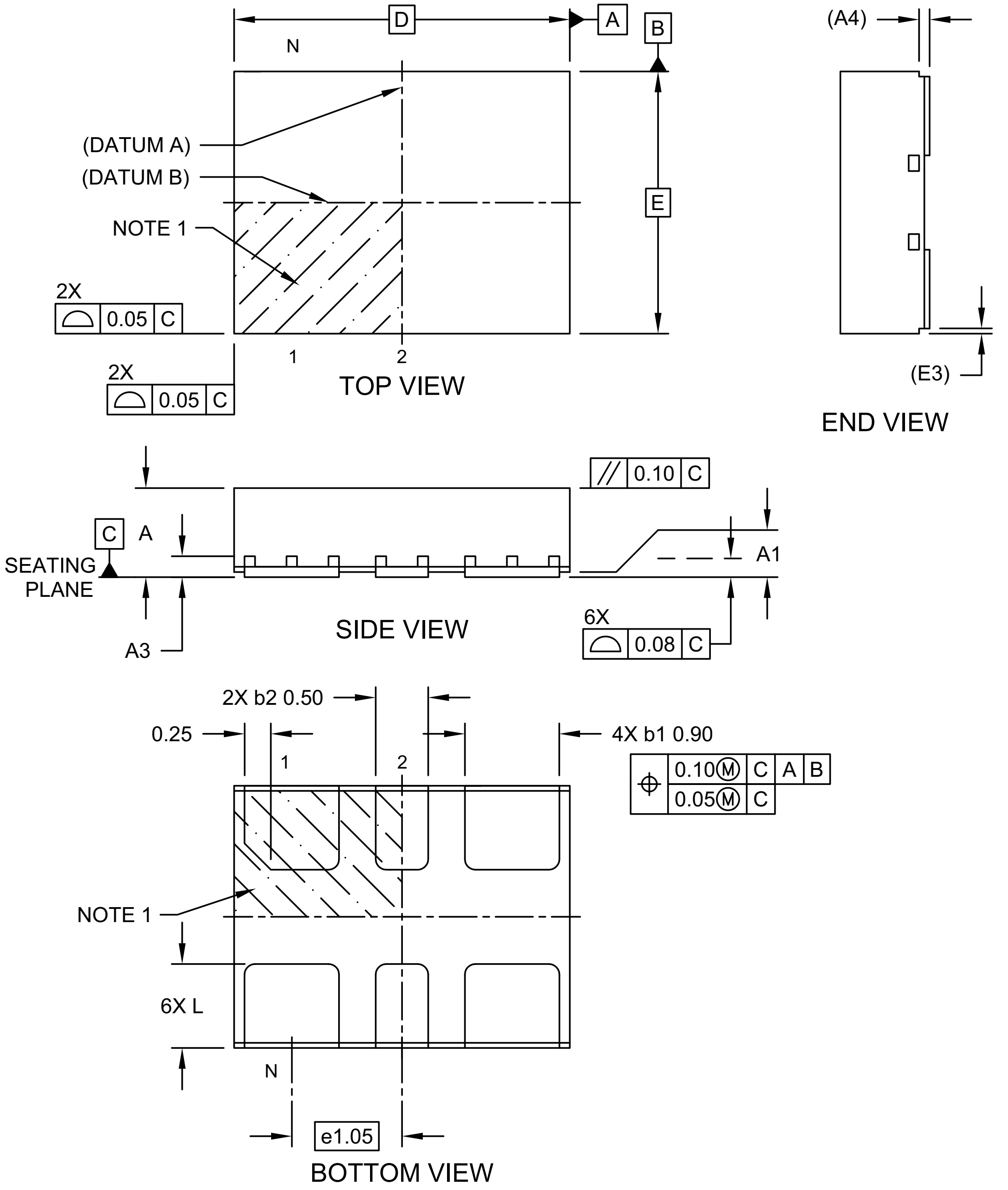
NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

## 6-Lead Very Thin Plastic Dual Flat, No Lead Package (KDA) - 3.2x2.5 mm Body [VDFN] With Stepped Wettable Flanks

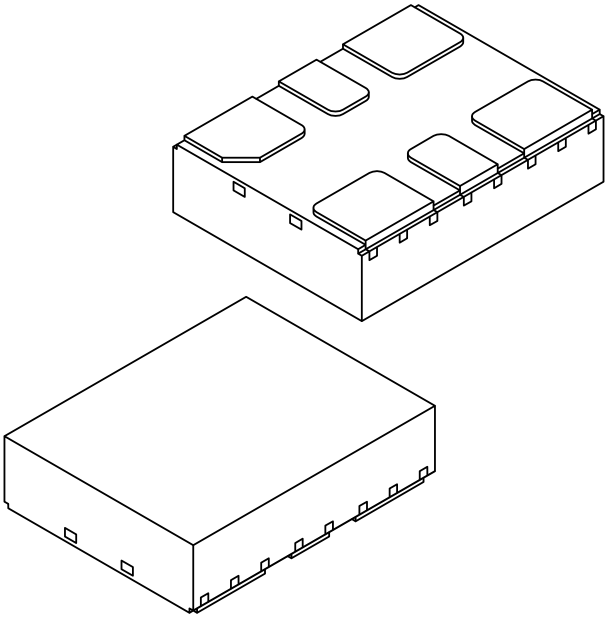
| | |
|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |



Microchip Technology Drawing C04-01252 Rev A Sheet 1 of 2

## 6-Lead Very Thin Plastic Dual Flat, No Lead Package (KDA) - 3.2x2.5 mm Body [VDFN] With Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 6 | |
| Pitch | e | | 1.05 BSC | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | 0.15 | 0.20 | 0.25 |
| Overall Length | D | | 3.20 BSC | |
| Overall Width | E | | 2.50 BSC | |
| Terminal Width | b1 | 0.85 | 0.90 | 0.95 |
| Terminal Width | b2 | 0.45 | 0.50 | 0.55 |
| Terminal Length | L | 0.70 | 0.80 | 0.90 |
| Step Width | E3 | | 0.05 REF | |
| Step Height | A4 | | 0.10 REF | |

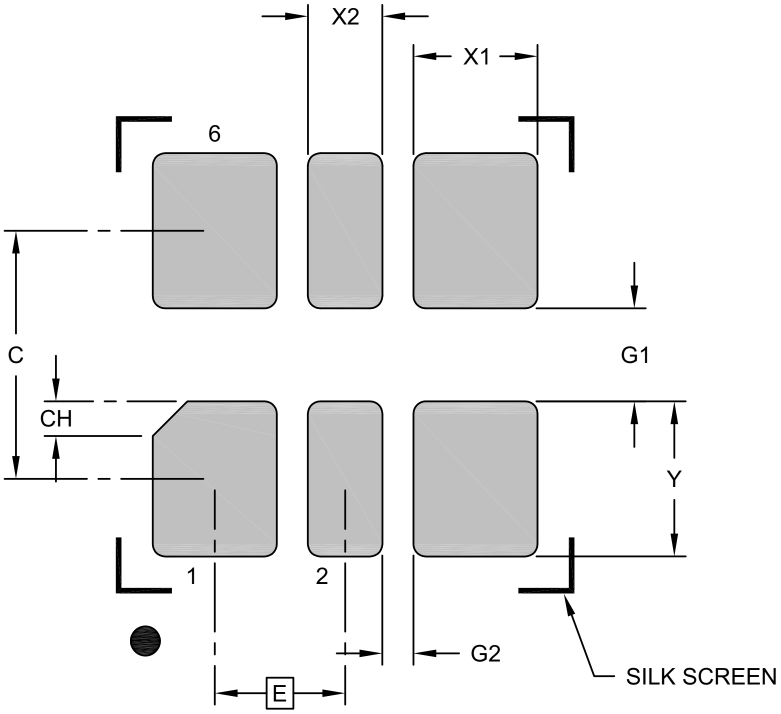
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-01252 Rev A Sheet 2 of 2

## 6-Lead Very Thin Plastic Dual Flat, No Lead Package (KDA) - 3.2x2.5 mm Body [VDFN] With Stepped Wettable Flanks

| | |
|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |



RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.05 BSC | |
| Contact Pad Spacing | C | | 2.00 | |
| Contact Pad Width (X20) | X1 | | | 1.00 |
| Optional Center Pad Width | X2 | | | 0.60 |
| Contact Pad Length (X20) | Y | | | 0.80 |
| Contact Pad to Contact Pad (X3) | G1 | 0.75 | | |
| Contact Pad to Contact Pad (X4) | G2 | 0.25 | | |
| Terminal 1 Corner Chamfer | CH | | 0.28 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-03252 Rev A

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision A (June 2019)

- Initial release of DSA1103/23 as Microchip data sheet DS20005891B.
- Minor changes throughout the data sheet.

## Revision B (August 2022)

- Updated the General Description.
- Removed ±10 ppm from the Electrical Characteristics table in the Frequency Stability row.

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | X | 3 | X | X | X | -XXX.XXXX | X | XXX |
|---|---|---|---|---|---|---|---|---|
| Device (First 2 Digits) | Enable Modes | Device (First 2 Digits) | Package | Temperature Range | Frequency Stability | Frequency | Media Type | Automotive Suffix |

| | | | |
|---|---|---|---|
| **Device:** | DSA11x3: | | Low-Jitter Precision LVDS Oscillator for Automotive |
| **Enable Modes:** | 0 | = | Enable/Standby |
| | 2 | = | Enable/Disable |
| **Package:** | B | = | 5.0 mm x 3.2 mm CDFN |
| | C | = | 3.2 mm x 2.5 mm VDFN |
| | D | = | 2.5 mm x 2.0 mm VDFN |
| | W | = | 3.2 mm x 2.5 mm VDFN (Wettable Flanks) |
| **Temperature Range:** | A | = | –40°C to +125°C |
| | L | = | –40°C to +105°C |
| | I | = | –40°C to +85°C |
| **Stability:** | 1 | = | ±50 ppm |
| | 2 | = | ±25 ppm |
| | 3 | = | ±20 ppm |
| **Frequency Code:** | xxx.xxxx | = | 2.3 MHz to 460 MHz (user-defined) |
| **Media Type:** | T | = | 1,000/Reel |
| | (blank) | = | 100/Tube |
| **Automotive Suffix:** | VXX | = | Automotive Suffix in which “XX” is assigned by Microchip. |

Note: Please use the Microchip Clockworks tool to check AEC-Q100 compliance status and build the exact part number.

**Examples:**

| | |
|---|---|
| a) DSA1123BI2-400.0000TVA0: | Low-Jitter Precision LVDS Oscillator for Automotive, Enable/Disable, 5x3.2 CDFN, –40°C to +85°C, ±25ppm, 400 MHz, 1000/Reel |
| b) DSA1103CL3-074.2500VA0: | Low-Jitter Precision LVDS Oscillator for Automotive, Enable/Standby, 3.2x2.5 VDFN, –40°C to +105°C, ±20 ppm, 74.25 MHz, 100/Tube |
| c) DSA1103WI2-056.0000VA0: | Low-Jitter Precision LVDS Oscillator for Automotive, Enable/Standby, 3.2x2.5 VDFN (Wettable Flanks), –40°C to +85°C, ±25 ppm, 56 MHz, 100/Tube |

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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