



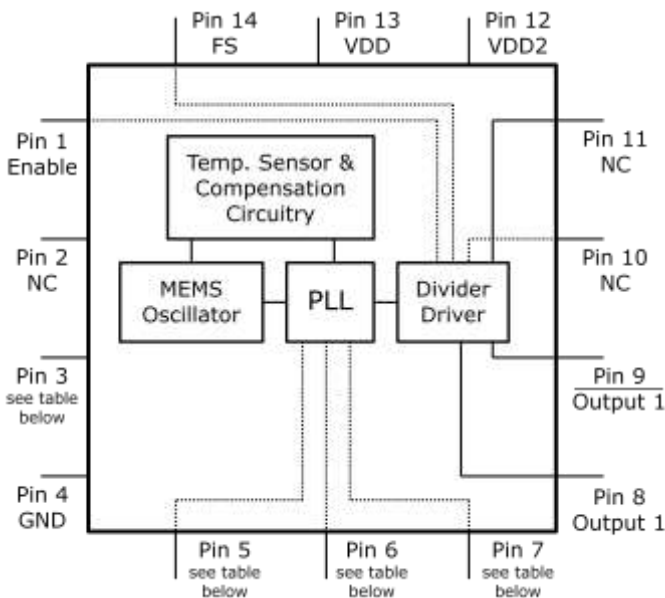
## Low-Jitter I<sup>2</sup>C/SPI Programmable LVPECL Oscillator

### General Description

The DSC2120 and DSC2220 series of programmable, high-performance LVPECL oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability while incorporating high output frequency flexibility. DSC2120 and DSC2220 allow the user to modify the output frequency using I<sup>2</sup>C or SPI interface, respectively. User can also select from two pre-programmed default output frequencies using the control pin.

DSC2120 and DSC2220 are packaged in 14-pin 3.2x2.5 mm QFN packages and available in temperature grades from Ext. Commercial to Industrial.

### Block Diagram



Pin #	DSC2120 (I <sup>2</sup> C)	DSC2220 (SPI)
3	NC	SCLK
5	SDA	MOSI
6	SCL	MISO
7	CS_bar	SS

### Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **I<sup>2</sup>C/SPI Programmable Output Freq**
- **Short Lead Times: 2 Weeks**
- **Wide Freq. Range:**
  - LVPECL Output: 2.3 to 460 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

### Applications

- **Consumer Electronics**
- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

## Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	DSC2120: Leave unconnected or grounded
	SCLK	I	DSC2220: Serial clock from master
4	GND	Power	Ground
5	SDA	I	DSC2120: I <sup>2</sup> C Serial Data
	MOSI		DSC2220: SPI Serial Data from Master to Slave
6	SCL	I	DSC2120: I <sup>2</sup> C Serial Clock
	MISO	O	DSC2220: SPI Serial Data from Slave to Master
7	CS_bar	I	DSC2120: I <sup>2</sup> C Chip Select (Active Low)
	SS	I	DSC2220: SPI Slave Select (Active Low)
8	Output1+	O	Positive LVPECL Output
9	Output1-	O	Negative LVPECL Output
10	NC	NA	Leave unconnected or grounded
11	NC	NA	Leave unconnected or grounded
12	VDD2	Power	Power Supply
13	VDD	Power	Power Supply
14	FS	I	Default output clock frequency bit

## Operational Description

The DSC2120/2220 is a LVPECL oscillator consisting of a MEMS resonator and a support PLL IC. The LVPECL output is generated through independent 8-bit programmable dividers from the output of the internal PLL.

DSC2120/2220 allows for easy programming of the output frequencies using I<sup>2</sup>C/SPI interface. Upon power-up, the initial output frequency is controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for two different default frequencies. The control

pin (FS) selects the initial frequency. Once the device is powered up, a new output frequency can be programmed. Programming details are provided in the **Programming Guide**. Standard default frequencies are described in the following sections. Discera supports customer defined versions of the DSC2120/2220.

When Enable (pin 1) is floated or connected to VDD, the DSC2120/2220 is in operational mode. Driving Enable to ground will disable both output drivers (hi-impedance mode).

## Default Output Clock Frequencies

Table 2 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 2. Pre-programmed pin-selectable output frequency combinations

Ordering Info	Freq (MHz)	Select Bit [FS] – <b>Default is [1]</b>	
		0	<b>1</b>
B0001	f <sub>OUT</sub>	125	<b>212.5</b>
BXXXX	f <sub>OUT</sub>	Contact factory for additional configurations.	

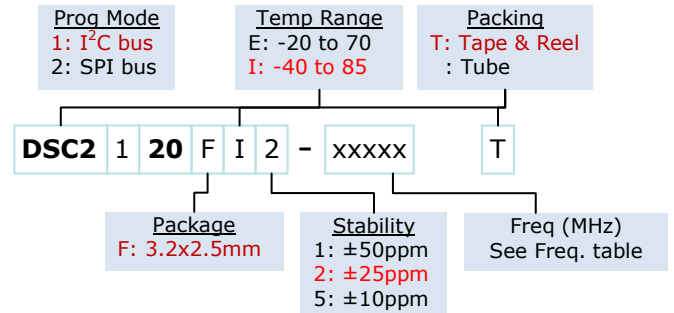
Frequency select bit are weakly tied high so if left unconnected the default setting will be [1] and the device will output the associated frequency highlighted in **Bold**.

## Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V <sub>DD</sub> +0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
	HBM	4000		
	MM	400		
	CDM	1500		

Note: 1000+ years of data retention on internal memory

## Ordering Code



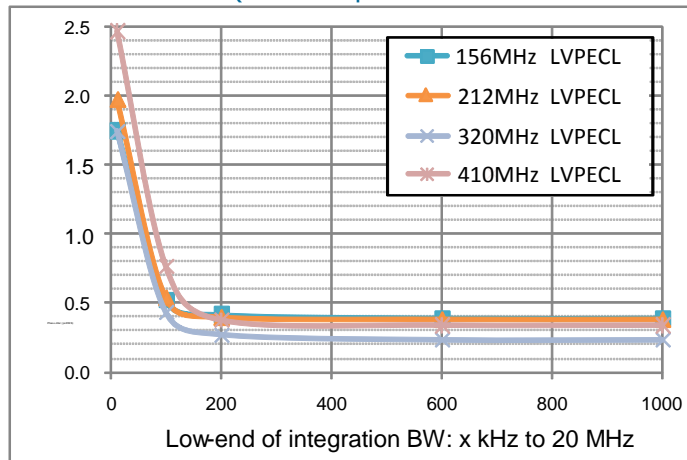
## Specifications (Unless specified otherwise: T=25° C)

Parameter	Condition	Min.	Typ.	Max.	Unit
Supply Voltage <sup>1</sup>	V <sub>DD</sub>	2.25		3.6	V
Supply Current	I <sub>DD</sub> EN pin low – output is disabled		21	23	mA
Supply Current <sup>2</sup>	I <sub>DD</sub> Output Enabled, R <sub>L</sub> =50Ω		56.5	58	mA
Frequency Stability	Δf Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf 1 year @25°C			±5	ppm
Startup Time <sup>2</sup>	t <sub>SU</sub> T=25°C			5	ms
Input Logic Levels					
Input logic high	V <sub>IH</sub>	0.75xV <sub>DD</sub>		-	V
Input logic low	V <sub>IL</sub>	-		0.25xV <sub>DD</sub>	
Output Disable Time <sup>3</sup>	t <sub>DA</sub>			5	ns
Output Enable Time	t <sub>EN</sub>			20	ns
Pull-Up Resistor <sup>4</sup>	Pull-up exists on all digital IO		40		kΩ
<b>LVPECL Output</b>					
Output Logic Levels					
Output logic high	V <sub>OH</sub>	R <sub>L</sub> =50Ω	V <sub>DD</sub> -1.08	-	V
Output logic low	V <sub>OL</sub>		-	V <sub>DD</sub> -1.55	
Pk to Pk Output Swing		Single-Ended		800	mV
Output Transition time <sup>4</sup>					
Rise Time	t <sub>R</sub>	20% to 80% R <sub>L</sub> =50Ω		250	ps
Fall Time	t <sub>F</sub>				
Frequency	f <sub>0</sub>	Single Frequency	2.3	460	MHz
Output Duty Cycle	SYM	Differential	48	52	%
Period Jitter <sup>5</sup>	J <sub>PER</sub>	F <sub>0</sub> =156.25 MHz		2.5	ps <sub>RMS</sub>
Integrated Phase Noise	J <sub>PH</sub>	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	ps <sub>RMS</sub>

### Notes:

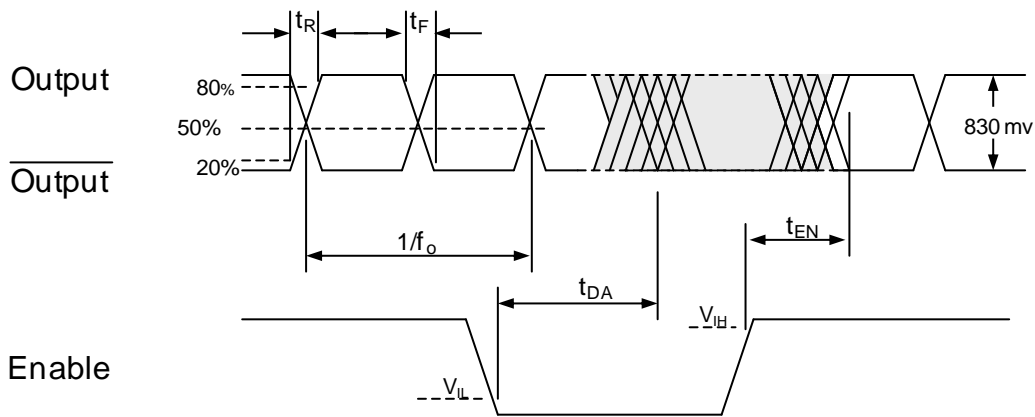
- Pin 4 V<sub>DD</sub> should be filtered with 0.01uF capacitor.
- Output is enabled if Enable pad is floated or not connected.
- t<sub>SU</sub> is time to 100PPM stable output frequency after V<sub>DD</sub> is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Period Jitter includes crosstalk from adjacent output.

**Nominal Performance Parameters** (Unless specified otherwise: T=25° C, V<sub>DD</sub>=3.3 V)

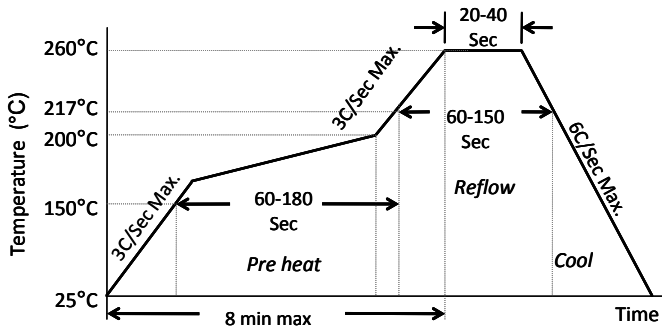


LVPECL Phase jitter (integrated phase noise)

**Output Waveform: LVPECL**



## Solder Reflow Profile



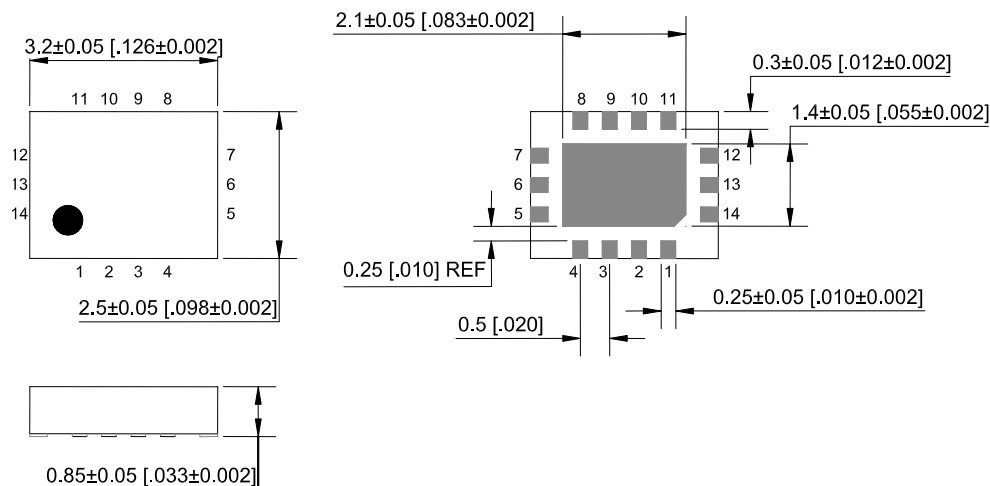
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

## Package Dimensions

### 3.2 x 2.5 mm 14 Lead Plastic Package

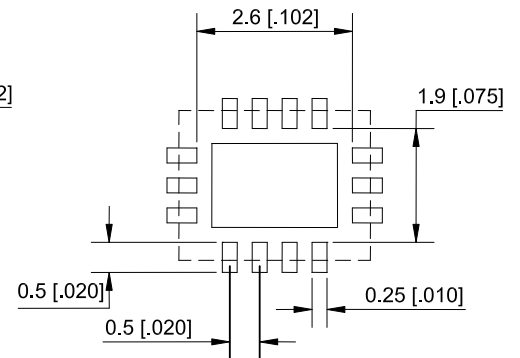
#### External Dimensions

units: mm[inch]



#### Recommended Solder Pad Layout

units: mm[inch]



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