



# Low-Jitter Configurable LVDS Oscillator

#### **General Description**

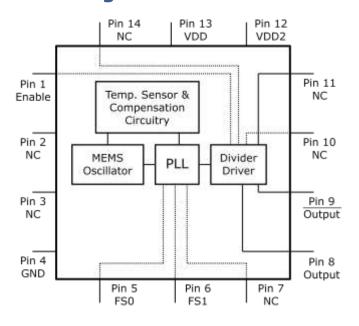
The DSC2030 series of high performance LVDS oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The DSC2030 allows the user to easily modify the frequency of the oscillator using pins. The DSC2030 has provision for up to four user-defined preprogrammed, pin-selectable output frequencies.

DSC2030 is packaged in a 14-pin 3.2x2.5 mm QFN package and available in temperature grades from Ext. Commercial to Automotive.

#### **Features**

- Low RMS Phase Jitter: <1 ps (typ)
- High Stability: ±10, ±25, ±50 ppm
- Wide Temperature Range
  - o Industrial: -40° to 85° C
  - o Ext. commercial: -20° to 70° C
- High Supply Noise Rejection: -50 dBc
- 4 Pin-Selectable Output Frequencies
- Short Lead Times: 2 Weeks
- Wide Freq. Range:
  - LVDS Output: 2.3 to 460 MHz
- Miniature Footprint of 3.2x2.5mm
- Excellent Shock & Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - o 20x better MTF than quartz oscillators
- Supply Range of 2.25 to 3.6 V
- Lead Free & RoHS Compliant

### **Block Diagram**



# **Applications**

- Consumer Electronics
- Storage Area Networks
  - o SATA, SAS, Fibre Channel
- Passive Optical Networks
  - o EPON, 10G-EPON, GPON, 10G-PON
- Ethernet
  - o 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express



#### **Pin Description**

| Pin No. | Pin Name | Pin Type | Description                                     |  |
|---------|----------|----------|---|--|
| 1       | Enable   | I        | Enables outputs when high and disables when low |  |
| 2       | NC       | NA       | Leave unconnected or grounded                   |  |
| 3       | NC       | NA       | Leave unconnected or grounded                   |  |
| 4       | GND      | Power    | Ground  |  |
| 5       | FS0      | I        | Least significant bit for frequency selection   |  |
| 6       | FS1      | I        | Most significant bit for frequency selection    |  |
| 7       | NC       | NA       | Leave unconnected or grounded                   |  |
| 8       | Output+  | 0        | Positive LVDS Output                            |  |
| 9       | Output-  | 0        | Negative LVDS Output                            |  |
| 10      | NC       | NA       | Leave unconnected or grounded                   |  |
| 11      | NC       | NA       | Leave unconnected or grounded                   |  |
| 12      | VDD2     | Power    | Power Supply                                    |  |
| 13      | VDD      | Power    | Power Supply                                    |  |
| 14      | NC       | NA       | Leave unconnected or grounded                   |  |

#### **Operational Description**

The DSC2030 is a LVDS oscillator consisting of a MEMS resonator and a support PLL IC. The LVDS output is generated through independent 8-bit programmable dividers from the output of the internal PLL.

The actual frequency output by the DSC2030 is controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to four

different frequencies. Two control pins (FS0 – FS1) select the output frequency. Discera supports customer defined versions of the DSC2030. Standard frequency options are described in the following sections.

When Enable (pin 1) is floated or connected to VDD, the DSC2030 is in operational mode. Driving Enable to ground will tri-state output driver (hi-impedance mode).

## **Output Clock Frequencies**

Table 1 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 1. Pre-programmed pin-selectable output frequency combinations

| Ordering | Freq             | Freq Select Bits [FS1, FS0] - <b>Default is [11]</b> |          |        |       |  |
|----------|------------------|--|----------|--------|-------|--|
| Info     | (MHz)            | 00   | 01       | 10     | 11    |  |
| C0001    | f <sub>OUT</sub> | 148.35165  | 74.17582 | 148.5  | 74.25 |  |
| C0002    | f <sub>OUT</sub> | 100  | 0*       | 0*     | 100   |  |
| C0003    | f <sub>OUT</sub> | 100  | 150      | 156.25 | 312.5 |  |
| C0004    | f <sub>OUT</sub> | 148.5  | 148.35   | 0*     | 0*    |  |
| C0005    | f <sub>OUT</sub> | 315  | 0*       | 0*     | 315   |  |
| C000X    | f <sub>OUT</sub> | Contact factory for additional configurations.       |          |        |       |  |

Frequency select bit are weakly tied high so if left unconnected the default setting will be [11] and the device will output the associated frequency highlighted in **Bold**.  $0^*$  – denotes invalid selection, output frequency is not specified.

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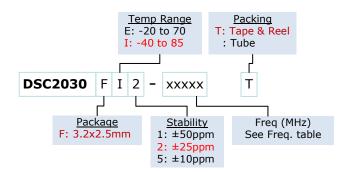


# **Absolute Maximum Ratings**

| Item           | Min  | Max            | Unit | Condition  |
|----------------|------|----------------|------|------------|
| Supply Voltage | -0.3 | +4.0           | V    |            |
| Input Voltage  | -0.3 | $V_{DD} + 0.3$ | V    |            |
| Junction Temp  | -    | +150           | °C   |            |
| Storage Temp   | -55  | +150           | °C   |            |
| Soldering Temp | -    | +260           | °C   | 40sec max. |
| ESD            | -    |                | V    |            |
| HBM            |      | 4000           |      |            |
| MM             |      | 400            |      |            |
| CDM            |      | 1500           |      |            |

#### Note: 1000+ years of data retention on internal memory

### **Ordering Code**



## **Specifications** (Unless specified otherwise: T=25° C)

| Parameter   |                                  | Condition  | Min.                 | Тур.               | Max.                      | Unit              |
|---|----------------------------------|--|----------------------|--------------------|---------------------------|-------------------|
| Supply Voltage <sup>1</sup>                             | $V_{DD}$                         |  | 2.25                 |                    | 3.6                       | V                 |
| Supply Current  | $I_{DD}$                         | EN pin low – output is disabled  |                      | 21                 | 23                        | mA                |
| Supply Current <sup>2</sup>                             | $I_{DD}$                         | EN pin high – outputs are enabled $R_L$ =100 $\Omega$ , $F_0$ = 156.25 MHz                   |                      | 29                 | 32                        | mA                |
| Frequency Stability                                     | Δf                               | Includes frequency variations due<br>to initial tolerance, temp. and<br>power supply voltage |                      |                    | ±10<br>±25<br>±50         | ppm               |
| Aging   | Δf                               | 1 year @25°C   |                      |                    | ±5                        | ppm               |
| Startup Time <sup>3</sup>                               | t <sub>su</sub>                  | T=25°C   |                      |                    | 5                         | ms                |
| Input Logic Levels Input logic high Input logic low     | $oldsymbol{V}_{IH}$              |  | 0.75xV <sub>DD</sub> |                    | -<br>0.25xV <sub>DD</sub> | V                 |
| Output Disable Time <sup>4</sup>                        | $t_DA$                           |  |                      |                    | 5                         | ns                |
| Output Enable Time                                      | t <sub>EN</sub>                  |  |                      |                    | 20                        | ns                |
| Pull-Up Resistor <sup>2</sup>                           |                                  | Pull-up exists on all digital IO   |                      | 40                 |                           | kΩ                |
|   | LVDS Output                      |  |                      |                    |                           |                   |
| Output Offset Voltage                                   |                                  | R=100Ω Differential  | 1.125                |                    | 1.4                       | V                 |
| Delta Offset Voltage                                    |                                  |  |                      |                    | 50                        | mV                |
| Pk to Pk Output Swing                                   |                                  | Single-Ended   |                      | 350                |                           | mV                |
| Output Transition time <sup>4</sup> Rise Time Fall Time | t <sub>R</sub><br>t <sub>F</sub> | 20% to $80%$ R <sub>L</sub> = $100Ω$ , C <sub>L</sub> = $2pF$                                |                      | 200                | 350                       | ps                |
| Frequency   | $f_0$                            | Single Frequency   | 2.3                  |                    | 460                       | MHz               |
| Output Duty Cycle                                       | SYM                              | Differential   | 48                   |                    | 52                        | %                 |
| Period Jitter <sup>5</sup>                              | $J_{PER}$                        | F <sub>O</sub> =156.25 MHz   |                      | 2.5                |                           | ps <sub>RMS</sub> |
| Integrated Phase Noise                                  | J <sub>CC</sub>                  | 200kHz to 20MHz @156.25MHz<br>100kHz to 20MHz @156.25MHz<br>12kHz to 20MHz @156.25MHz        |                      | 0.28<br>0.4<br>1.7 | 2                         | ps <sub>RMS</sub> |

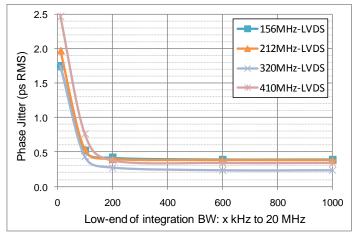
#### Notes:

- Pin 4  $V_{\text{DD}}$  should be filtered with 0.01uf capacitor.
- Output is enabled if Enable pad is floated or not connected.
- 3. 4. 5.  $t_{\text{SU}}$  is time to 100PPM stable output frequency after  $V_{\text{DD}}$  is applied and outputs are enabled. Output Waveform and Test Circuit figures below define the parameters. Period Jitter includes crosstalk from adjacent output.

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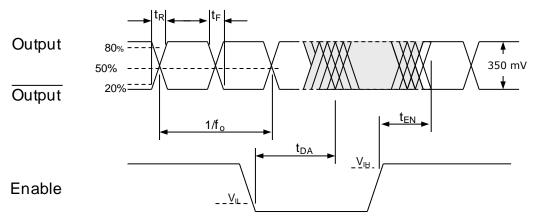


# Nominal Performance Parameters (Unless specified otherwise: T=25° C, V<sub>DD</sub>=3.3 V)



LVDS Phase jitter (integrated phase noise)

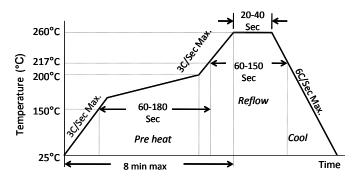
# **Output Waveform: LVDS**



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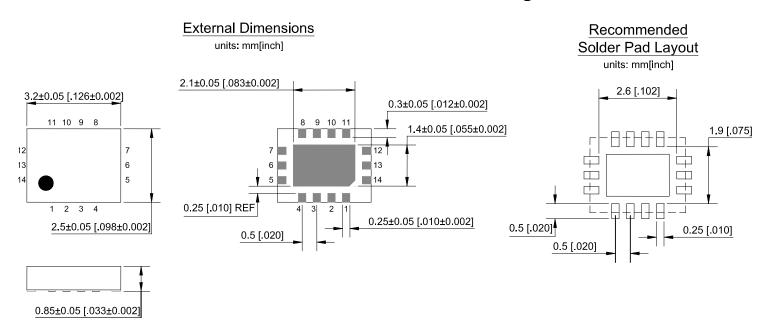
#### **Solder Reflow Profile**



| MSL 1 @ 260°C refer to JSTD-020C  |              |  |  |  |
|-----------------------------------|--------------|--|--|--|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/Sec Max. |  |  |  |
| Preheat Time 150°C to 200°C       | 60-180 Sec   |  |  |  |
| Time maintained above 217°C       | 60-150 Sec   |  |  |  |
| Peak Temperature                  | 255-260°C    |  |  |  |
| Time within 5°C of actual Peak    | 20-40 Sec    |  |  |  |
| Ramp-Down Rate                    | 6°C/Sec Max. |  |  |  |
| Time 25°C to Peak Temperature     | 8 min Max.   |  |  |  |

### **Package Dimensions**

#### 3.2 x 2.5 mm 14 Lead Plastic Package



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