DSC2032

Low-Jitter Configurable LVDS-LVPECL Oscillator

General Description

The DSC2032 series of high performance dual output oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. The two outputs are controlled by separate supply voltages to allow for high output isolation. The frequencies of the outputs can be identical or independently derived from a common PLL frequency source. The DSC2032 has provision for up to eight user-defined pre-programmed, pin selectable output frequency combinations.

DSC2032 is packaged in a 14-pin 3.2x2.5 mm QFN package and available in temperature grades from Ext. Commercial to Industrial.
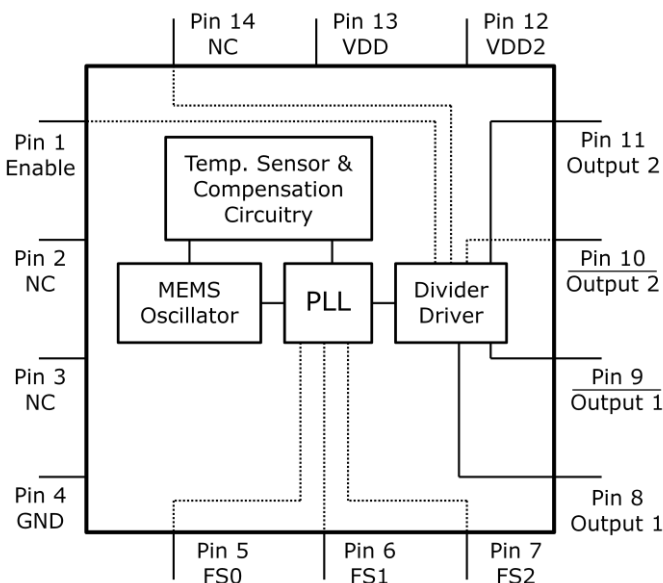
Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Two Independent Outputs**
  - LVPECL & LVDS
- **Pin-Selectable Configurations**
  - 3-bit Output Frequency Combinations
- **Wide Freq. Range**
  - LVPECL Output: 2.3 – 460 MHz
  - LVDS Output: 2.3 – 460 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

Block Diagram

Applications

- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	Leave unconnected or grounded
4	GND	Power	Ground
5	FS0	I	Least significant bit for frequency selection
6	FS1	I	Middle bit for frequency selection
7	FS2	I	Most significant bit for frequency selection
8	Output1+	O	Positive LVDS Output 1
9	Output1-	O	Negative LVDS Output 1
10	Output 2-	O	Negative LVPECL Output 2
11	Output 2+	O	Positive LVPECL Output 2
12	VDD2	Power	Power Supply 2 for LVDS Output 2
13	VDD	Power	Power Supply
14	NC	NA	Leave unconnected or grounded

Operational Description

The DSC2032 is a dual oscillator with an LVDS output and an LVPECL output. The device consists of a MEMS resonator and a support PLL IC. The two outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL. Two constraints are imposed on the output frequencies: 1) $f_2 = M \times f_1/N$, where M and N are even integers between 4 and 254, 2) $1.2\text{GHz} < N \times f_2 < 1.7\text{GHz}$.

The actual frequencies output by the DSC2032 are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to eight different frequency combinations. Three control pins (FS0 – FS2) select the output frequency combination. Discera supports customer defined versions of the DSC2032. Standard frequency options are described in in the following sections.

When Enable (pin 1) is floated or connected to VDD, the DSC2032 is in operational mode. Driving Enable to ground will tri-state both output drivers (hi-impedance mode).

Output Clock Frequencies

Table 1 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 1. Pre-programmed pin-selectable output frequency combinations

Ordering Info	Freq (MHz)	Freq Select Bits [FS2, FS1, FS0] – **Default is [111]**							
		000	001	010	011	100	101	110	**111**
L0001	f_{OUT1}	125	0*	0*	0*	0*	0*	0*	**125**
	f_{OUT2}	156.25	0*	0*	0*	0*	0*	0*	**156.25**
L0002	f_{OUT1}	125	125	0*	0*	0*	0*	0*	**0***
	f_{OUT2}	156.25	156.25	0*	0*	0*	0*	0*	**0***
LXXXXX	f_{OUT1}	Contact factory for additional configurations.							
	f_{OUT2}								

Frequency select bit are weakly tied high so if left unconnected the default setting will be [111] and the device will output the associated frequency highlighted in **Bold**.
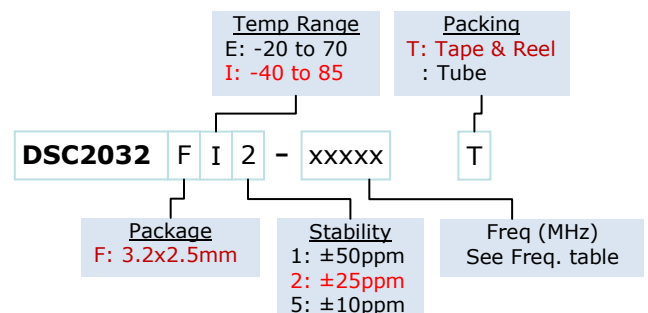0* – denotes invalid selection, output frequency is not specified.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Note: 1000+ years of data retention on internal memory

Ordering Code

Temp Range
E: -20 to 70
I: -40 to 85

Packing
T: Tape & Reel
 : Tube

DSC2032   F   I   2   –   xxxxx   T

Package
F: 3.2x2.5mm

Stability
1: ±50ppm
2: ±25ppm
5: ±10ppm

Freq (MHz)
See Freq. table

Specifications (Unless specified otherwise: T=25° C)

| Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current[2]	I_{DD}	EN pin high – outputs are enabled R_L=50Ω, F_{O1}= F_{O2}=156.25 MHz		64		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time[3]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	V_{IH} V_{IL}		0.75xV_{DD} -		- 0.25xV_{DD}	V
Output Disable Time[4]	t_{DA}				5	ns
Output Enable Time	t_{EN}				20	ns
Pull-Up Resistor[2]		Pull-up exists on all digital IO		40		kΩ
LVDS Outputs						
Output Offset Voltage		R=100Ω Differential	1.125		1.4	V
Delta Offset Voltage					50	mV
Pk to Pk Output Swing		Single-Ended		350		mV
Output Transition time[4] Rise Time Fall Time	t_R t_F	20% to 80% R_L=100Ω, C_L= 2pF		200	350	ps
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter[5]	J_{PER}	F_{O1}=F_{O2}=156.25 MHz		2.5		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	2	ps_{RMS}
LVPECL Outputs						
Output Logic Levels Output logic high Output logic low	V_{OH} V_{OL}	R_L=50Ω	V_{DD}-1.08 -		- V_{DD}-1.55	V
Pk to Pk Output Swing		Single-Ended		800		mV
Output Transition time[4] Rise Time Fall Time	t_R t_F	20% to 80% R_L=50Ω		250		ps
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter[5]	J_{PER}	F_{O1}=125 MHz		2.5		ps_{RMS}
Integrated Phase Noise	J_{CC}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	2	ps_{RMS}

Notes:
1. Pin 4 V_{DD} should be filtered with 0.01uf capacitor.
2. Output is enabled if Enable pad is floated or not connected.
3. t_{su} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
4. Output Waveform and Test Circuit figures below define the parameters.
5. Period Jitter includes crosstalk from adjacent output.

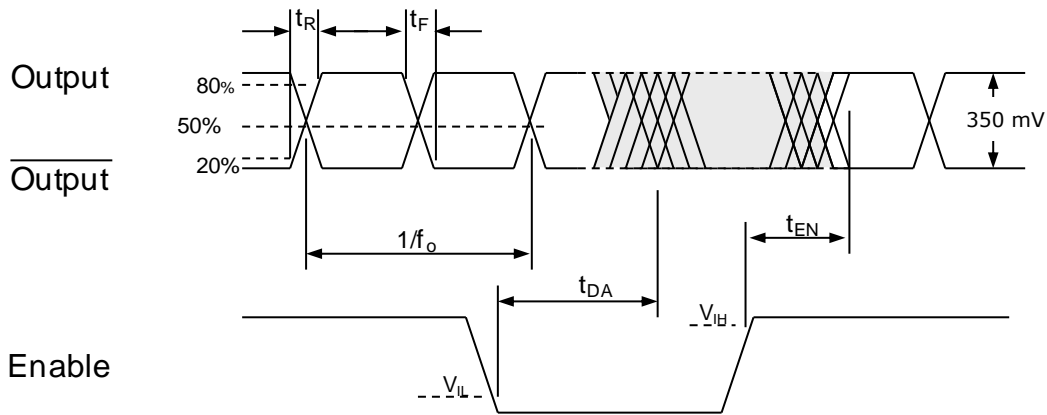# Nominal Performance Parameters (Unless specified otherwise: T=25° C, V$_{DD}$=3.3 V)
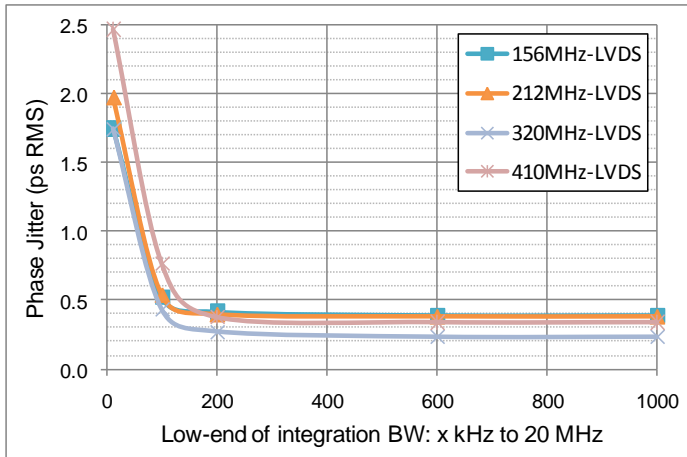
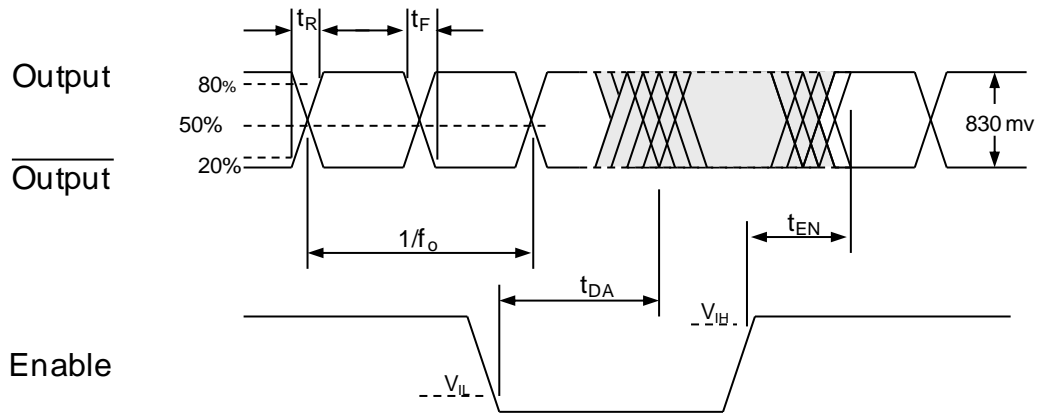LVDS Phase jitter (integrated phase noise)
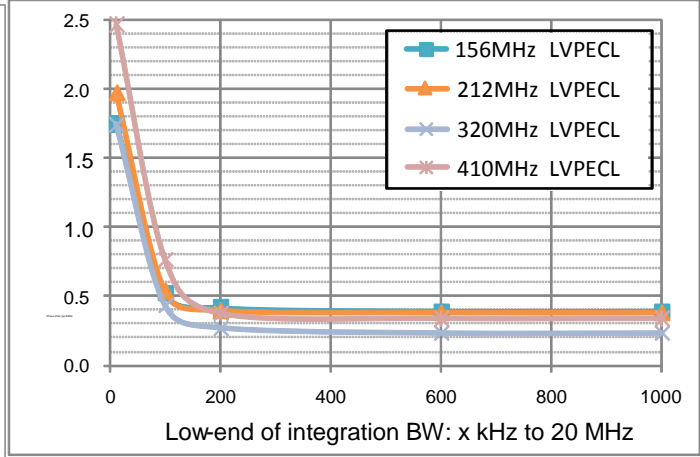
LVPECL Phase jitter (integrated phase noise)

Output Waveform: LVDS
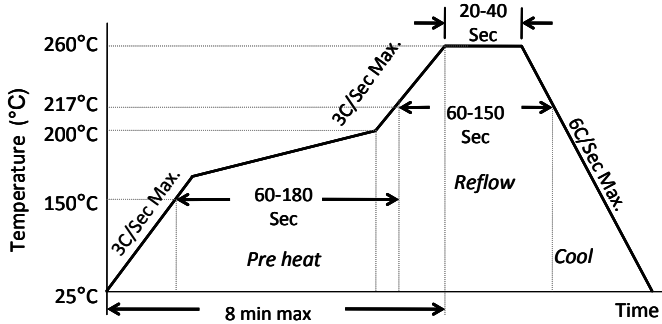

Output Waveform: LVPECL

Solder Reflow Profile

| MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Package Dimensions

3.2 x 2.5 mm 14 Lead Plastic Package

External Dimensions
units: mm[inch]
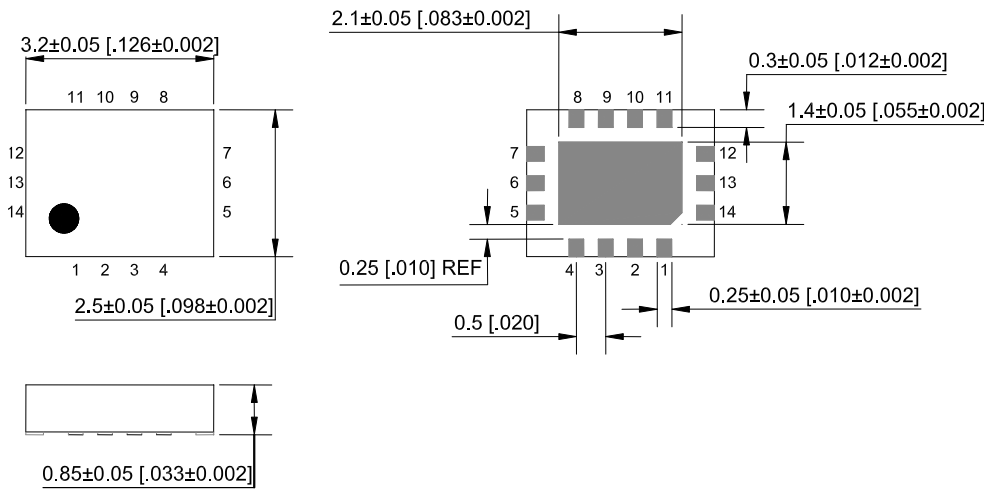
Recommended
Solder Pad Layout
units: mm[inch]
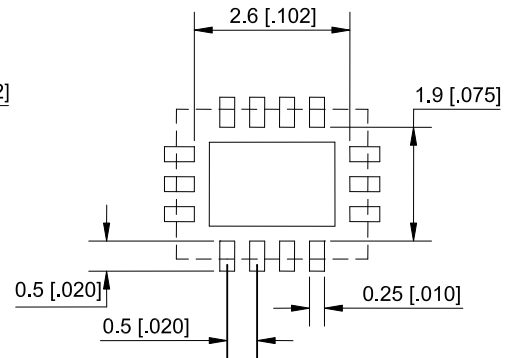
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DSC2032   Page 6   MK-Q-B-P-D-12042608-2