



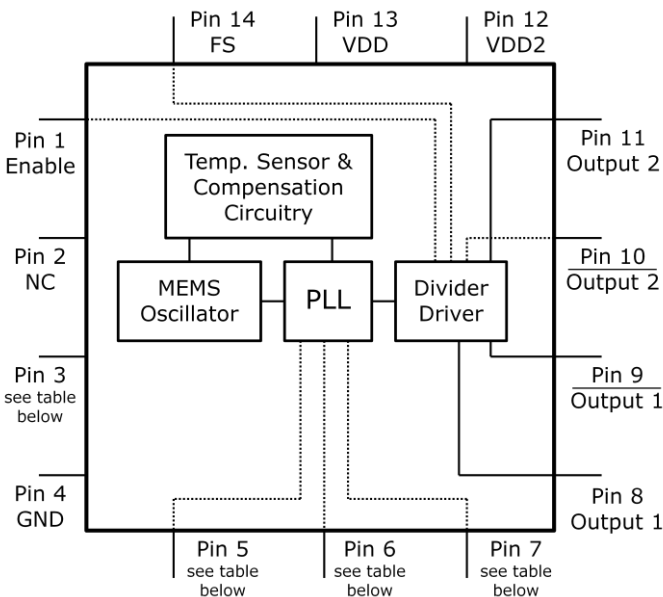
Low-Jitter I²C/SPI Programmable LVDS-LVPECL Oscillator

General Description

The DSC2132 and DSC2232 series of programmable, high-performance dual oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device flexibility. DSC2132 and DSC2232 allow the user to independently modify the frequency of each output using I²C or SPI interface, respectively. User can also select from two pre-programmed default output frequencies using the control pin.

DSC2132 and DSC2232 are packaged in 14-pin 3.2x2.5 mm QFN packages and available in temperature grades from Ext. Commercial to Industrial.

Block Diagram



Pin #	DSC2132 (I ² C)	DSC2232 (SPI)
3	NC	SCLK
5	SDA	MOSI
6	SCL	MISO
7	CS_bar	SS

Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±50 ppm**
- **Wide Temperature Range**
 - Industrial: -40° to 85° C
 - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Independent LVDS & LVPECL Outputs**
- **I²C/SPI Programmable Frequencies**
- **Wide Frequency Range:**
 - LVDS Output: 2.3 to 460 MHz
 - LVPECL Output: 2.3 to 460 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
 - Qualified to MIL-STD-883
- **High Reliability**
 - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

Applications

- **Storage Area Networks**
 - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
 - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
 - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	DSC2132: Leave unconnected or grounded
	SCLK	I	DSC2232: Serial clock from master
4	GND	Power	Ground
5	SDA	I	DSC2132: I ² C Serial Data
	MOSI		DSC2232: SPI Serial Data from Master to Slave
6	SCL	I	DSC2132: I ² C Serial Clock
	MISO	O	DSC2232: SPI Serial Data from Slave to Master
7	CS_bar	I	DSC2132: I ² C Chip Select (Active Low)
	SS	I	DSC2232: SPI Slave Select (Active Low)
8	Output1+	O	Positive LVDS Output 1
9	Output1-	O	Negative LVDS Output 1
10	Output 2-	O	Negative LVPECL Output 2
11	Output 2+	O	Positive LVPECL Output 2
12	VDD2	Power	Power Supply for LVDS Output
13	VDD	Power	Power Supply
14	FS	I	Default output clock frequency bit

Operational Description

The DSC2132/2232 is a dual oscillator with an LVPECL output and an LVDS output. The device consists of a MEMS resonator and a support PLL IC. The outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL.

DSC2132/2232 allows for easy programming of the output frequencies using I²C/SPI interface. Upon power-up, the initial output frequencies are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for two different default frequency pairs. The

control pin (FS) selects the initial pair. Once the device is powered up, a new output frequency pair can be programmed. Programming details are provided in the **Programming Guide**. Standard default frequency pairs are described in the following sections. Discera supports customer defined versions of the DSC2132/22332.

When Enable (pin 1) is floated or connected to VDD, the DSC2132/2232 is in operational mode. Driving Enable to ground will tri-state both output drivers (hi-impedance mode).

Output Clock Frequencies

Table 1 lists the standard default frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 1. Pre-programmed pin-selectable output frequency pairs

Ordering Info	Freq (MHz)	Select Bit [FS] – Default is [1]	
		0	1
L0001	f _{OUT1}	125	0*
	f _{OUT2}	156.25	0*
L0002	f _{OUT1}	125	156.25
	f _{OUT2}	156.25	156.25
LXXXX	f _{OUT1}	Contact factory for additional configurations.	
	f _{OUT2}		

Frequency select bit are weakly tied high so if left unconnected the default setting will be [1] and the device will output the associated frequency highlighted in **Bold**.

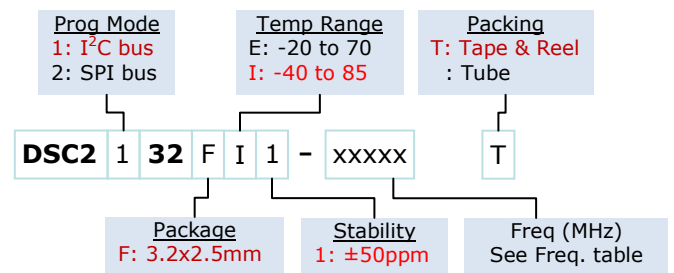
0* – denotes invalid selection, output frequency is not specified.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V _{DD} +0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Note: 1000+ years of data retention on internal memory

Ordering Code



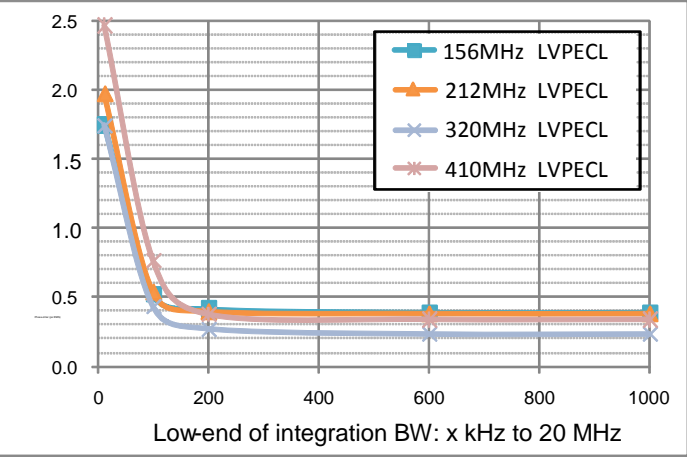
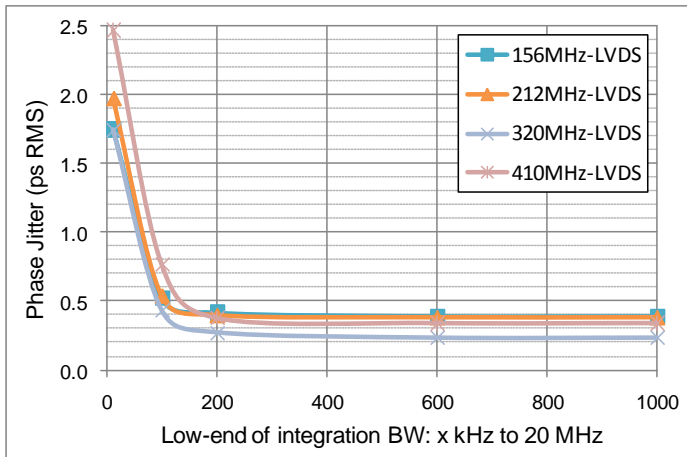
Specifications (Unless specified otherwise: T=25° C)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage ¹	V _{DD}		2.25		3.6	V
Supply Current	I _{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current ²	I _{DD}	EN pin high – outputs are enabled R _L =50Ω, F _{O1} =F _{O2} =156.25 MHz		64		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time ³	t _{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	V _{IH} V _{IL}		0.75xV _{DD} -		- 0.25xV _{DD}	V
Output Disable Time ⁴	t _{DA}				5	ns
Output Enable Time	t _{EN}				20	ns
Pull-Up Resistor ²		Pull-up exists on all digital IO		40		kΩ
LVDS Output						
Output Offset Voltage		R=100Ω Differential	1.125		1.4	V
Delta Offset Voltage					50	mV
Pk to Pk Output Swing		Single-Ended		350		mV
Output Transition time ⁴ Rise Time Fall Time	t _R t _F	20% to 80% R _L =50Ω, C _L = 2pF		200		ps
Frequency	f ₀	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	J _{PER}	F _{O1} =F _{O2} =156.25 MHz		2.5		ps _{RMS}
Integrated Phase Noise	J _{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	2	ps _{RMS}
LVPECL Output						
Output Logic Levels Output logic high Output logic low	V _{OH} V _{OL}	R _L =50Ω	V _{DD} -1.08 -		- V _{DD} -1.55	V
Pk to Pk Output Swing		Single-Ended		800		mV
Output Transition time ⁴ Rise Time Fall Time	t _R t _F	20% to 80% R _L =50Ω		250		ps
Frequency	f ₀	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	J _{PER}	F _{O1} =F _{O2} =156.25 MHz		2.5		ps _{RMS}
Integrated Phase Noise	J _{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	2	ps _{RMS}

Notes:

1. Pin 4 V_{DD} should be filtered with 0.01uF capacitor.
2. Output is enabled if Enable pad is floated or not connected.
3. t_{SU} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
4. Output Waveform and Test Circuit figures below define the parameters.
5. Period Jitter includes crosstalk from adjacent output.

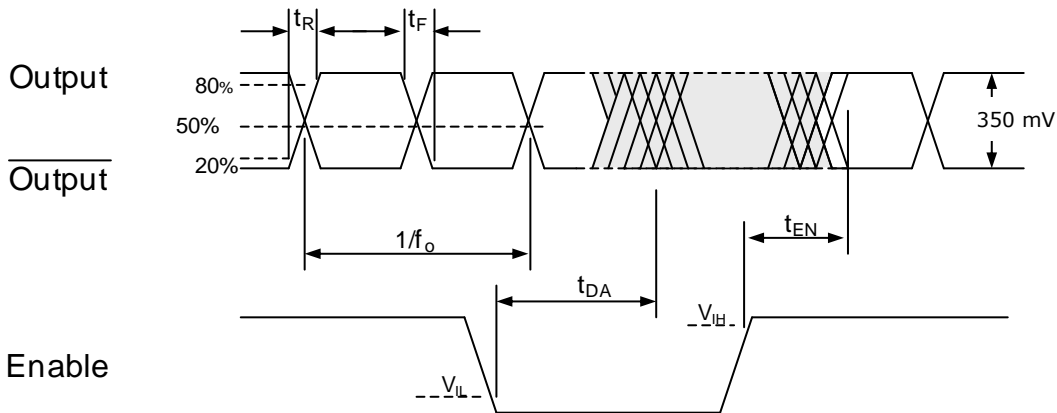
Nominal Performance Parameters (Unless specified otherwise: T=25° C, V_{DD}=3.3 V)



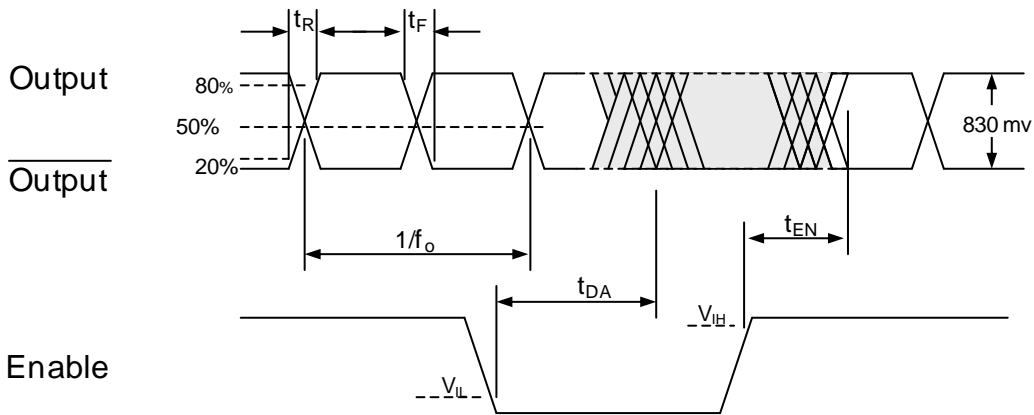
LVDS Phase jitter (integrated phase noise)

LVPECL Phase jitter (integrated phase noise)

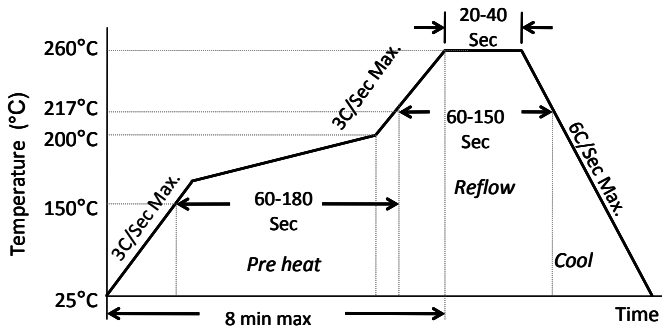
Output Waveform: LVDS



Output Waveform: LVPECL



Solder Reflow Profile



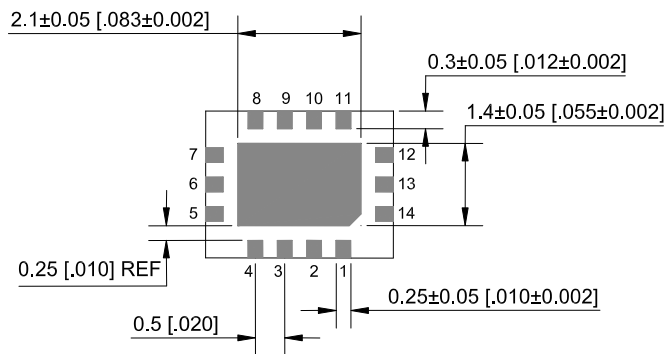
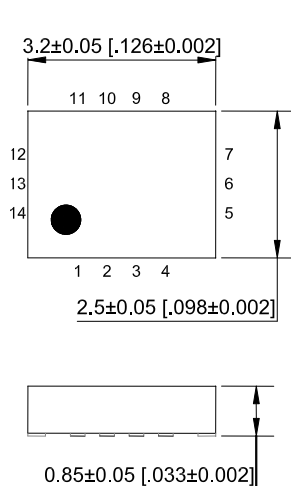
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Package Dimensions

3.2 x 2.5 mm 14 Lead Plastic Package

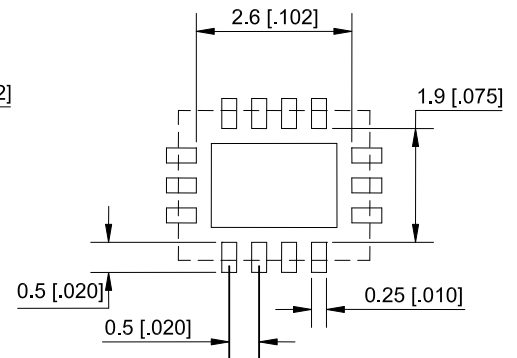
External Dimensions

units: mm[inch]



Recommended Solder Pad Layout

units: mm[inch]



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