DSC2141 | DSC2241

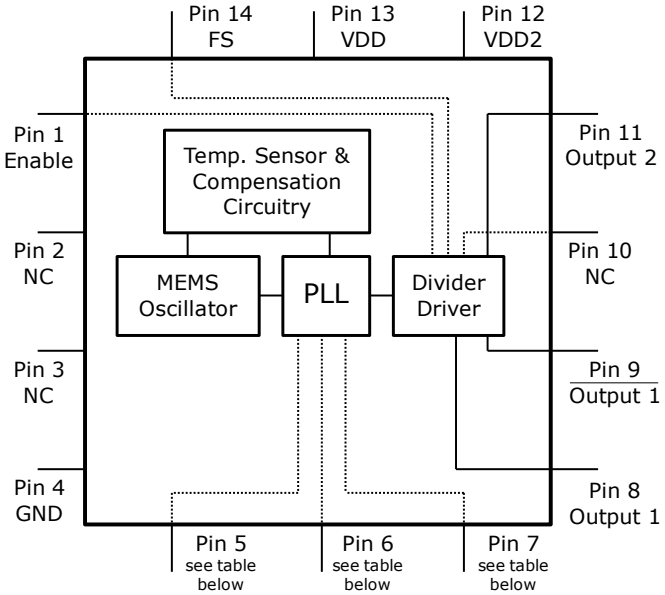
Low-Jitter I²C/SPI Programmable Dual HCSL-CMOS Oscillator

General Description

The DSC2141 and DS2241 series of programmable, high-performance oscillators with HCSL & CMOS outputs utilize a proven silicon MEMS technology to provide excellent jitter and stability while incorporating high output frequency flexibility. DSC2141 and DSC2241 allow the user to independently modify the frequency of each output using I2C or SPI interface, respectively. User can also select from two pre-programmed default output frequencies using the control pin.

DSC2141 and DSC2241 are packaged in 14-pin 3.2x2.5 mm QFN packages and available in temperature grades from Ext. Commercial to Industrial.

Block Diagram



Pin #	DSC2141 (I²C)	DSC2241 (SPI)
3	NC	SCLK
5	SDA	MOSI
6	SCL	MISO
7	CS_bar	SS

Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±50 ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Two Independent Outputs**
  - HCSL and CMOS
- **I²C/SPI Programmable Frequencies**
- **Wide Frequency Range: 10 to 460 MHz**
  - HCSL Output: 2.3 to 460 MHz
  - CMOS Output: 2.3 to 170 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

Applications

- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	DSC2141: Leave unconnected or grounded
	SCLK	I	DSC2241: Serial clock from master
4	GND	Power	Ground
5	SDA	I	DSC2141: I²C Serial Data
	MOSI		DSC2241: SPI Serial Data from Master to Slave
6	SCL	I	DSC2141: I²C Serial Clock
	MISO	O	DSC2241: SPI Serial Data from Slave to Master
7	CS_bar	I	DSC2141: I²C Chip Select (Active Low)
	SS	I	DSC2241: SPI Slave Select (Active Low)
8	Output1+	O	Positive HCSL Output 1
9	Output1-	O	Negative HCSL Output 1
10	NC	NA	Leave unconnected or grounded
11	Output 2	O	CMOS Output
12	VDD2	Power	Power Supply for CMOS Output
13	VDD	Power	Power Supply
14	FS	I	Default output clock frequency bit

Operational Description

The DSC2141/2241 is a dual output HCSL – CMOS oscillator consisting of a MEMS resonator and a support PLL IC. The outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL.

DSC2141/2241 allows for easy programming of the output frequencies using I²C/SPI interface. Upon power-up, the initial output frequencies are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for two different default frequency pairs. The control pin (FS) selects the initial pair. Once the device is powered up, a new output frequency pair can be programmed. Programming details are provided in the ***Programming Guide***. Standard default frequency pairs are described in the following sections.

When Enable (pin 1) is floated or connected to VDD, the DSC2141/2241 is in operational mode. Driving Enable to ground will tri-state both output drivers (hi-impedance mode).

Output Clock Frequencies

Table 1 lists the standard default frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 1. Pre-programmed pin-selectable output frequency pairs

Ordering Info	Freq (MHz)	Select Bit [FS] – **Default is [1]**	
		0	**1**
K0001	f_{OUT1}	50	**156.25**
	f_{OUT2}	25	**25**
KXXXX	f_{OUT1}	Contact factory for additional configurations.	
	f_{OUT2}		

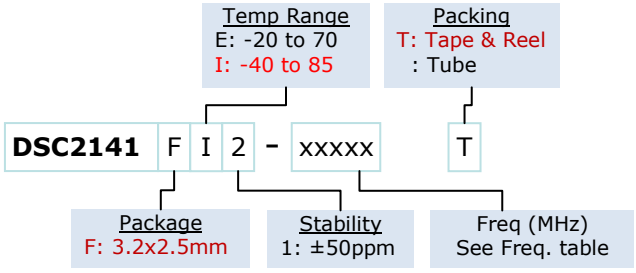
Frequency select bit are weakly tied high so if left unconnected the default setting will be [1] and the device will output the associated frequency highlighted in **Bold**.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Note: 1000+ years of data retention on internal memory

Ordering Code

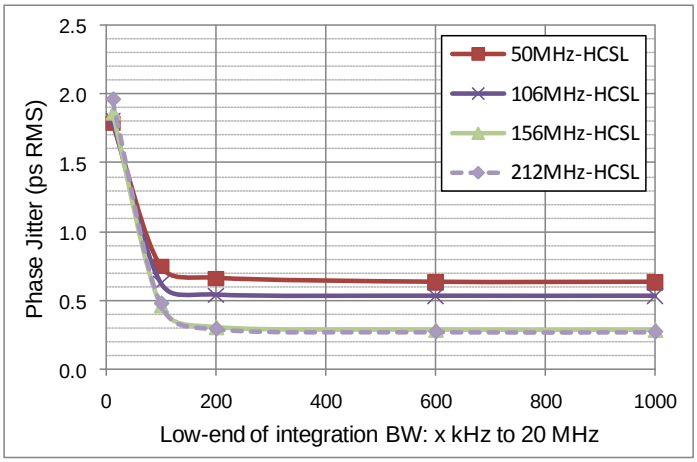


Specifications (Unless specified otherwise: T=25° C)

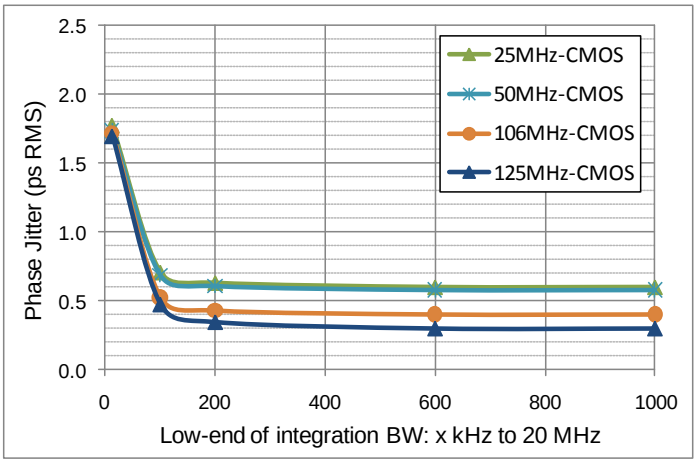
Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current[2]	I_{DD}	EN pin high – outputs are enabled HCSL: R_L=50Ω, F_{O1} =125 MHz CMOS: CL=15pf, F_{O1} =75 MHz		49		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time[3]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[4]	t_{DA}				5	ns
Output Enable Time	t_{EN}				20	ns
Pull-Up Resistor[2]		Pull-up exists on all digital IO		40		kΩ
HCSL Output						
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	R_L=50Ω	 0.725 -		 - 0.1	V
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time[4] Rise Time Fall Time	 t_R t_F	20% to 80% R_L=50Ω, C_L= 2pF	200		400	ps
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter[5]	J_{PER}	F_{O1}=F_{O2}=156.25 MHz		2.8		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.37 1.7	 2	ps_{RMS}
CMOS Output						
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	I=±6mA	 0.9xV_{DD} -		 - 0.1xV_{DD}	V
Output Transition time[4] Rise Time Fall Time	 t_R t_F	20% to 80% C_L=15pf		 1.1 1.3	 2 2	ns
Frequency	f_0	Commercial/Industrial temp range	2.3		170	MHz
Output Duty Cycle	SYM		45		55	%
Period Jitter[5]	J_{PER}	F_{O2}=125 MHz		3		ps_{RMS}
Integrated Phase Noise	J_{CC}	200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz		0.3 0.38 1.7	 2	ps_{RMS}

Notes:
1. Pin 4 V_{DD} should be filtered with 0.01uf capacitor.
2. Output is enabled if Enable pad is floated or not connected.
3. t_{su} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
4. Output Waveform and Test Circuit figures below define the parameters.
5. Period Jitter includes crosstalk from adjacent output.

Nominal Performance Parameters (Unless specified otherwise: T=25° C, V_{DD}=3.3 V)

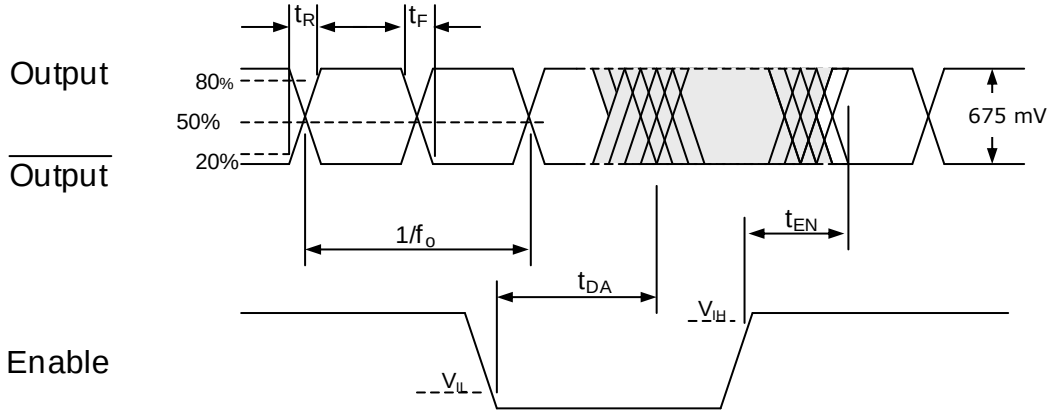


HCSL Phase jitter (integrated phase noise)

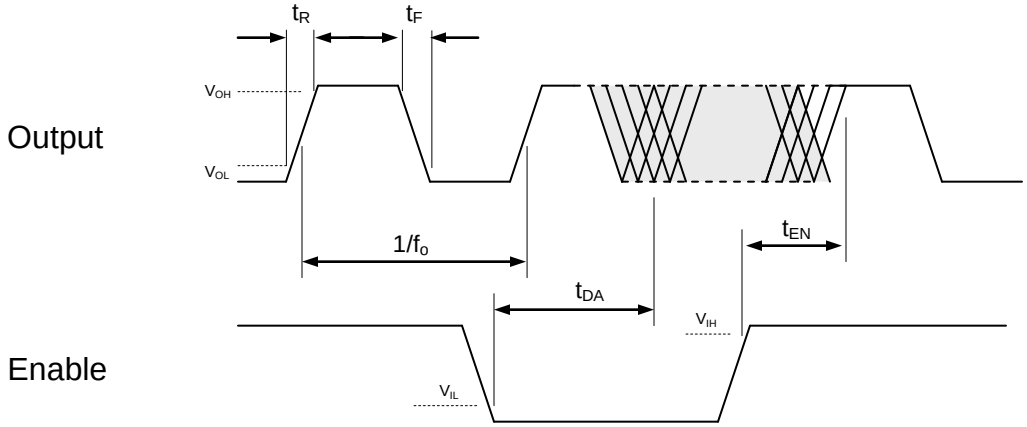


CMOS Phase jitter (integrated phase noise)

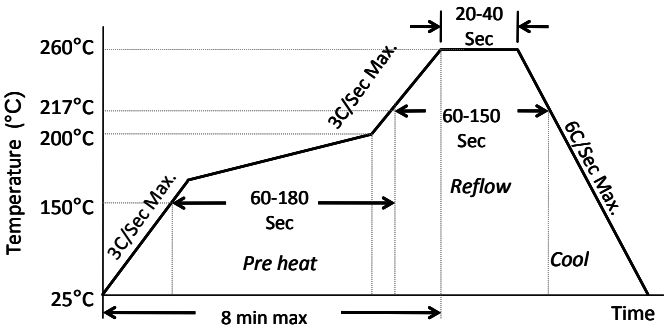
Output Waveform: HCSL



Output Waveform: CMOS



Solder Reflow Profile



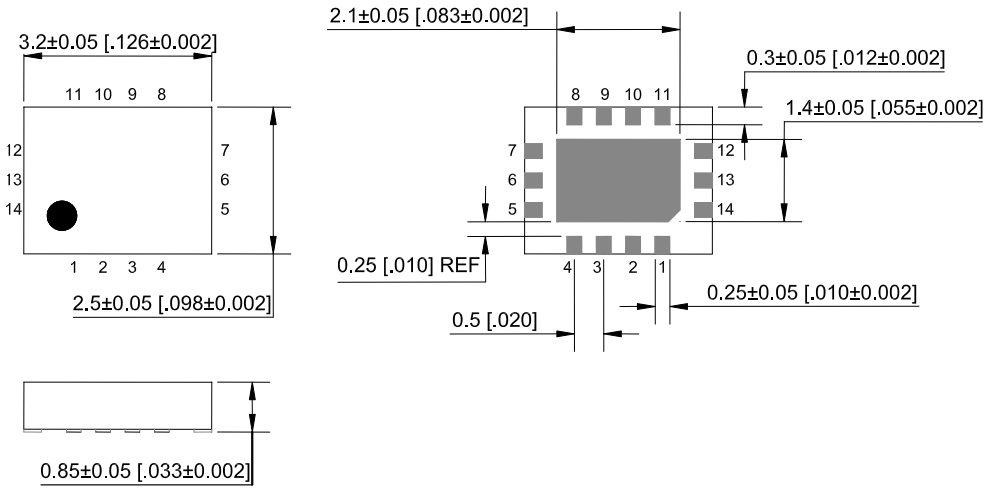
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Package Dimensions

3.2 x 2.5 mm 14 Lead Plastic Package

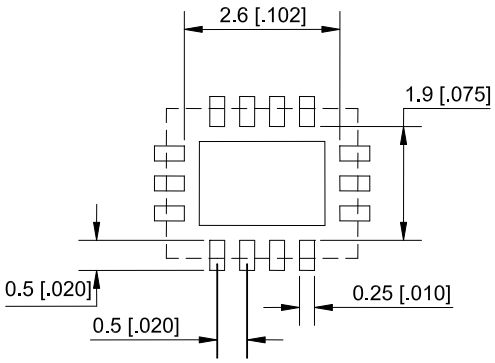
External Dimensions

units: mm[inch]



Recommended Solder Pad Layout

units: mm[inch]



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