



Crystal-less™ Four Output 56.6MHz Clock Generator

General Description

The DSC511-05 is a Crystal-less™, four output clock generator. The clock generator uses proven silicon MEMS technology to provide 56.6MHz at each output with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, MEMS clock generators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

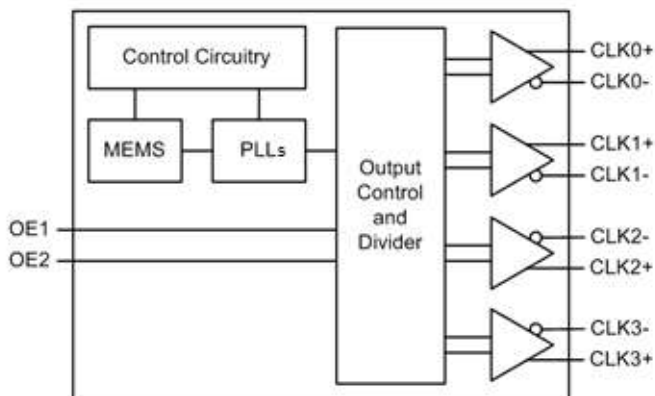
DSC511-05 has input pins OE1 and OE2 for Output Enable / Disable feature allowing it to disable all outputs when OE(1:2) = 0. Each output enable pin controls a bank of two synchronous XAUI clocks. See the OE function table 1 for more detail.

The device is available in a 20 pin QFN. Output formats are available in any combination of LVPECL, LVDS, HCSL and LVCMOS

Features

- **Available Output Formats:**
 - HCSL, LVPECL, LVDS or LVCMOS per output
- **Wide Temperature Range**
 - Ext. Industrial: -40° to 105° C
 - Industrial: -40° to 85° C
 - Ext. commercial: -20° to 70° C
- **Supply Range of 2.25 to 3.6 V**
- **Low Power Consumption**
 - 30% lower than competing devices
- **Excellent Shock & Vibration Immunity**
 - Qualified to MIL-STD-883
- **Package:**
 - 20 QFN, 5mm x 3.2mm
- **Lead Free & RoHS Compliant**
- **Short Lead Time: 2 Weeks**
- **AEC-Q100 Automotive Qualified**

Block Diagram



* Clk0+/-, Clk1+/-, Clk2 +/- and Clk3 +/- are 56.6 MHz. For other frequencies, please contact the factory.

Applications

- **Communications/Networking**
 - Ethernet
 - 1G, 10GBASE-T/KR/LR/SR, and FcoE
 - Routers and Switches
 - Gateways, VoIP, Wireless AP's
 - Passive Optical Networks
- **Embedded Applications**

Specifications (Unless specified otherwise: T=25° C, VDD =3.3V)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage ¹	V _{DD}		2.25		3.6	V
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±100	ppm
					±50	
Startup Time ³	t _{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	V _{IH} V _{IL}		0.75xV _{DD} -		- 0.25xV _{DD}	V
Output Disable Time ⁴	t _{DA}				5	ns
Output Enable Time	t _{EN}				20	ns
Pull-Up Resistor ²		Pull-up on OE pin		40		kΩ

Parameter		Condition	Min.	Typ.	Max.	Unit
LVDS Outputs						
Supply Current ² (All LVDS outputs)	I _{DD}	All outputs running at 56.6MHz, R _L =100Ω		110	TBD	mA
		All outputs disabled		29	TBD	
Output offset Voltage	V _{OS}	R _L =100Ω Differential	1.125		1.4	V
Delta Offset Voltage	ΔV _{OS}				50	mV
Pk to Pk Output Swing	V _{PP}	Single-Ended		350		mV
Output Transition time ³ Rise Time Fall Time	t _R t _F	20% to 80% R _L =100Ω, C _L = 2pF		200	TBD	ps
Frequency	f ₀	At any output	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter	J _{PER}			2.5		ps _{RMS}
Integrated Phase Noise	J _{PH}	200kHz to 20MHz @56.6MHz 100kHz to 20MHz @56.6MHz 12kHz to 20MHz @56.6MHz		1.7	TBD TBD 2	ps _{RMS}

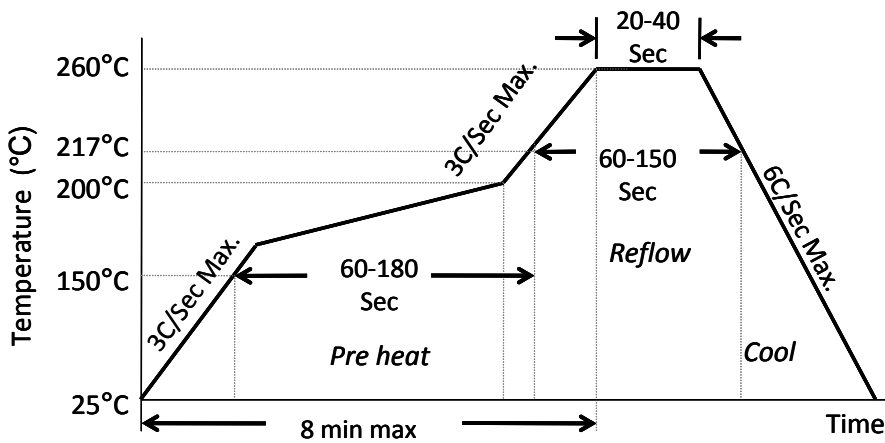
Notes:

- VDD pins 9 and 19 should be filtered with 0.1uf capacitor.
- t_{SU} is setup time to achieve 100ppm at output frequency after V_{DD} is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Output is enabled if OE pin is floated or not connected.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Solder Reflow Profile

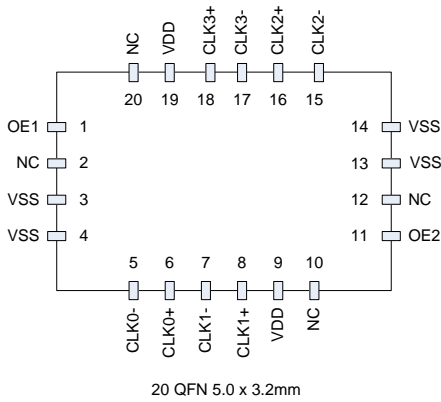


20 QFN MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

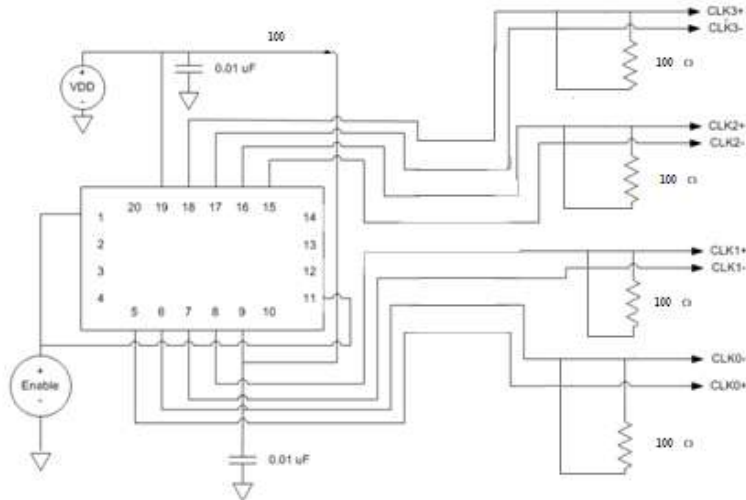
Pin Description (20 QFN)

Pin No.	Pin Name	Pin Type	Description
1	OE1	I	Output Enable; active high
2	NC	NA	Leave unconnected or grounded
3	VSS	Power	Ground
4	VSS	Power	Ground
5	CLK0-	O	Complement output of differential pair (56.6MHz)
6	CLK0+	O	True output of differential pair (56.6MHz)
7	CLK1-	O	Complement output of differential pair (56.6MHz)
8	CLK1+	O	True output of differential pair (56.6MHz)
9	VDD	Power	Power Supply
10	NC	NA	Leave unconnected or grounded
11	OE2	I	Output Enable; active high
12	NC	NA	Leave unconnected or grounded
13	VSS	Power	Ground
14	VSS	Power	Ground
15	CLK2-	O	Complement output of differential pair (56.6MHz)
16	CLK2+	O	True output of differential pair (56.6MHz)
17	CLK3-	O	Complement output of differential pair (56.6MHz)
18	CLK3+	O	True output of differential pair (56.6MHz)
19	VDD	Power	Power Supply
20	NC	NA	Leave unconnected or grounded

Pin Diagram (20 QFN)



Connection Diagram (20 QFN, Four LVDS Outputs)



OE Function and Output Waveform: LVDS

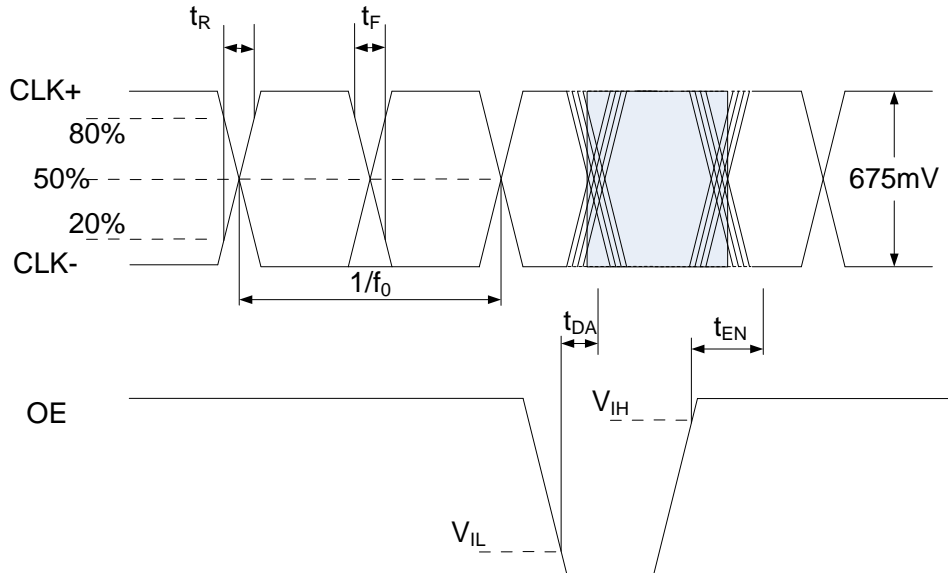
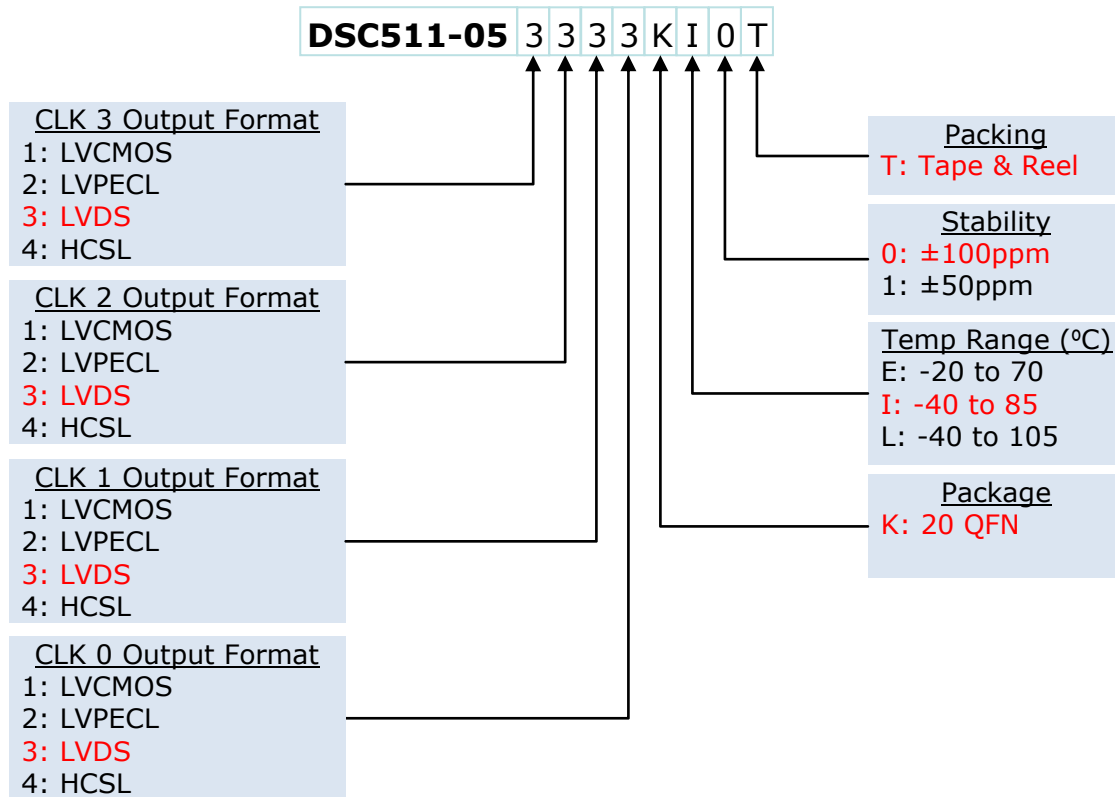


Table 1: output enable select table

CLK1/CLK2 are synchronous					
OE1	OE2	CLK0	CLK1	CLK2	CLK3
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	EN	EN	Hi-Z
1	0	EN	Hi-Z	Hi-Z	EN
1	1	EN	EN	EN	EN

CLK0/CLK3 are synchronous

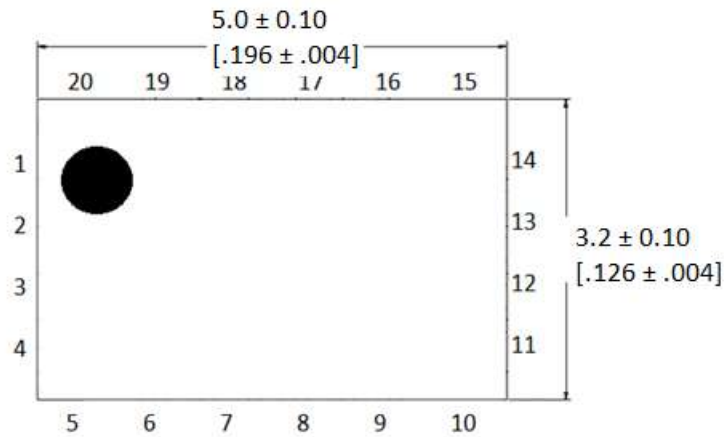
Ordering Information



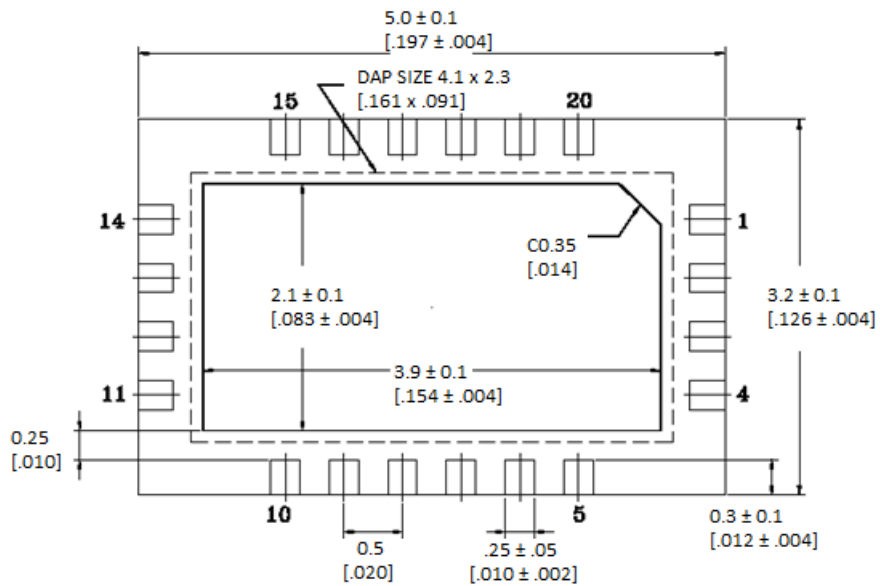
Package Dimensions

20 QFN, 5.0 x 3.2 mm

Top View units: mm[inches]



Bottom View units: mm[inches]±

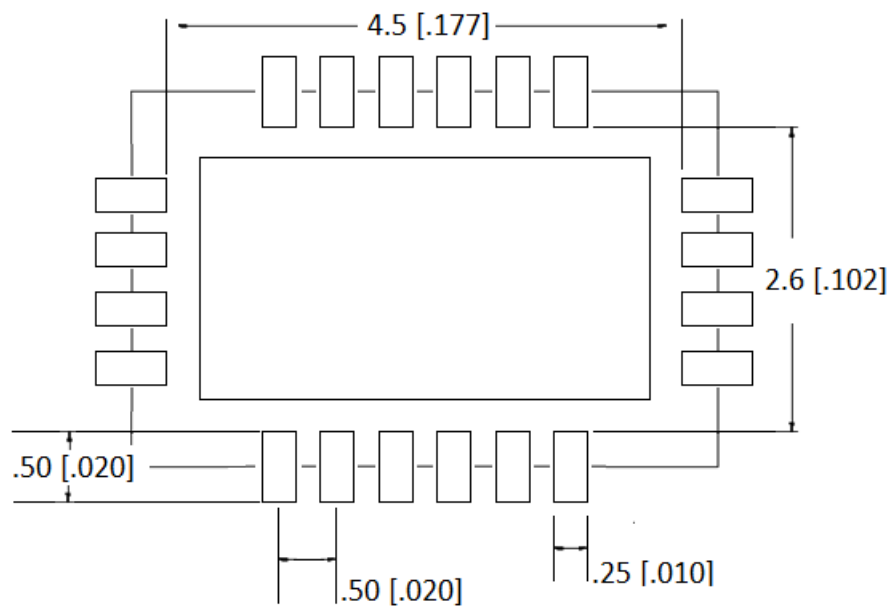


Side View
units: mm[inches]



Recommended Solder Pad Layout

units: mm[inches]



*Connect the center pad to VSS for best thermal performance

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