DSC513-05

Crystal-less™ Four Output 200 MHz Clock Generator

General Description

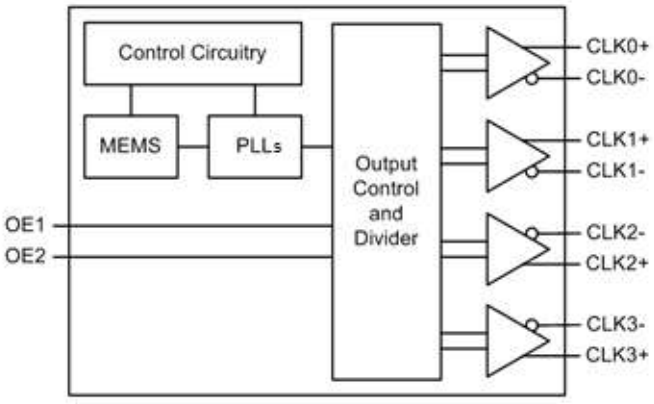
The DSC513-05 is a Crystal-less™, four output clock generator. The clock generator uses proven silicon MEMS technology to provide 200 MHz at each output with excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the external quartz crystal, MEMS clock generators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC513-05 has input pins OE1 and OE2 for Output Enable / Disable feature allowing it to disable all outputs when OE(1:2) = 0. Each output enable pin controls a bank of two synchronous clocks.See the OE function table 1 for more detail.
The device is available in a 20 pin QFN. Output formats are available in any combination of LVPECL, LVDS, HCSL and LVCMOS

Features

- **Available Output Formats:**
  - HCSL, LVPECL, LVDS or LVCMOS per output
- **Wide Temperature Range**
  - Ext. Industrial: -40° to 105° C
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **Supply Range of 2.25 to 3.6 V**
- **Low Power Consumption**
  - 30% lower than competing devices
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **Package:**
  - 20 QFN, 5mm x 3.2mm
- **Lead Free & RoHS Compliant**
- **Short Lead Time: 2 Weeks**
- **AEC-Q100 Automotive Qualified**

Block Diagram



* Clk0+/-, Clk1+/-, Clk2 +/- and Clk3 +/- are 200 MHz. For other frequencies, please contact the factory.

Applications

- **Communications/Networking**
  - **Ethernet**
  - **1G, 10GBASE-T/KR/LR/SR, and FcoE**
  - **Routers and Switches**
  - **Gateways, VoIP, Wireless AP's**
  - **Passive Optical Networks**
- **Embedded Applications**

Specifications (Unless specified otherwise: T=25° C, VDD =3.3V)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±100 ±50	ppm
Startup Time[3]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[4]	t_{DA}				5	ns
Output Enable Time	t_{EN}				20	ns
Pull-Up Resistor[2]		Pull-up on OE pin		40		kΩ

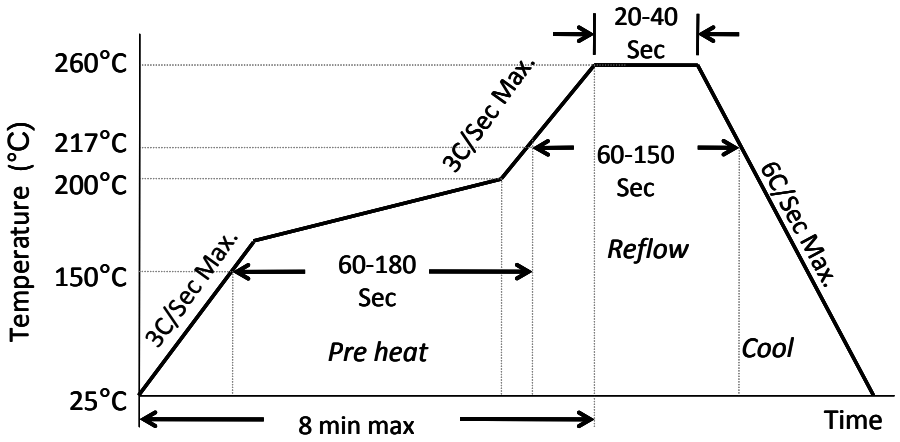
Parameter		Condition	Min.	Typ.	Max.	Unit
LVDS Outputs						
Supply Current[2] (All LVDS outputs)	I_{DD}	All outputs running at 200MHz, R_L=100Ω		110	TBD	mA
		All outputs disabled		29	TBD	
Output offset Voltage	V_{OS}	R_L =100Ω Differential	1.125		1.4	V
Delta Offset Voltage	ΔV_{OS}				50	mV
Pk to Pk Output Swing	V_{PP}	Single-Ended		350		mV
Output Transition time[3] Rise Time Fall Time	 t_R t_F	20% to 80% R_L=100Ω, C_L= 2pF		200	TBD	ps
Frequency	f_0	At any output	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter	J_{PER}			2.5		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @ 200 MHz 100kHz to 20MHz @ 200 MHz 12kHz to 20MHz @ 200 MHz		 1.7	TBD TBD 2	ps_{RMS}

Notes:
1. VDD pins 9 and 19 should be filtered with 0.1uf capacitor.
2. t_{su} is setup time to achieve 100ppm at output frequency after V_{DD} is applied and outputs are enabled.
3. Output Waveform and Test Circuit figures below define the parameters.
4. Output is enabled if OE pin is floated or not connected.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Solder Reflow Profile

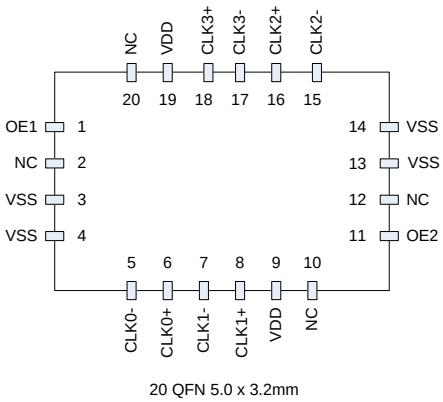


20 QFN MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Pin Description (20 QFN)

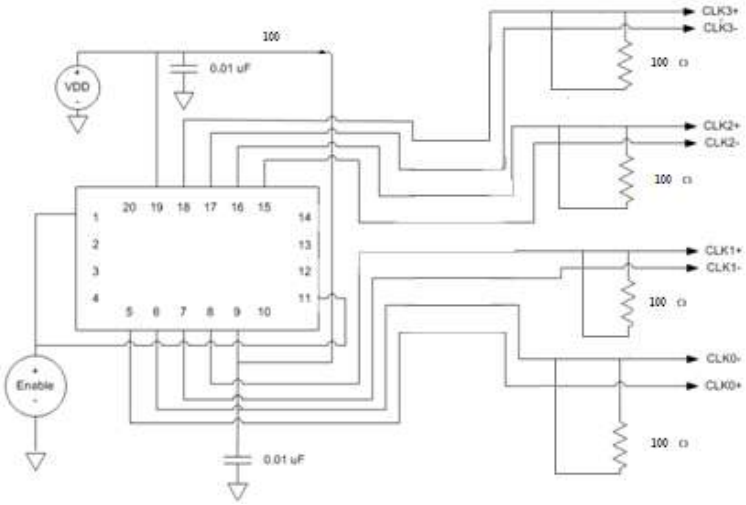
Pin No.	Pin Name	Pin Type	Description
1	OE1	I	Output Enable; active high
2	NC	NA	Leave unconnected or grounded
3	VSS	Power	Ground
4	VSS	Power	Ground
5	CLK0-	O	Complement output of differential pair (200MHz)
6	CLK0+	O	True output of differential pair (200MHz)
7	CLK1-	O	Complement output of differential pair (200MHz)
8	CLK1+	O	True output of differential pair (200MHz)
9	VDD	Power	Power Supply
10	NC	NA	Leave unconnected or grounded
11	OE2	I	Output Enable; active high
12	NC	NA	Leave unconnected or grounded
13	VSS	Power	Ground
14	VSS	Power	Ground
15	CLK2-	O	Complement output of differential pair (200MHz)
16	CLK2+	O	True output of differential pair (200MHz)
17	CLK3-	O	Complement output of differential pair (200MHz)
18	CLK3+	O	True output of differential pair (200MHz)
19	VDD	Power	Power Supply
20	NC	NA	Leave unconnected or grounded

Pin Diagram (20 QFN)



20 QFN 5.0 x 3.2mm

Connection Diagram (20 QFN, Four LVDS Outputs)



OE Function and Output Waveform: LVDS

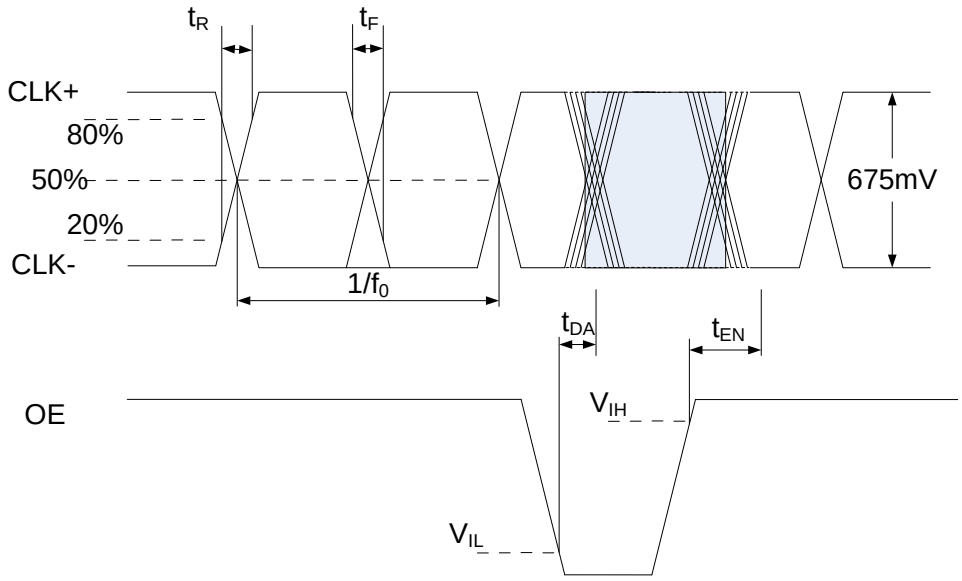


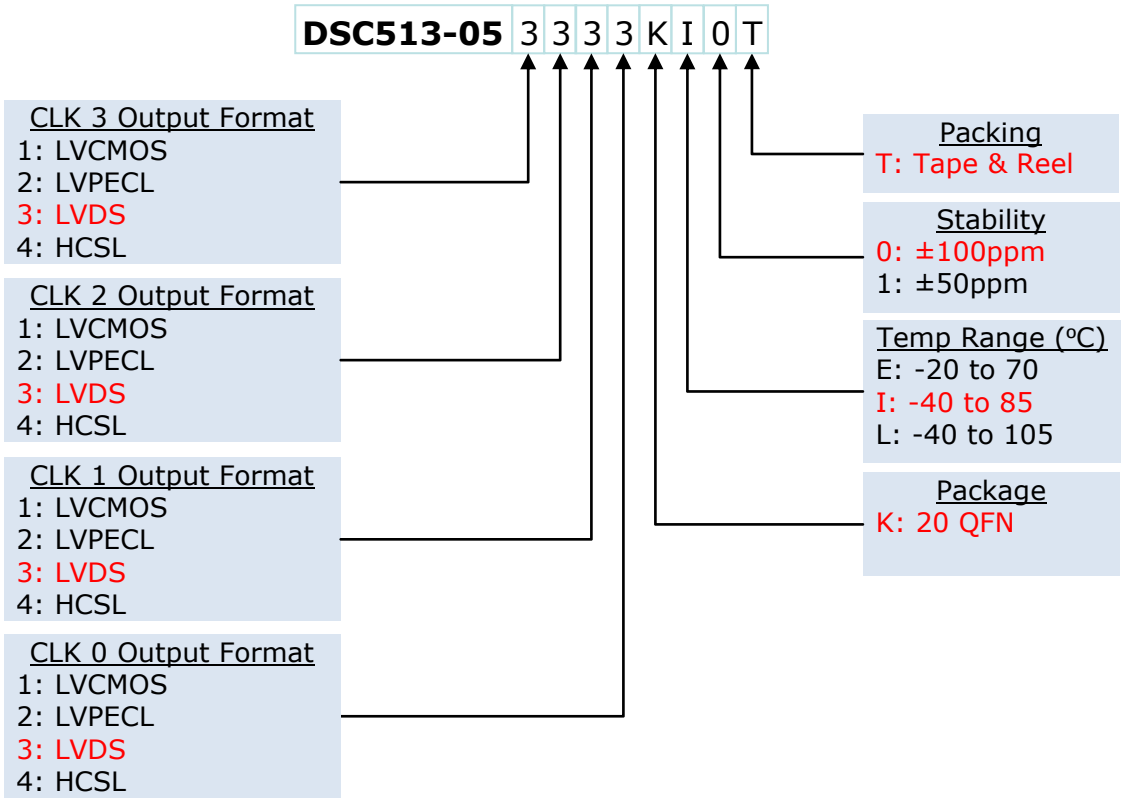
Table 1: output enable select table

CLK1/CLK2 are synchronous

OE1	OE2	CLK0	CLK1	CLK2	CLK3
0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	Hi-Z	EN	EN	Hi-Z
1	0	EN	Hi-Z	Hi-Z	EN
1	1	EN	EN	EN	EN

CLK0/CLK3 are synchronous

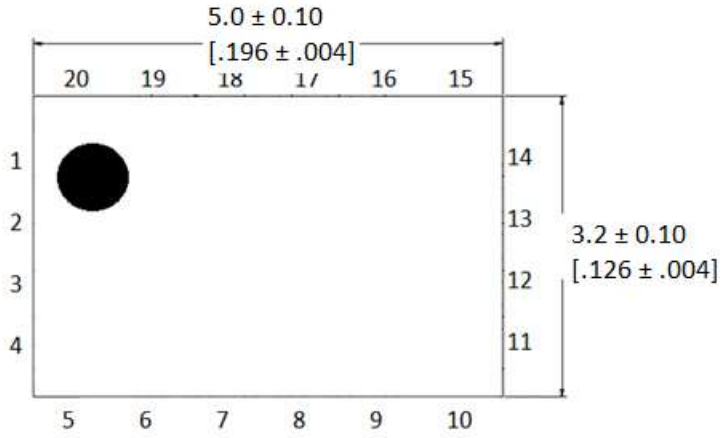
Ordering Information



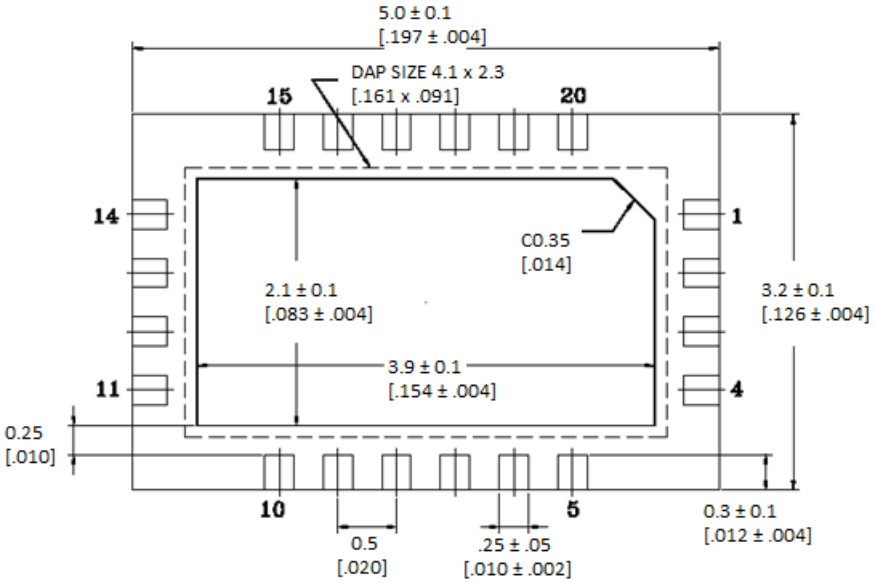
Package Dimensions

20 QFN, 5.0 x 3.2 mm

Top View
units: mm[inches]



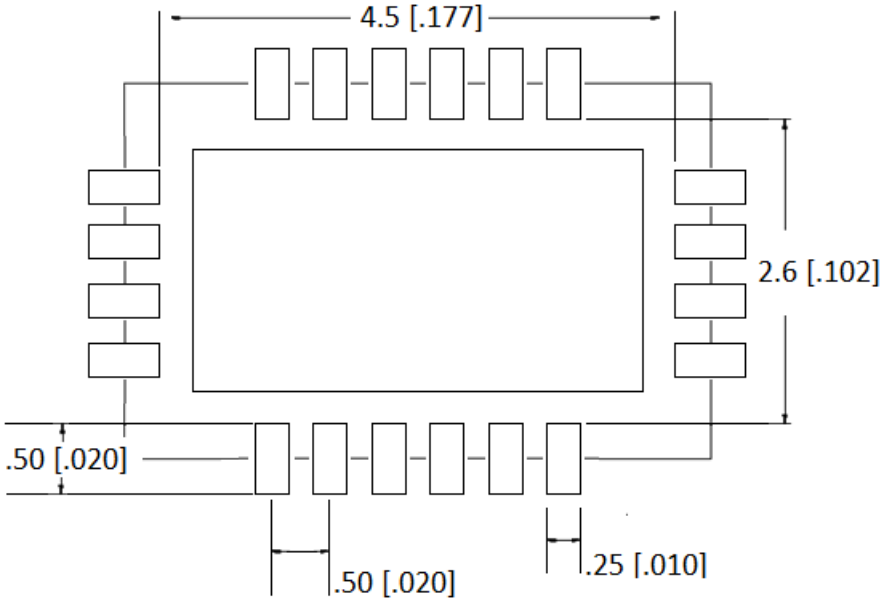
Bottom View
units: mm[inches]±



Side View
units: mm[inches]

Recommended Solder Pad Layout

units: mm[inches]



*Connect the center pad to VSS for best thermal performance

Disclaimer:

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