Appendix A

Instruction Set Encoding

APPENDIX A. INSTRUCTION SET ENCODING

CONTENTS

A. INSTRUCTION SET ENCODING

This appendix defines the hardware-level encoding of the DSP16/DSP16A device instructions.

A.1 FORMATS

Multiply/ALU Instructions

Format 1: Multiply/ALU Read/Write Group.

Field	T					D	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 1a: Multiply/ALU Read/Write Group.

Field	T					$\overline{aT}$	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2: Multiply/ALU Read/Write Group.

Field	T					D	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2a: Multiply/ALU Read/Write Group.

Field	T					$\overline{aT}$	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Special Function Instructions

Format 3: Special Functions.

Field	T					D	S	F2				CON				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Control Instructions

Format 4: Branch Direct Group.

Field	T1				JA											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 5: Branch Indirect Group.

Field	T					B										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 6: Conditional Branch Qualifier/Software Interrupt (icall).
Note that a branch instruction immediately follows except
for a software interrupt (icall).

Field	T					SI					C					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Data Move Instructions

Format 7: Data Move Group.

Field	T					D	R					Y/Z				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 7a: Data Move Group.

Field	T					$\overline{aT}$	R					Y				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Format 8: Data Move (Immediate Operand – 2 words).

Field	T					D	R					Y			
	Immediate Operand (N)														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 9: Short Immediate Group.

Field	T					I	Short Immediate Operand (M)								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Cache Instructions

Format 10: Do – Redo.

Field	T					NI				K						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

A.2 REPLACEMENT TABLES FOR FORMAT FIELDS

Field Descriptions

T Field. Specifies the type of instruction.

T	Operation*		Format
0000x	goto JA		4
00010	Short imm j, k, rb, re		9
00011	Short imm r0, r1, r2, r3		9
00100	Y = a1[I]	F1	1
00101	Z : aT[I]	F1	2a
00110	Y	F1	1
00111	aT[I] = Y	F1	1a
01000	aT = R		7a
01001	R = a0		7
01010	R = N		8
01011	R = a1		7
01100	Y = R		7
01101	Z : R		7
01110	do, redo		10
01111	R = Y		7
1000x	call JA		4
10010	ifc CON	F2	3
10011	if CON	F2	3
10100	Y = y[I]	F1	1
10101	Z : y[I]	F1	2
10110	x = Y	F1	1
10111	y[I] = Y	F1	1
11000	Branch indirect		5
11001	y = a0 x = X	F1	1
11010	Cond. branch qualifier		6
11011	y = a1 x = X	F1	1
11100	Y = a0[I]	F1	1
11101	Z : y x = X	F1	2
11110	Reserved		—
11111	y = Y x = X	F1	1

* imm = immediate

D Field. Specifies a destination accumulator.

D	Register
0	Accumulator 0
1	Accumulator 1

$\overline{aT}$ Field. Specifies transfer accumulator.

$\overline{aT}$	Register
0	Accumulator 1
1	Accumulator 0

S Field. Specifies a source accumulator.

S	Register
0	Accumulator 0
1	Accumulator 1

X Field. Specifies the addressing of ROM data in two-operand multiply/ALU instructions. Specifies the high or low half of an accumulator or the y register in one-operand multiply/ALU instructions.

X	Operation
Two-Operand Multiply/ALU	
0	*pt++
1	*pt++i
One-Operand Multiply/ALU	
0	aTl, yl
1	aTh, yh

F1 Field. Specifies the multiply/ALU function.

F1	Operation	
0000	aD = p	p = x*y
0001	aD = aS + p	p = x*y
0010		p = x*y
0011	aD = aS – p	p = x*y
0100	aD = p	
0101	aD = aS + p	
0110	NOP	
0111	aD = aS – p	
1000	aD = aS | y	
1001	aD = aS ^ y	
1010	aS & y	
1011	aS – y	
1100	aD = y	
1101	aD = aS + y	
1110	aD = aS & y	
1111	aD = aS – y	

Y Field. Specifies the form of register indirect.

Y	Operation
0000	*r0
0001	*r0++
0010	*r0– –
0011	*r0++j
0100	*r1
0101	*r1++
0110	*r1– –
0111	*r1++j
1000	*r2
1001	*r2++
1010	*r2– –
1011	*r2++j
1100	*r3
1101	*r3++
1110	*r3– –
1111	*r3++j

Z Field. Specifies the form of register indirect compound addressing with postmodification.

Z	Operation
0000	*r0zp
0001	*r0pz
0010	*r0m2
0011	*r0jk
0100	*r1zp
0101	*r1pz
0110	*r1m2
0111	*r1jk
1000	*r2zp
1001	*r2pz
1010	*r2m2
1011	*r2jk
1100	*r3zp
1101	*r3pz
1110	*r3m2
1111	*r3jk

I Field. Specifies a register for short immediate data move instructions.

I	Register
00	r0/j
01	r1/k
10	r2/rb
11	r3/re

SI Field. Specifies when the conditional branch qualifier instructions should be interpreted as a software interrupt instruction.

SI	Operation
0	Not a software interrupt
1	Software interrupt

INSTRUCTION SET ENCODING
Replacement Tables for Format Fields

F2 Field. Specifies the special function to be performed.

F2	Operation
0000	aD = aS >> 1
0001	aD = aS << 1
0010	aD = aS >> 4
0011	aD = aS << 4
0100	aD = aS >> 8
0101	aD = aS << 8
0110	aD = aS >> 16
0111	aD = aS << 16
1000	aD = p
1001	aDh = aSh + 1
1010	Reserved
1011	aD = md(aS)
1100	aD = y
1101	aD = aS + 1
1110	aD = aS
1111	aD = –aS

B Field. Specifies the type of branch instruction (except software interrupt).

B	Operation
000	return
001	ireturn
010	goto pt
011	call pt
1xx	Reserved

R Field. Specifies the register for data move instructions.

R	Register
000000	r0
000001	r1
000010	r2
000011	r3
000100	j
000101	k
000110	rb
000111	re
001000	pt
001001	pr
001010	pi
001011	i
010000	x
010001	y
010010	yl
010011	auc
010100	psw
010101	c0
010110	c1
010111	c2
011000	sioc
011001	srta
011010	sdx
011011	tdms
011100	pioc
011101	pdx0
011110	pdx1
Other codes	Reserved

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C Field. Specifies the condition for special functions and conditional control instructions.

CON	Condition
00000	mi
00001	pl
00010	eq
00011	ne
00100	lvs
00101	lvc
00110	mvs
00111	mvc
01000	heads
01001	tails
01010	c0ge
01011	c0lt
01100	c1ge
01101	c1lt
01110	true
01111	false
10000	gt
10001	le
Other codes	Reserved

NI Field. Number of instructions to be loaded into the cache. Zero implies redo operation.

K Field. Number of times the NI instruction in cache are to be executed.

JA Field. 12-bit jump address.