

# OPERATIONS MANUAL

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**DSTD  
101** CPU AND  
PARALLEL I/O  
DY00439

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**dy-4 SYSTEMS INC.**

DOCUMENT NO. DSTD-101-M  
REVISION 3

DSTD-101  
CPU AND PARALLEL I/O  
OPERATORS MANUAL  
DY00439

PREPARED BY: dy-4 SYSTEMS INC.

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#### NOTICE

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## REVISION

This revision of the DSTD-101 manual also includes a change to the functionality and layout of the card itself. The following describes the change from revision 2 of the PCB to revision 3.

The change is in the memory socket configuration jumper blocks, J5, J7, J8, J10 and J11. Revision 3 of the DSTD-103 supports 8K x 8 pseudo static RAMs. It also fixes a design bug in 2764 configurations Section 3-3 and Appendix A-3 show the new jumper block layouts.

The on-board memory disable option is described in this revision. It was previously an undocumented option and is available on all revisions of the board.

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## SECTION 1

## 1.0 GENERAL INFORMATION

## 1.1 Introduction

The dy-4 SYSTEMS DSTD-101 CPU, Figure 1-1, is a Z80 based microcomputer board. It features five 28 pin memory sockets capable of accepting any combinations of pin compatible RAM, ROM or EPROM. Additionally, it provides a 4-channel counter/timer which is accessible both internally through software and externally for zero-count output and trigger control. It also provides two 8 bit parallel ports with either totem pole or open collector drivers. The ports may be individually strapped as either input or, output; transparent or latched. On-board memory can be disabled under software control. This means that the DSTD-101 can be used in systems requiring boot PROMs as well as a full 64K bytes of RAM.

## 1.2 DSTD Series General Description

The DSTD series was designed to satisfy the need for low cost OEM microcomputer modules. The DSTD-Z80 BUS uses a mother board interconnect system concept. The modules for the STD-Z80 BUS are a compact 4.5 x 6.5 inches which provides for system partitioning by function, e.g. CPU, Memory, I/O, etc. This smaller module size makes system packaging easier, while increasing MOS-LSI densities provide high functionality per module.

## 1.3 DSTD-101 CPU Features

- \* Utilizes the powerful Z80 microprocessor.
- \* Provides five 28-pin sockets which may be strapped to accept any combination of the following industry-standard memory devices:

EPROM	STATIC RAM	ROM
2758 (1Kx8) 2759 (1Kx8)	4118 (1Kx8)	MK34000 (2Kx8)
2716 (2Kx8)	4801 (1Kx8)	
2732 (4Kx8)	4802 (2Kx8)	
2764 (8Kx8)	2186 (8Kx8)	



- \* Bi-directional address, data and control busses to permit external DMA.
- \* Four cascadable counter/timer channels, both hardware and software accessible.
- \* Two 8-bit parallel ports, both strappable for either input or output.
- \* On-board memory can be disabled under software control ( see the restrictions discussed in sections 2.2.9 and 3.2.3.)
- \* Fully buffered signals for system expandability.
- \* Selectable reset address to either 0000H or E000H.
- \* Selectable Wait State generator, for memory devices on all M1 cycles or all MEMRQ cycles or all INTAK cycles or on-board memory cycles only.
- \* Compatible with MDX-SST for single step operation during debugging.
- \* 4 MHz version available.
- \* Single +5 Volt supply.
- \* STD-280 BUS compatible.



FIGURE 1-1 DSTD-101 MODULE

## SECTION 2

### 2.0 FUNCTIONAL HARDWARE DESCRIPTION

#### 2.1 Introduction

The DSTD-101 utilizes a Z80 microprocessor as the system controller. It features five 28-pin memory sockets. The user can populate the module with any combination of designated ROM, RAM and EPROM. Address decoding allows the user to configure the memory on any 8K boundary of the 64K memory map. A PAL decoder is supplied which will allow the user to choose one of two popular memory configurations or, if desired, the user may implement other mixtures of memory devices simply by programming the PAL accordingly.

A 4-channel counter/timer circuit is included on-board for software controlled counting and timing functions. The CTC Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external access. In addition, an on-board strapping option makes it possible to cascade the four CTC channels for long count sequences.

The DSTD-101 has two 8-bit parallel ports. Each port can be configured as either an input or output. The ports may be either Totem Pole/Open Collector, Inverting/Non-Inverting, Latched or Transparent.

A strapping option allows the user to select a reset address of either 0000H or E000H. The E000H option is required for use of standard software and hardware products including dy-4 SYSTEMS Monitor and CP/M operating system disk boot proms. These products also require strapping on-board RAM to reside at Location FC00 through FFFFH.

A 4MHz version of DSTD-101 is also available.

#### 2.2 Block Diagram Description

Figure 2-1 is a Block Diagram illustrating the flow of system address, data and control signals on DSTD-101. The following paragraphs describe the function of each of the major blocks.

##### 2.2.1 CPU

The Z80 CPU is the system controller. It fetches, decodes and executes instructions from memory and generates the necessary address and control signals to co-ordinate data flow between the CPU and memory, or between the CPU and system I/O system.

### 2.2.2 Clock Generator

The DSTD-101 uses a crystal-controlled oscillator to generate the basic clock signals necessary for sequencing and synchronizing all CPU operations. The divide-by-2 clock ensures a 50% duty cycle. The system clock frequency is 2.5 MHz for the DSTD-101-2.5 and 4.0 MHz for the DSTD-101-4.0. An inverted clock is applied to the system bus for use by other modules. An active pullup circuit ensures proper clock levels.

### 2.2.3 CTC (Counter/Circuit)

The Counter/Timer Circuit (MK3882/Z80-CTC) provides four independent, programmable channels for either software or hardware controlled counting and timing functions. Each channel can be configured by the CPU for various modes of operation and the built-in daisy chain priority interrupt logic provides for automatic, independent interrupt vectoring. The I/O port addresses for the CTC are hard-wired as follows:

I/O PORT ADDRESS	CTC CHANNEL
7C	0
7D	1
7E	2
7F	3

The Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external hardware control. A strapping option has also been included to permit any or all of the four CTC channels to be cascaded for long count sequences.

Section 3 provides the necessary information for utilizing this option. For a complete description of CTC operation, refer to either the Mostek MK3882 or Zilog Z80-CTC Technical Manual.

### 2.2.4 Memory

The DSTD-101 has been designed to accommodate any combination of the byte-wide RAM, ROM and EPROM devices. Five 28-pin sockets have been provided, each of which may be strapped for any of the allowed memory types. These user-selectable options are fully described in Section 3.

### 2.2.5 Decode Logic

This section primarily consists of a PAL which decodes the high order six bits of memory address and generates the applicable chip select if on-board memory is to be selected. The PAL provides for two separate memory configurations. The first places the memory starting at 0000H. The second places the memory starting at E000H. A strapping option must be hard-wired to the desired configuration as explained in Section 3.

### 2.2.6 Reset Control Logic

This is a strapping option that causes a hardware-forced memory starting address upon system reset. A reset address of either 0000H or E000H may be selected.

### 2.2.7 Wait State Generator

This function, if selected, causes memory read and write cycles to be lengthened by one clock period for slower memory devices. An additional Wait State may also be inserted during INTAK cycles.

### 2.2.8 Parallel Ports

The DSTD-101 has two parallel ports. These ports are implemented using octal transceiver chips. The jumper blocks associated with the ports are used to "program" the transceivers for appropriate operations.

### 2.2.9 On-board Memory Disable

The DSTD-101 has a latch that can be used to disable all or part the on-board memory allowing the processor to access a full 64K bytes of external memory. (The memory decode PAL is normally programmed to disable all on-board memory.) This latch is a single bit latch accessed as an I/O port located at 7BH using bit 0 of the data bus. The feature is enabled by installing a jumper between JB12-9 and JB12-10.

**Note that 7BH is also the address of parallel port B. Thus using this feature puts restrictions on the use of the B port. To enable the on-board memory write to port B (7BH) with bit 0 cleared. To disable on-board memory write to port B with bit 0 set.**

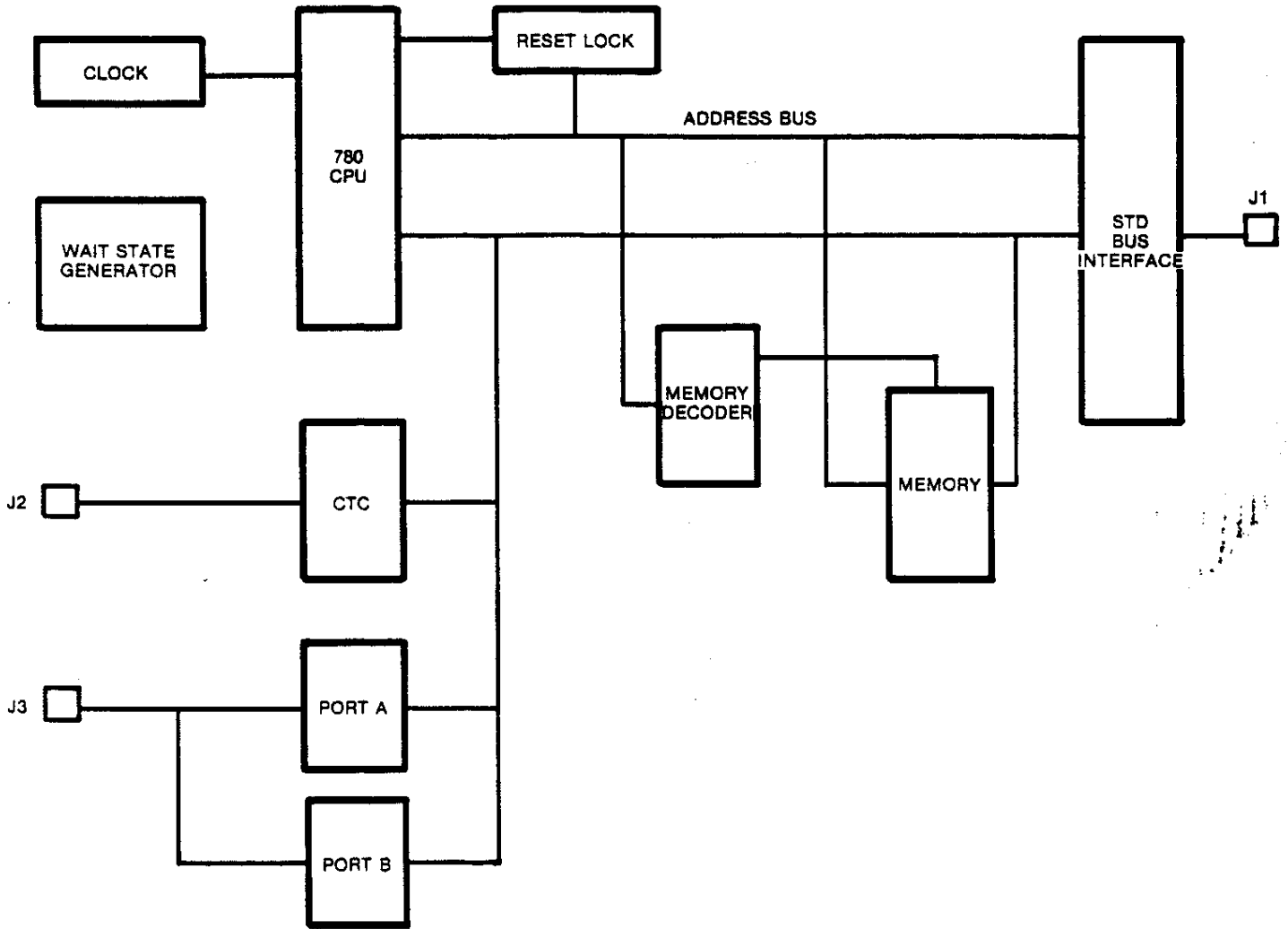


FIGURE 2 - 1 DSTD 101 FUNCTIONAL BLOCK DIAGRAM

## SECTION 3

## 3.0 USER SELECTABLE OPTIONS

## 3.1 Introduction

The DSTD-101 incorporates many strapping options to provide the user with a high degree of flexibility in system configurations. This section describes the use of the available jumper options.

## 3.2 Memory Options

The PAL memory decoder shipped with the DSTD-101 from the factory supports the following options.

## 3.2.1 Restart Address

The DSTD-101 is capable of starting execution at either 0000H or E000H after reset. Reset address E000H is implemented in hardware. Since the program counter (internal to the Z80 microprocessor) always resets to 0000H, external hardware is required to force the most significant three bits of the data bus to all ones to get 0E000H. A multiplexer and a latch to control the multiplexer are used to perform this function. The first instruction at E000H should be 'JMP E003' to set the processors internal program counter to the correct memory location. The hardware latch forcing the address bit must then be cleared. This is done automatically by the first I/O cycle that the processor performs. If no I/O port access is normally made then a dummy I/O read to an unused port address must be done otherwise memory accesses will be constrained to addresses E000H through FFFFH. To ensure proper operation after reset, the following code sequence should be placed in memory at the E000H.

ADDRESS		INSTRUCTION	
E000	C303E0	JP E003H	; jump instruction ; to update program computer
E003	DB nn	IN A, (nn)	; read unused I/O ; port nn to clear ; reset address latch
E005			; first instruction of ; user program

If standard dy-4 Systems software (DSTD-101P or PBOOT) is used, address E000H must be strapped as the reset address to be compatible with the firmware packages. The program counter and address latch modification instructions previously described are already contained within monitor PROM. Ensure that pins 2 and 3 of JB14 are connected when the MDX-SST module is used.

3.2.2 Memory Configuration

The DSTD-101 incorporates five 28-pin sockets which can be independently configured to accept a variety of pin compatible memory devices. Tables 3-1, 3-2 and 3-3 list the memory sockets, their corresponding jumper blocks and address space for both standard configurations for several memory device sizes.

The DSTD-101 is shipped from the factory with a memory decoding PAL (U12) that supports the two most popular memory configurations using 2K byte chips. The first configuration starts the memory at location 0000H and the second starts it at location E000H. The first configuration is selected by installing a jumper between JB12-5 and JB12-6. The memory decoder offers the option to disable the fifth socket. This feature is supplied because dy-4 Systems memory products are arranged in 8K byte pages. The first four sockets are sufficient to fill the first 8K byte page and thus to allow a full 48K byte RAM system without memory addressing conflicts and double driving the backplane bus the fifth socket can be disabled. The fifth socket is disabled by installing a jumper between JB12-7 and JB12-8. Refer to Table 3-5.

In the second configuration the first four of the five socket can occupy the full 8K bytes starting at E000H or the second half of the fourth socket (FC00H to FFFFH) can be disabled and the fifth socket enabled. The fifth socket in these configurations is typically occupied by a RAM device and is required for some system firmware packages. The fifth socket is enabled by installing a jumper between JB12-7 and JB12-8. Refer to Table 3-5.

TABLE 3-1

2K MEMORY DEVICES/JUMPER BLOCK ASSIGNMENT

SOCKET	ADDRESS OPT 0	ADDRESS OPT 1	JUMPER BLOCK
U5	0000 - 07FF	E000 - E7FF	JB5
U6	0800 - 0FFF	E800 - EFFF	JB7
U7	1000 - 17FF	F000 - F7FF	JB8
U8	1800 - 1FFF	F800 - FBFF (FFFF)	JB10
U9	2000 - 27FF ( - )	FC00 - FFFF ( - )	JB11



There are two other standard memory decoder PAL's available from the factory. One is used with 4K x 8 memory devices and the other is used with 8K x 8 memory devices. Table 3 - 2 shows the memory map for 4K devices and Table 3 - 3 shows the memory map for the 8K devices. Consult the factory if these options are required.

TABLE 3 - 2  
4K MEMORY DEVICES/JUMPER BLOCK ASSIGNMENT

SOCKET	ADDRESS OPT 0	ADDRESS OPT 1	JUMPER BLOCK
U5	0000 - 0FFF	C000 - CFFF	JB5
U6	1000 - 1FFF	D000 - DFFF	JB7
U7	2000 - 2FFF	E000 - EFFF	JB8
U8	3000 - 3FFF	F000 - FBFF (FFFF)	JB10
U9	4000 - 4FFF	FC00 - FFFF	JB11

TABLE 3 - 3

8K MEMORY DEVICES/ BLOCK ASSIGNMENT

SOCKET	ADDRESS OPT 0	ADDRESS OPT 1	JUMPER BLOCK
U5	0000 - 1FFF	6000 - 7FFF	JB5
U6	2000 - 3FFF	8000 - 9FFF	JB7
U7	4000 - 5FFF	A000 - BFFF	JB8
U8	6000 - 7FFF	C000 - DFFF	JB10
U9	8000 - 9FFF	E000 - FFFF	JB11

Table 3-4 shows the straps necessary to configure the sockets for the different memory types. All the sockets are wired independently, allowing any mix of chips within the addressing constraints.

TABLE 3 - 4  
MEMORY DEVICE JUMPER STRAPS

TYPE	PART NO.	PINS				JUMPERS
		27	23	21	1	
1Kx8 EPROM	2758	-	Vpp	GND	-	B3-B2 ; A1-A2
1Kx8 EPROM	2759	-	Vpp	Vcc	-	B3-B2 ; A1-B2
2Kx8 EPROM	2716	-	Vpp	A10	-	B3-B2 ; A1-B1
4Kx8 EPROM	2732	-	A11	A10	-	B3-A4 ; A1-B1
8Kx8 EPROM	2764	PGM	A11	A10	Vpp	A3-C1 ; B3-A4 A1-B1 ; C3-B2
1Kx8 RAM	4801	-	/WE	GND	-	A3-B3 ; A1-A2
2Kx8 RAM	4802	-	/WE	A10	-	A3-B3 ; A1-B1
8Kx8 RAM	2186	/WE	A11	A10	RDY	A3-C1 ; A4-B3 A1-B1 ; C2-C3
2Kx8 EEROM	X2816A	-	/WE	A10	-	A3-B3 ; A1-B1

JUMPER BLOCK LAYOUT FOR J5,J7,J8,J10,J11

	A	B	C
1	o	o	o
2	o	o	o
3	o	o	o
4	o	o	

Table 3-5 shows the JB12 straps necessary for the two standard configurations with RAM enabled and disabled for 2Kx8 devices.

TABLE 3 - 5  
1K-RAM ADDRESS/ENABLE OPTIONS

ADDRESS	JUMPER CONNECTIONS JB12
Sockets 0000H - 1FFFH	5-6
Fifth Socket enabled (2000H - 27FFH)	7,8 open
Fifth Socket disabled	7-8
Sockets E000H - FBFFH	5,6 open
Fifth Socket enabled (FC00H - FFFFH)	7,8 open
Fifth Socket Disabled	7-8

### 3.2.3 On-board Memory Disable Option

The DSTD-101 has a latch that can be used to disable all or part the on-board memory allowing the processor to access a full 64K bytes of external memory. (The memory decode PAL is normally programmed to disable all on-board memory.) This latch is a single bit latch accessed as an I/O port located at 7BH using bit 0 of the data bus. The feature is enabled by installing jumper JB12 4A-4B.

**Note that 7BH is also the address of parallel port B.** Thus using this feature puts restrictions on the use of the B port. To enable the on-board memory write to port B (7BH) with bit 0 cleared. To disable on-board memory write to port B with bit 0 set.

### 3.3 Debug/Single Step Configuration

The DSTD-101 supports the MDX-SST module. This module generates a NMI (non-makable interrupt) and asserts the DEBUG signal. This debug signal, when enabled, forces a logic '1' onto the most significant three bits of the address bus. Thus the interrupt service is located at E066H. If the debug is disabled the interrupt service routine is at the normal address (0066H). To enable the debug line, install a jumper between JB14-3 and JB14-2 and between JB12-1 and JB12-2. Ensure that the memory option straps position the monitor software at E000H. dy-4 SYSTEMS' firmware supports the single step facilities.

### 3.4 WAIT STATE Generator

Three jumpers are provided to allow the use of slow memory devices. The first jumper generates a WAIT STATE on all memory cycles. The second jumper generates a WAIT STATE for M1 memory cycles only. Table 3-6 lists the access times of internal memory devices and table 3-7 lists the access times of external memory cards for the two different memory cycle types for both the 2.5 MHz and 4.0 MHz DSTD-101 cards. The third jumper generates a WAIT STATE on internal memory accesses only. Thus EPROMS can be used

along with a high speed RAM card. A fourth jumper allows the generation of a WAIT STATE on interrupt acknowledge cycles. Table 3-8 gives the connections for the WAIT STATE options.

TABLE 3 - 6  
M1-MEMORY CYCLE WAIT STATE TIMING - INTERNAL  
(in nS)

FUNCTION	JB13 CONNECTIONS	2.5MHz		4.0MHz	
		M1	Other	M1	Other
No Wait States		550	750	300	425
Wait States on M1 cycle	6 to 5	950	750	560	425
Wait States on all memory cycles	8 to 7	950	1150	560	675

TABLE 3 - 7  
M1-MEMORY CYCLE WAIT STATE TIMING - EXTERNAL  
(in nS)

FUNCTION	JB13 Connections	2.5MHz		4.0MHz	
		M1	Other	M1	Other
No wait States		580	780	340	455
Wait States on M1 cycle	6 to 5	620	780	590	455
Wait States on all memory cycles	8 to 7	620	1180	590	705

TABLE 3 - 8  
WAIT STATE OPTIONS

OPTION	JUMPER BLOCK JB13
No WAIT STATES	All open
All M1 cycles	5 to 6
All Memory cycles	7 to 8
Internal Memory cycles only	3 to 4
Internal Memory cycles and external M1 cycles	3 to 4 5 to 6
Interrupt acknowledge cycles	1 to 2

**3.5 Counter/Timer Options**

The four Counter/Timer channels may be cascaded for extended counting and timing functions. Table 3-9 shows the jumper pin numbers and the edge connector numbers for the CTC. Refer to the MK3882 Technical Manual or the Zilog Data Book for a complete description of CTC operation.

TABLE 3 - 9  
CTC CONNECTOR PIN ASSIGNMENT

SIGNAL		EDGE CONNECTOR		JUMPER BLOCK	
NAME		J2		JB4	
C/T0	I	1		2	
ZC0	O	2		3	
C/T1	I	3		4	
ZC1	O	4		5	
C/T2	I	5		6	
ZC2	O	6		7	
C/T3	I	7		8	
NMI		9		1	

Provision is made on the jumper block to enable the NMI input of the processor to be connected to one of the outputs of the CTC. NMI appears on pin 1 of JB4.

The CTC may also be used to generate interrupts or status changes during parallel I/O transfers. This will be discussed in more detail in the following sections.

### 3.6 PARALLEL PORTS

The DSTD-101 has two independent 8 bit parallel ports. These ports are implemented using the 74LS646/7/8/9 series of IC's. They are octal transceivers with latches. Table 3-10 lists the basic functions of these chips (see Appendix E for details).

TABLE 3 - 10  
I/O PORT DEVICE SELECTION OPTIONS

	DATA PATH	OUTPUT
74LS646	TRUE	3-State
74LS647	TRUE	Open Collector
74LS648	INVERTING	3-State
74LS649	INVERTING	Open Collector

Note when using open collector devices Resistor Network RN4 must be installed.

Both parallel ports are accessed through the one connector J3. Table 3-11 shows the pinouts for the connector.

TABLE 3 - 11  
I/O PORT CONNECTOR PIN ASSIGNMENT

PORT SIGNAL	PORT A	PORT B
DATA 0	1	11
DATA 1	2	12
DATA 2	3	13
DATA 3	4	14
DATA 4	5	15
DATA 5	6	16
DATA 6	7	17
DATA 7	8	18
CLKP	9	19
CONTROL	10	20
GND	21,22,23,24,25,26	

### 3.6.1 Modes Of Operation

Each parallel port has six basic modes of operation. These modes represent the most common configurations.

- 1) Latched Input Mode
- 2) Transparent Input Mode
- 3) Latched Output Mode
- 4) Transparent Output Mode
- 5) Latched Bidirectional Mode
- 6) Transparent Bidirectional Mode

Note, that latched bidirectional mode typically uses both ports. Table 3-13 summarizes some of the port configurations discussed in the following section.

### 3.6.2 Latched Input

In this mode, data is clocked into the port register by an external device using the "CLKP" signal. Data is clocked on rising edge of "CLKP". In some applications it is necessary to

inform the processor that valid or new data is available. This can be accomplished using the CTC.

Connect the "CLKP" signal to a channel on the counter/timer. The "CLKP" signal for port A is pin 9 and for port B it is pin 10 on the CTC jumper block JB4. This pin can be connected to a free CTC channel (CH0) / J4B-2; CH1 / J4B-4; CH2 / JB4-6; CH3 / JB4-8). The CTC channel is then used in the counter mode to report positive transitions of the "CLKP" signal.

### 3.6.3 Transparent Input Mode

In this mode the data is read directly from the port. This mode is typically used for scanning switches or other relatively static information - or when there is no clock available. Again the control signal, with the CTC may be used to indicate "valid data" as discussed in section 3.5.2.

### 3.6.4 Latched Output

In this mode the processor writes data into the port. The CONTROL signal may be used in one of several ways. Firstly, it may be used by the external device to enable the port. The CONTROL signal is connected to the ENABLE input of the port register. (Connect pins 4 and 3 on the appropriate port jumper block). Secondly, the control signal can be used as a strobe in the external device to indicate valid data. (Note that in latched output mode it cannot be used to clock data into the external device - use transparent output mode if this function is required). To use the CONTROL signal as a strobe connect pins 2 and 4 on the port jumper block. Thirdly, the CONTROL signal may be connected to a channel of the CTC and used by the external device to inform the processor that it is ready for new data. The strapping options allow many other handshake arrangements including combinations of the above.

### 3.6.5 Transparent Output

This mode is used when strobing data into an external device. The CONTROL signal is connected to the write port line (pins 2 and 4 of the port jumper block). In this mode the port acts simply as a buffer. Data is clocked on the rising edge of the CONTROL signal.

### 3.6.6 Latched Bidirection Mode

This mode typically requires the use of both ports. Port A for the OUT direction and Port B for the IN direction. The ports are connected together in the edge connector (J3). The external device controls the direction of the data flow on the bidirectional bus. The external device clocks data into the B port using CLKPB.

CLKPB can be connected in the CTC to provide an indication to



the processor that new valid data is available from the external device. The /RDPB signal is connected to the CONTROL B signal to inform the external device when the processor has read the data from the port. The processor outputs data to the external device by writing it to Port A. /WRPA is connected to CLKPA (JB4-9 to JB6-2). This is used to inform the external device that new data is available from the processor. The external device enables the data onto the bus using the CONTROLA line. The CONTROLA line can be connected to a CTC channel to let the processor know when the external device has taken the data.

### 3.6.7 Transparent Bidirectional Mode

This mode provides simple bidirectional capability. The port is enabled at all times and the direction is controlled by the RDPA signal. ie. The direction is out unless the processor is "reading" the port. The /RDPA is also connected to the control signal to enable the drivers in the external device. The CLKPA line can be either connected to the CTC or to the /WRPA signal to provide handshake signals in the desired direction. Other configurations are possible. For example the out data can be latched instead of transparent.

Jumper blocks JB6 and JB9 are used to configure Port A and Port B respectively. Table 3-11 shows connector pinouts for both ports (J3).

Port A has the I/O address 7AH and Port B is 7BH.

Table 3-12 describes the Jumper Block pin functions.

TABLE 3 - 12  
PARALLEL PORT JUMPER BLOCK PIN DESCRIPTION (JB6,9)

PIN	NAME	FUNCTION
1	RDP(A/B)	Read port signal from the processor usually connected to the ENABLE or DIRECTION pins.
2	WRP(A/B)	Write port signal from the processor usually connected to the CONTROL signal for handshake purposes.
3	ENABLE(A/B)	Port chip enable when low, enables the port.
4	CONTROL(A/B)	General purpose signal for connect to external device to CTC or ENABLE.
5	SEL AB	When low the "out" direction is transparent. When high the "out" direction is latched - strobed by WRP (A/B).
6,8	GND	Used for option selection.
7	SEL BA	When low the "in" direction is transparent. When high the "in" direction is latched - strobed by CLKP (A/B).
9	DIRECTION	Controls the direction of the port when enabled - low is in, high is out.
10	+5V	used for option selection.

Refer to Appendix E for detailed specifications of the integrated circuits needed to implement the parallel ports.

TABLE 3 - 13  
SAMPLE PORT CONFIGURATION

MODE	JB6 and/or JB9 JUMPER CONFIGURATIONS		FUNCTION
LATCHED MODE	8-9 1-3 7-10		Direction in Port enable Latched mode
TRANSPARENT INPUT	8-9 1-3 7-8		Direction in Port enable Transparent
LATCHED OUTPUT	9-10 3-6 or (3-4)  or (2-4)  5-10		Direction out Enable on When external device controls enable Strobe for external device Latched mode
TRANSPARENT OUTPUT	9-10 3-6 2-4  5-6		Direction out Enable on Write strobe for external device Transparent mode
LATCHED BIDIRECTIONAL	PORT A 9-10 (JB4 -9/JB6 -2) 3-4 (JB4 11/JB4 -8)	PORT B 8-9 1-4   JB 4-10/ JB 4-6  1-4	Direction Handshake Out enable Handshake Handshake  In enable
TRANSPARENT	1-9		Direction
BIDIRECTIONAL	3-6 1-4		Port enable Handshake

## SECTION 4

## 4.0 SPECIFICATIONS

## 4.1 FUNCTIONAL SPECIFICATIONS

## 4.1.1 Word Size

Instruction: 8, 16, 24, or 32 bits

Data: 8 bits

## 4.1.2 Cycle Time

Clock period (T state): 400 ns for DSTD-101-2.5  
250 ns for DSTD-101-4.0

Instruction Cycle: Min. 4 T states  
Max. 23 T states

## 4.1.3 Memory Capacity

Five 28-pin sockets are provided which may be populated with any mixture of the following devices:

2758 (1K x 8 EPROM)  
2716 (2K x 8 EPROM)  
2732 (4K x 8 EPROM)  
2764 (8K x 8 EPROM)  
MK 34000 (2K x 8 ROM)  
4118/4801 (1K x 8 RAM)  
4802/2016 (2K x 8 RAM)  
2186 (8K x 8 RAM)

## 4.1.4 Memory Access Time

The time required to access on-board memory by external DMA controllers is 100 ns plus the access time of the memory device. This is defined as the time interval between the time that the memory address is valid on the STD BUS and the time that the output data is valid on the STD BUS.

## 4.1.5 I/O Addressing

The on-board I/O addressing is hard-wired to the following port addresses:

PORT		ADDRESS
PARALLEL PORT A		7A
PARALLEL PORT B		7B
CTC	CH 0	7C
CTC	CH 1	7D
CTC	CH 2	7E
CTC	CH 3	7F

## 4.1.6 I/O Capacity

The CPU utilizes the lower 8 bits of its address bus for I/O addressing to yield a total of 256 possible port addresses, including the four CTC channels and 2 parallel port addresses on the module.

## 4.1.7 Interrupts

The CPU may be programmed to process interrupts in any of three different modes (mode 0, 1 or 2 as described in any Z80 Technical Manual). Mode 2 operation (vectored interrupts) is by far the most powerful and is compatible with dy-4 DSTD, and MOSTEK MDX Series cards.

Multi-level interrupt processing is also possible with the Z80 CPU. The level of stacking is limited only by available memory space.

The DSTD-101 will also accept non-maskable interrupts which force a restart at location 0066H.

## 4.1.8 System Clock

DSTD-101-2.5	2.5 MHz $\pm$ 0.05%
DSTD-101-4.0	4.0 MHz $\pm$ 0.05%

## 4.2 Electrical Specification

## 4.2.1 STD BUS Interface

Bus Inputs: One 74LS load max.

Bus Outputs:  $I_{OL}$  = 24 mA min. @  $V_{OL}$  = 0.5 Volts  
 $I_{OH}$  = 15 mA min. @  $V_{OH}$  = 2.4 Volts

#### 4.2.2 Parallel/CTC Ports

Inputs: One 74LS load max.

Outputs:  $I_{OL} = 24$  mA min. @  $V_{OL} = 0.5$  Volts

$I_{OH} = 15$  mA min. @  $V_{OH} = 2.4$  Volts

#### 4.2.3 Operating Temperature

0 Degrees C to 50 Degrees C

95% humidity non-condensing

#### 4.2.4 Power Supply Requirements

+5V +/- 5% @ 1.2A

(excluding memory power requirements)

### 4.3 Mechanical Specification

#### 4.3.1 Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long

0.48 in. (1.22 cm.) maximum height

0.062 in. (0.16 cm.) printed circuit board thickness

#### 4.3.2 STD BUS Edge Connector

56 Pin Dual Readout; 0.125 in. centers

##### 4.3.2.1 Mating Connector

Viking 3VH28/1CE5 (printed circuit)

Viking 3VH28/1CND5 (wire wrap)

Viking 3VH28/1CN5 (solder lug)

#### 4.3.3 Parallel Port Connector

26 Pin Dual Readout; 0.100 inch grid

##### 4.3.3.1 Mating Connector

Flat cable Ansley 609-2600M or equivalent

4.3.4 Counter/Timer Connector

10 Pin Dal 0.100 inch grid

4.3.4.1 Mating Connector

Flat cable Ansley 609-1000M or equivalent

## SECTION 5

### 5.0 FACTORY NOTICES

#### 5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser  
Date and place of purchase  
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

dy-4 SYSTEMS INC.,  
888 Lady Ellen Place,  
Ottawa, Ontario  
K1Z 5M1, Canada

Securely package and mail the circuit board, prepaid and insured, to the same address.

#### 5.2 Limited Warranty

Dy-4 warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

#### NOTICE

The antistatic bag is provided for shipment of the dy-4 PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will **VOID** the warranty.



APPENDIX A  
OPTION JUMPER SUMMARY

OPTION JUMPER SUMMARY

APPENDIX A

OPTION JUMPER SUMMARY

A-1 Jumper Block Functional Summary

JB4	-	Counter/Timer	
JB5	-	Memory Configuration	Socket U5
JB6	-	Parallel Port A	
JB7	-	Memory Configuration	Socket U6
JB8	-	Memory Configuration	Socket U7
JB9	-	Parallel Port B	
JB10	-	Memory Configuration	Socket U8
JB11	-	Memory Configuration	Socket U9
JB12	-	Memory Options/Addressing	
JB13	-	Wait State Generator	
JB14	-	Restart Address Option	
JB15	-	BUSAK Chain	

A-2 Counter/Timer (JB4)

1	0	Internal Non-maskable Interrupt		
2	0	Counter/Timer	Channel 0	Input
3	0	Zero Detect	Channel 0	Output
4	0	Counter/Timer	Channel 1	Input
5	0	Zero Detect	Channel 1	Output
6	0	Counter/Timer	Channel 2	Input
7	0	Zero Detect	Channel 2	Output
8	0	Counter/Timer	Channel 3	Input
9	0	Parallel Port A	Clock Signal	Input
10	0	Parallel Port B	Clock Signal	Input
11	0	Parallel Port A	Enable Signal	Input
12	0	Parallel Port B	Enable Signal	Input

OPTION JUMPER SUMMARY

A-3 Memory Configuration (JB5,7,8,10,11)

The following shows the layout of the memory configuration jumper blocks. The layout is the same for all sockets. J5, J7, J8, J10, J11.

	A	B	C
1	o	o	o
2	o	o	o
3	o	o	o
4	o	o	

- A1 Socket Pin 21 A10, L
- A2 Ground
- A3 Processor Write Strobe
- A4 Processor Address bit 11
- B1 Processor Address bit 10
- B2 +5V
- B3 Socket Pin 23 WE/Vpp/All
- B4 n/c
- C1 Socket Pin 27 WE/Vpp
- C2 Wait Line
- C3 Socket Pin 1 Wait/Vpp

A-4 Parallel Port Configuration (JB6,9)

The following shows the layout of the parallel port configuration jumper blocks.

Read Port Signal	1	o	o	2	Write Port Signal
Port Enable (Enable)	3	o	o	4	(Control)
SEL A/B	5	o	o	6	Ground
SEL B/A	7	o	o	8	Ground
Direction	9	o	o	10	+5V

OPTION JUMPER SUMMARY

A-5 Memory Options (JB12)

JB12

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

1,2	Single Step Debug Option Enable
3,5,7	Ground
4	Opt 2 Memory Option Input 2
6	Opt 1 Memory Option Input 1
8	ENSRAM Enable Static Ram
9,10	DSMEM Onboard Memory Paging Option Enable

A-6 Wait State Generator (JB13)

JB13

2	4	6	8
o	o	o	o
o	o	o	o
1	3	5	7

Install a jumper to generate a Wait State on the appropriate condition: 1,2 INTAK; 3,4ANYCS; 5,6MI; 7,8MREQ.

A-7 Restart Address Option (JB14)

1	o	Ground
JB14 2	o	Multiplexer Select
3	o	Restart/Debug Latch

A-8 BUSAK Chain (JB15)

This option is not normally installed.

APPENDIX B

STD-Z80 BUS PIN OUT

## APPENDIX B

### STD-280 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
14	D4	
15	A7	
16	A15	
17	A6	
18	A14	Address Bus (Tri-state, output, active high).

STD-Z80 BUS PIN OUT

19	A5	A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

STD-Z80 BUS PIN OUT

- 36        /MEMEX                    Memory expansion, not used on dy-4 Systems DSTD cards.
- 37        /REFRESH                /REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
- 38        /DEBUG                    /DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
- 39        /M1                        Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
- 40        STATUS 0                    DMA priority chain input.
- 41        /BUSAK                      Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.



STD-Z80 BUS PIN OUT

- 42        /BUSRQ            Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
- 43        /INTAK            Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
- 44        /INTRQ            Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
- 45        /WAITRQ            WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

STD-Z80 BUS PIN OUT

- 46        /NMIRQ            Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
- 47        /SYSRESET        System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
- 48        /PBRESET           Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
- 49        /CLOCK                Processor Clock (Output, active low). Single phase system clock.
- 50        CNTRL                Auxiliary Timing
- 51        PCO                   Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

STD-Z80 BUS PIN OUT

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C

PARTS LIST

## APPENDIX C

## PARTS LIST

DY00439 -I - 11 - 3

CPU PARALLEL I/O CARD

QTY	DESIGNATION	PART NUMBER
Integrated Circuits		
1	U20	74LS04
1	U16	74LS08
1	U18	74LS20
2	U19, U17	74S74
1	U15	74LS74
1	U26	74LS123
1	U25	74LS243
2	U1, U24	74LS244
1	U11	74LS257A
3	U21, U22, U23	74LS645
2	U2, U3	74LS646/7/8/9
1	U10	3880 [-4] Z80A
1	U4	3882 [-4] CTC
1	U14	PAL12L6 VER 1.0
1	U13	PAL12L6 VER 3.0
1	U12	PAL12L6 VER 2.0
Resistors		
4	RN1, RN2, RN5, RN4	109-102G
	RN3,	109-472G
1	R7, R8	470 1/4 watt
1	R1	22 1/4 watt
1	R3	220 1/4 watt
1	R2	1.2K 1/4 watt
1	R6	100 1/4 watt
2	R4, R5	30K 1/4 watt
1	Q1	2N3906 Trans-istor
1	Y1	5.00 [8.00] MHz Series resonant crystal.
1	D1	1N4148

DSTD - 101 PARTS LIST

Capacitors

2	C2, C6	10uF Tantalum
2	C1, C26	30pF cer radial
19	C7-C25	0.01uF cer radial
1	C3	0.1uF cer radial
2	C5, C4	1,000pF ceramic radial

Sockets

3	20 pin	AMP 640-464-1
2	24 pin	AMP 583-460-3
6	28 pin	AMP 640-362-1
1	40 pin	AMP 640-379-1

Connectors

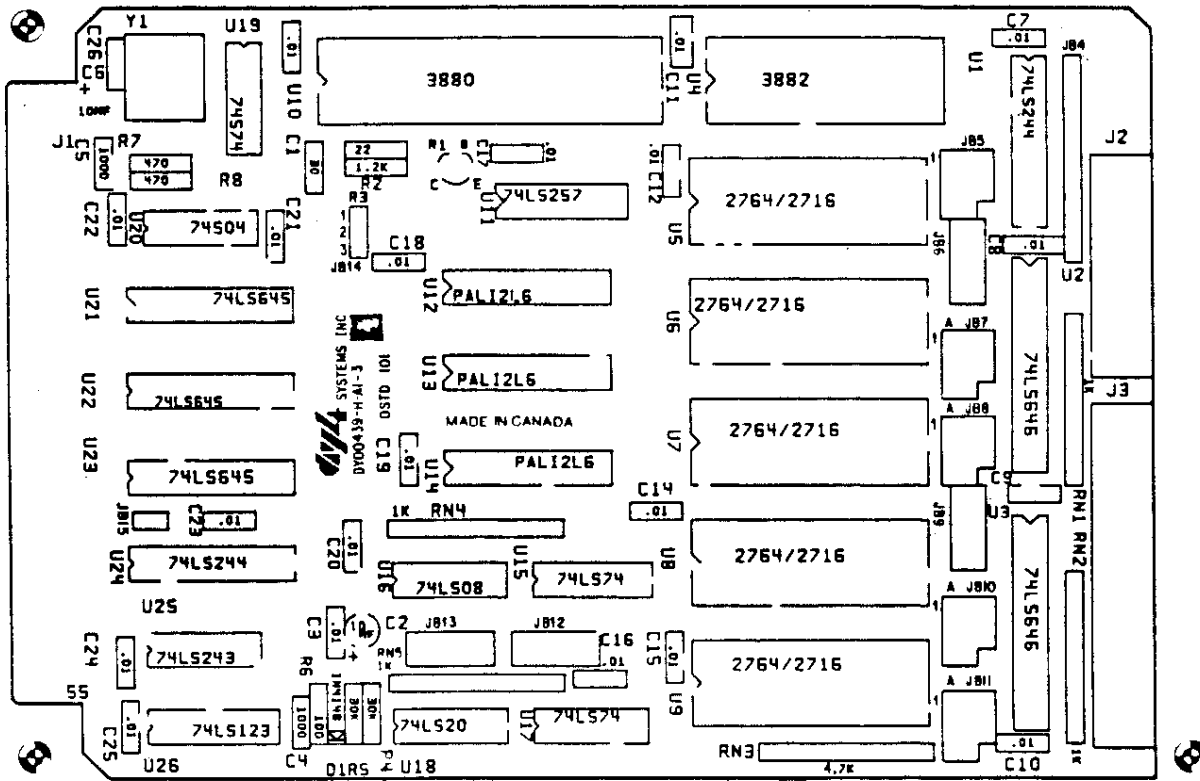
1	J2	10 pin right angle connector AMP 87476-2
1	J3	26pin right angle connector AMP 87476-3

Jumper Blocks

3	JB6, 9, 12	10 Pin dual SAE CHD6910W1S
1	JB4	12Pin Single SAE CHS6912W1S
5	JB5,7,8,10,11	3 Pin Single SAE CHS6903W1S 8 Pin Dual SAE CHD6908W1S
1	JB15	2Pin Single SAE CHS6902W1S
1	JB14	3 Pin Single SAE CHS6903W1S
1	JB13	8 Pin Dual SAE CHD6908W1S

Hardware

1	PCB	DY00439-D-A1-3
1	EJECTOR	HA9XBOLK



FILM N° DY00439-K-A1-3

FIGURE C-1 DSTD-101-3 SILK SCREEN

**APPENDIX D**  
**SCHEMATIC**

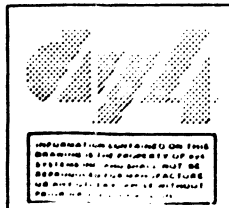
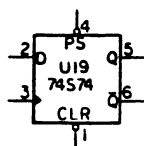
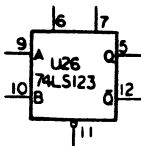


60				
59				
58				
57				
56				
55				
54				
53				
52				
51				
50				
49	1		TRANSISTOR 2N3906	Q1
48				
47	1		RESISTOR NETWORK 10 pin SIP 4.7K	RN3
46	4		RESISTOR NETWORK 10 pin SIP 1K	RN1,2,4,5
45	2		FIXED COMP 1/4W 470 5%	R7,8
44	1		RESISTOR 100	R6
43	2		RESISTOR 30K	R4,5
42	1		RESISTOR 220	R3
41	1		RESISTOR 1.2K	R2
40	1		RESISTOR FIXED COMP 1/4W 22 5%	R1
39				
38	3		HEADER (2 x 5)	JB6,9,12
37	5		HEADER (2 x 4)	JB5,7,8,10,11
36	1		HEADER (1 x 12)	JB4
35	1		HEADER (1 x 5)	JB13
34	1		HEADER (1 x 4)	JB13
33	6		HEADER (1 x 3)	JB5,7,8,10,11,14
32	1		HEADER (1 x 2)	JB15
31				
30	1		DIODE 1N4148	D1
29				
28	1		CRYSTAL HC18 5.00-8.00 MHZ	Y1
27				
26	1		CONNECTOR	J3
25	1		CONNECTOR	J2
24				
23	19		CAPACITOR 0.01 $\mu$ F	C7-25
22	2		RESISTOR 1000 pF	C4,5
21	1		RESISTOR 0.1 $\mu$ F	C3
20	2		RESISTOR 10 $\mu$ F	C2,6
19	2		CAPACITOR 30 pF	C1,26
18				
17	3		INTEGRATED CIRCUIT PAL12L6	UI2-14
16	1		RESISTOR 3882-4 CTC	U4
15	1		RESISTOR 3880-4 280(A)	U10
14	5		RESISTOR 2764	U5-9
13	2		RESISTOR 74LS646	U2,3
12	3		RESISTOR 74LS645	U21-23
11	1		RESISTOR 74LS257A	U11
10	2		RESISTOR 74LS244	U1,24
9	1		RESISTOR 74LS243	U25
8	1		RESISTOR 74LS123	U26
7	1		RESISTOR 74LS74	U15
6	2		RESISTOR 74S74	U17,19
5	1		RESISTOR 74LS20	U18
4	1		RESISTOR 74LS08	U16
3	1		INTEGRATED CIRCUIT 74S04	U20
2				
1	1		PRINTED CIRCUIT BOARD	
ITEM	QTY	PART NUMBER	DESCRIPTION	DESIGNATION

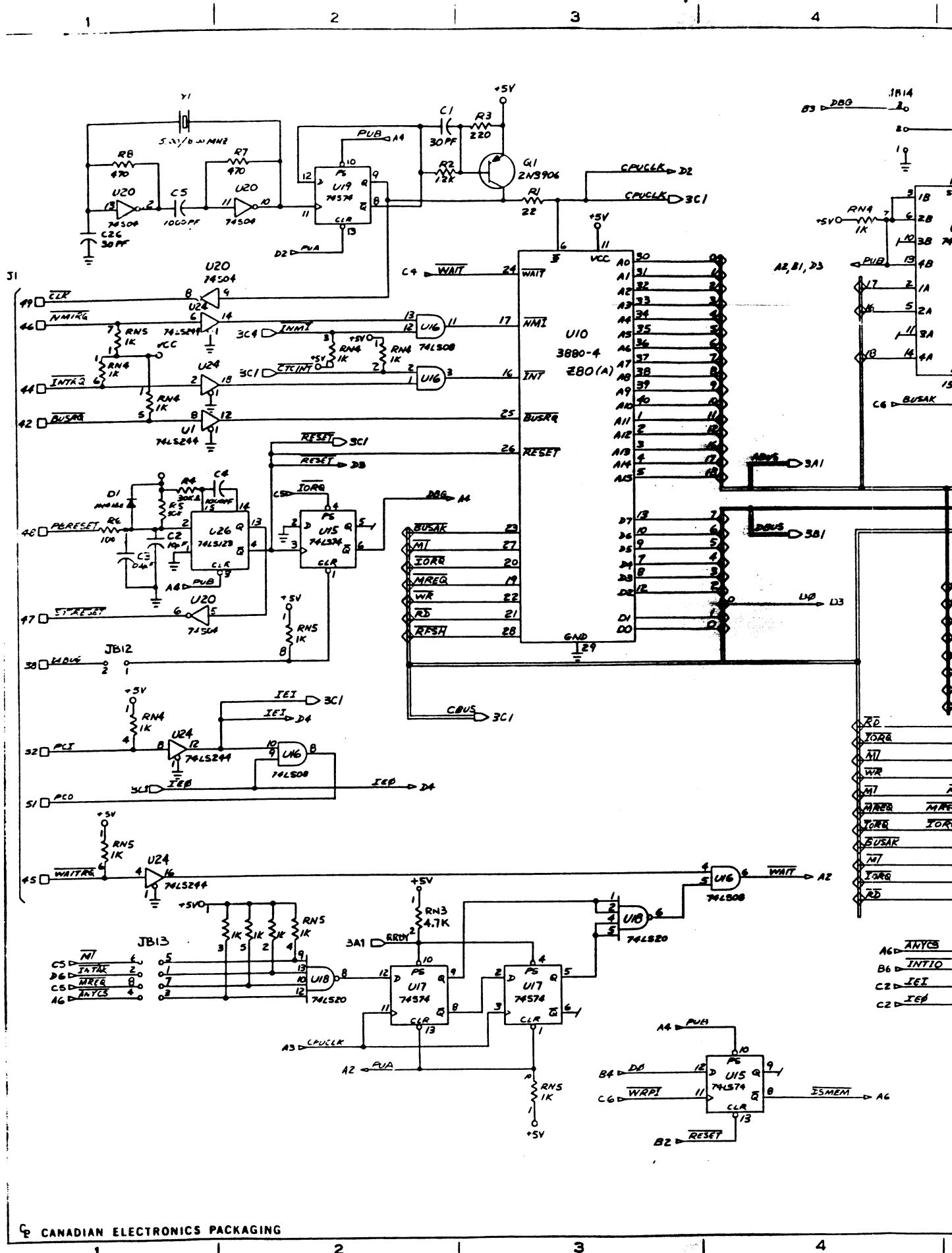
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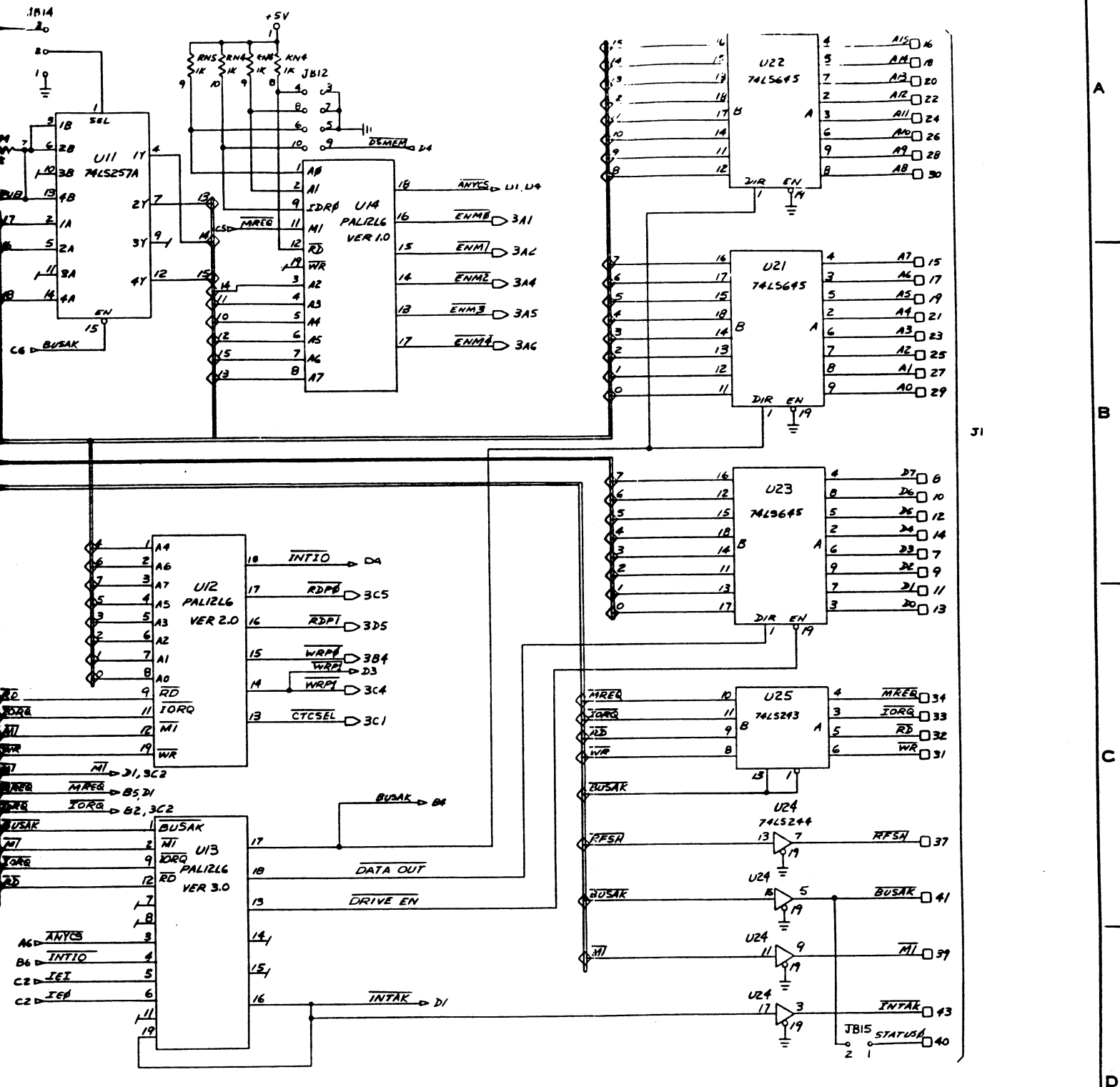
IC POWER PINS					
TYPE	+12	-12	+5	-5	GND
74S04			14		7
74LS06			14		7
74LS20			14		7
74S74			14		7
74LS74			14		7
74LS123			16		8
74LS243			14		7
74LS244			20		10
74LS257A			16		8
74LS645			20		10
74LS646			24		12
2764			28,26		14
3680-4 Z80(A)			11		29
3682-4 CTC			24		5
PAL12L6			20		10

UNUSED GATES



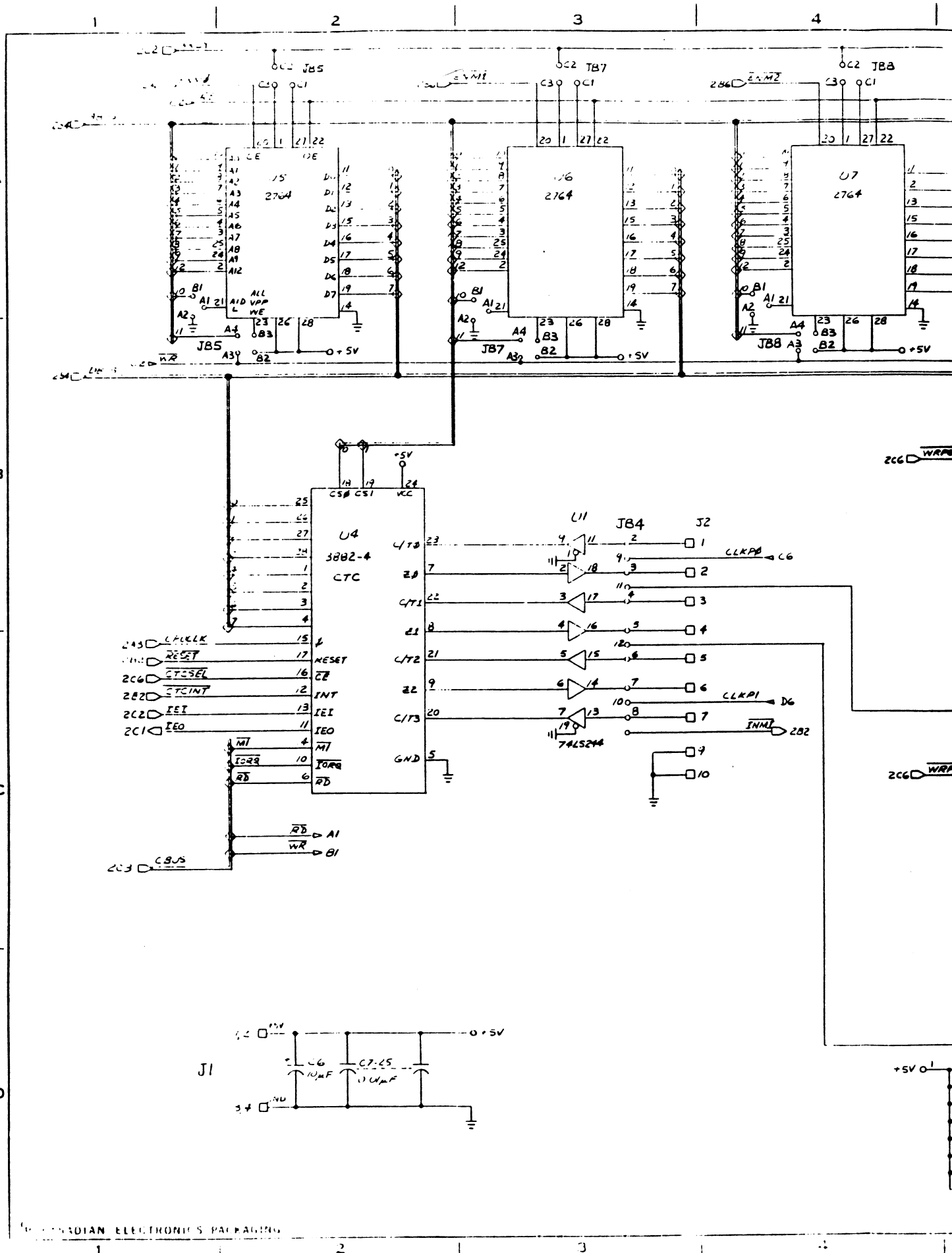
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APPD	TOL .00 .000	MAT'L	FINISH
TITLE DSTD IOI			
DWG NO	CY00-139 1-A1-3	ISS 3	SH 1 OF 1



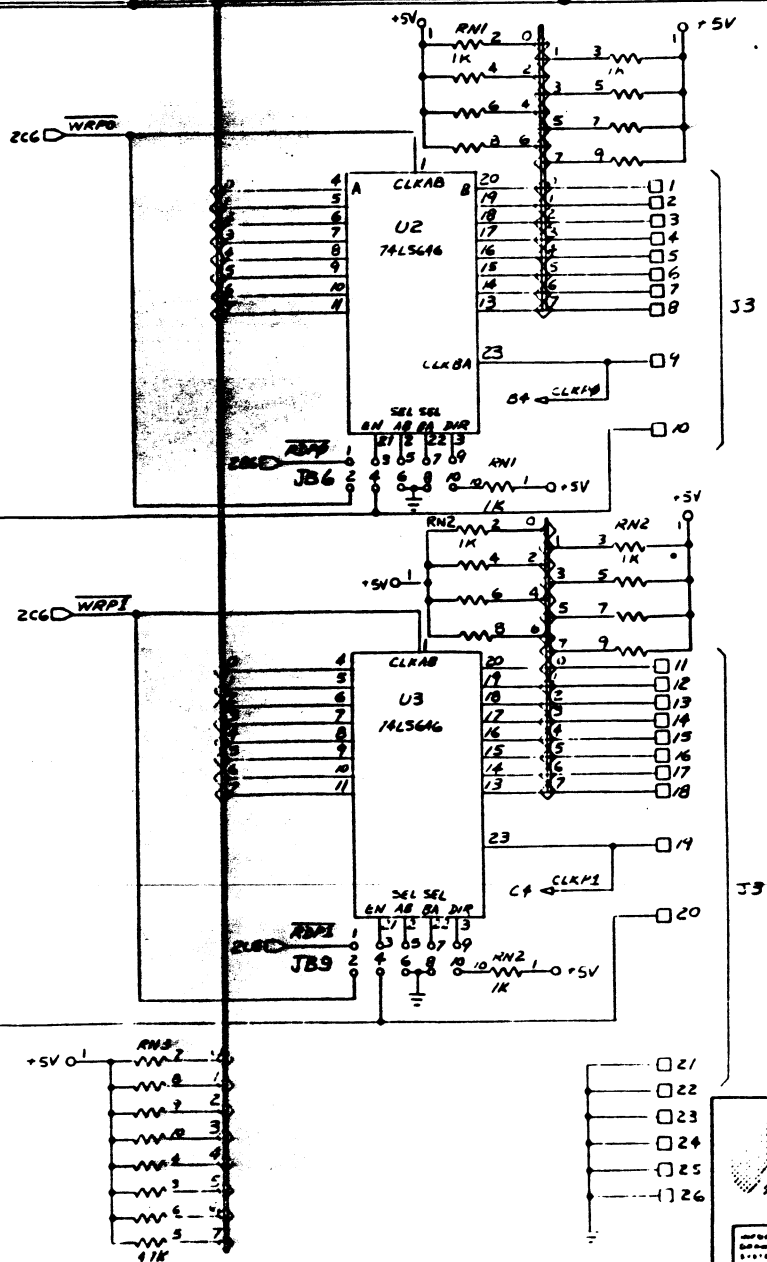
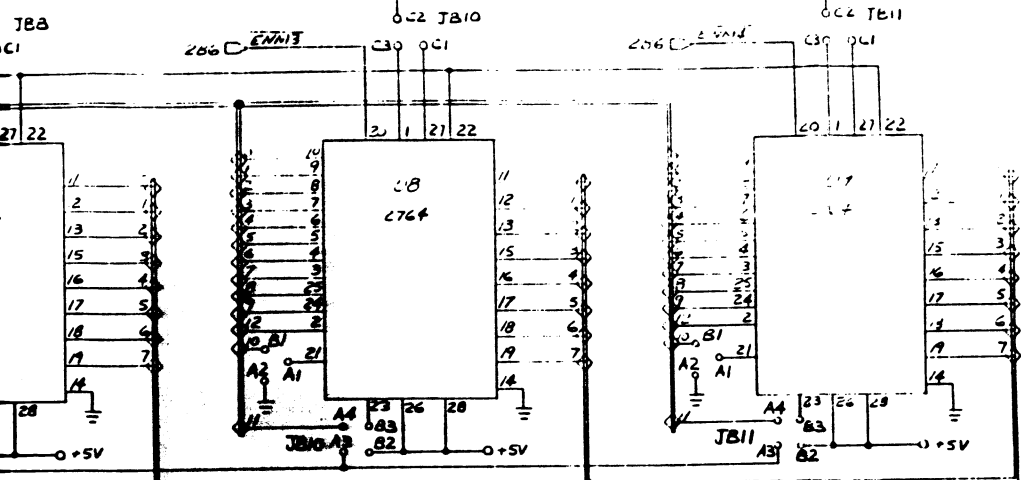


<b>CPU AND PARALLEL I/O</b>			
SCALE	DRN T. WILLIAMS	CHK W. MILAM	DATE 27 APR 81
APP'D	TOL .00 000	MAT L	FINISH
TITLE DSTD IOI			
DWG NO.	DY00439-I-A2-3	ISS 3	SH 2 OF 3

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ISSUE	DESCRIPTION	DATE	UNN	CHK
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CPU AND PARALLEL I/O			
SCALE	DRN WILLIAMS	CHK W. PARLATT	DATE 1 APR 71
APP D	TOL 00 000	MAT L	FINISH
TITLE DSTD IOI			
DWG NO	DYGO 4 1 1 A 3-3	ISS	1 9 1 3

**APPENDIX E**

**PARALLEL PORT REGISTER ELECTRICAL SPECIFICATIONS**

**74LS646/7/8/9**

TTL  
LSI

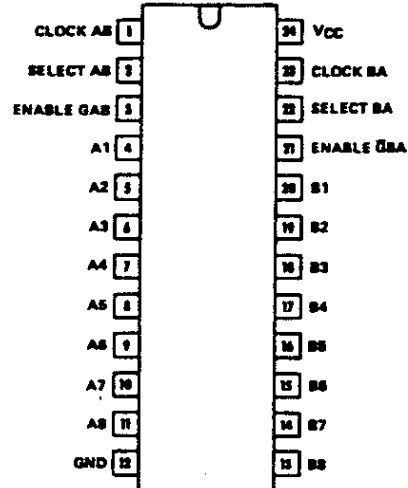
# TYPES SN54LS646 THRU SN54LS649 SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2581, JANUARY 1981

- Bidirectional Bus Transceivers/Registers in the New JT and NT 24-pin 300-mil Packages
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

SN54LS\* ... JT PACKAGE  
SN74LS\* ... JT OR NT PACKAGE  
(TOP VIEW)

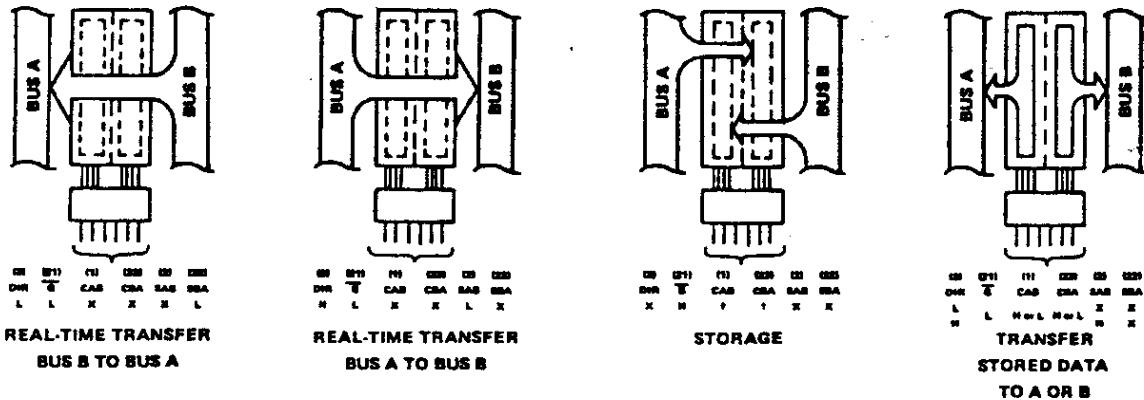


## description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control  $\bar{G}$  and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\bar{G}$  is active (low). In the isolation mode (control  $\bar{G}$  high), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled, and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS646, 'LS647, 'LS648, or 'LS649.





# TYPES SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

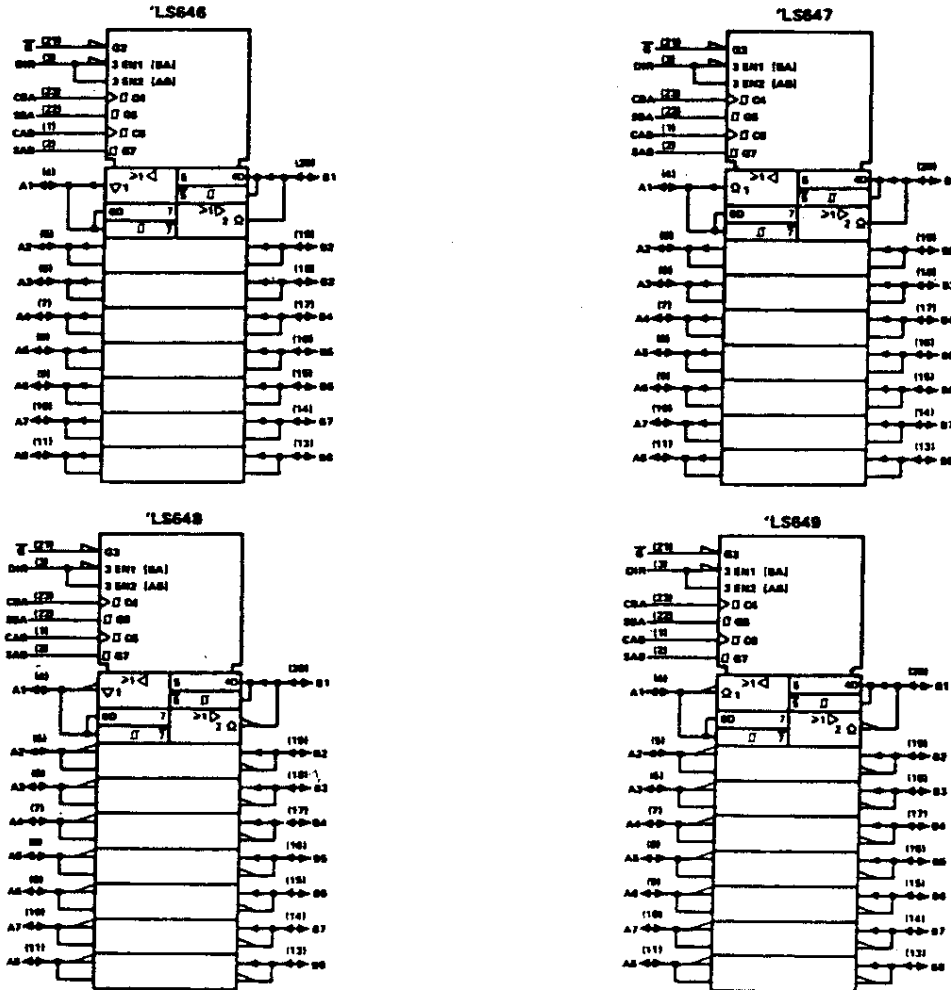
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\bar{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS646, 'LS647	'LS648, 'LS649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\bar{B}$ Data to A Bus
L	L	X	X	X	H	Output	Input	Stored B Data to A Bus	Stored $\bar{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time A Data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A Data to B Bus	Stored $\bar{A}$ Data to B Bus

H = high level L = low level X = irrelevant ↑ = low-to-high-level transition

\*The data output functions may be enabled or disabled by various signals at the  $\bar{G}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

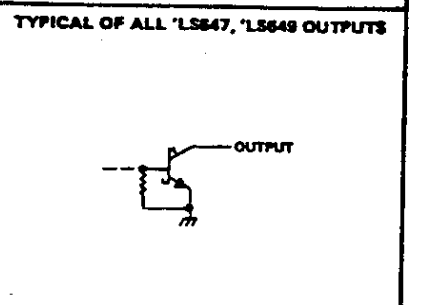
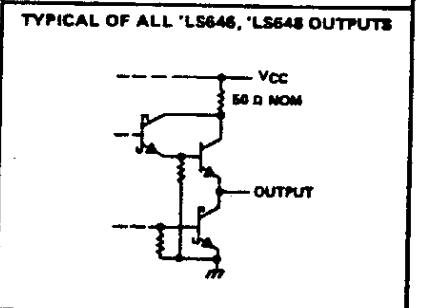
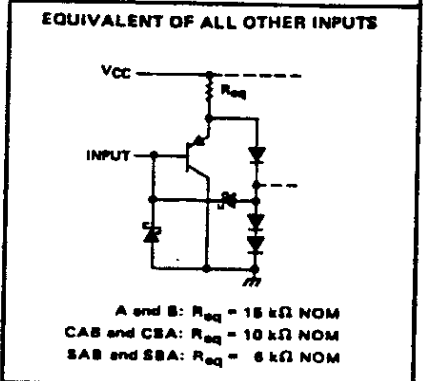
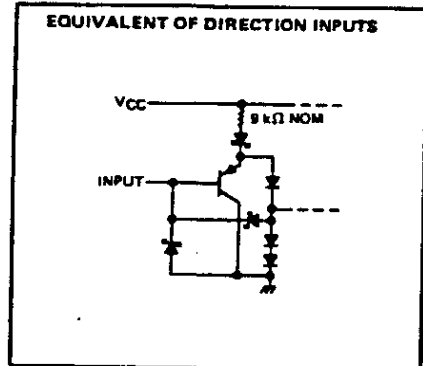
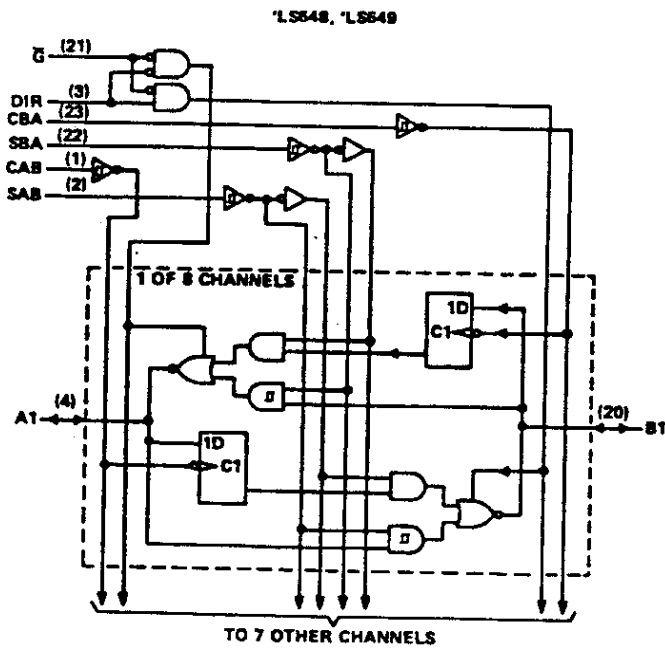
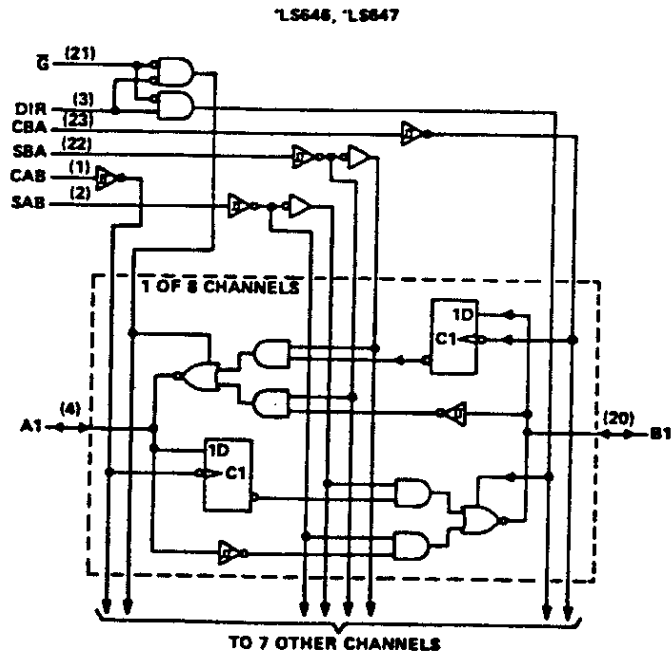
logic symbols



# TYPES SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS

functional block diagram (positive logic)

schematics of inputs and outputs



## TYPES SN54LS646, SN54LS648, SN74LS646, SN74LS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature: SN54LS646, SN54LS648	-55°C to 125°C
SN74LS646, SN74LS648	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-12			-15	mA
Low-level output current, $I_{OL}$			12			24	mA
Width of clock pulse, $t_{W}$	20			20			ns
Setup time, $t_{SU}$		Bus to clock		20			ns
Hold time, $t_H$		Bus from clock		0			ns
Operating free-air temperature, $T_A$	-55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.5			0.5	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ( $V_{T+} - V_{T-}$ ), A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL \text{ max}}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4	2.4	3.4		V
		$I_{OH} = \text{MAX}$	2		2			
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 12 \text{ mA}$		0.25	0.4	0.25	0.4	V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5	
$I_{OZH}$ Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$ , $V_O = 2.7 \text{ V}$			20			20	μA
$I_{OZL}$ Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$ , $V_O = 0.4 \text{ V}$			-400			-400	μA
$I_I$ Input current at maximum input voltage	A or B	$V_{CC} = \text{MAX}$		$V_I = 5.5 \text{ V}$			0.1	mA
	All others	$V_{CC} = \text{MAX}$		$V_I = 7 \text{ V}$			0.1	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_{IH} = 2.7 \text{ V}$			20			20	μA
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_{IL} = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}$ Short-circuit output current <sup>§</sup>	$V_{CC} = \text{MAX}$ , $V_O = 0$	-40		-225	-40		-225	mA
$I_{CC}$ Total supply current	'LS646	$V_{CC} = \text{MAX}$ , Outputs open	Outputs high	91	145	91	145	mA
			Outputs low	103	165	103	165	
			Outputs at Hi-Z	103	165	103	165	
	'LS648	$V_{CC} = \text{MAX}$ , Outputs open	Outputs high	78		78		
			Outputs low	86		86		
			Outputs at Hi-Z	88		88		

<sup>†</sup>For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>§</sup>Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

**TYPES SN54LS646, SN54LS648, SN74LS646, SN74LS648**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER <sup>o</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	Clock	Bus	$R_L = 667\ \Omega$ , $C_L = 45\ \text{pF}$ , See Note 2	15	25		15		ns	
$t_{PHL}$				23	35		26		ns	
$t_{PLH}$	Bus	Bus		12	18		25		ns	
$t_{PHL}$				13	20		23		ns	
$t_{PLH}$	Select, with bus input high <sup>†</sup>	Bus		33	50		36		ns	
$t_{PHL}$				14	25		36		ns	
$t_{PLH}$	Select, with bus input low <sup>†</sup>	Bus		26	40		27		ns	
$t_{PHL}$				21	35		27		ns	
$t_{PZH}$	Enable	Bus		33	55		30		ns	
$t_{PZL}$				42	65		38		ns	
$t_{PZH}$	Direction	Bus	28	45		24		ns		
$t_{PZL}$			39	60		35		ns		
$t_{PHZ}$	Enable	Bus	$R_L = 667\ \Omega$ , $C_L = 5\ \text{pF}$ , See Note 2	23	35		23		ns	
$t_{PLZ}$				22	35		22		ns	
$t_{PHZ}$	Direction	Bus		20	30		23		ns	
$t_{PLZ}$				18	30		19		ns	

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

$t_{PZH}$  = output enable time to high level

$t_{PZL}$  = output enable time to low level

$t_{PHZ}$  = output disable time from high level

$t_{PLZ}$  = output disable time from low level

<sup>†</sup> These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.

## TYPES SN54LS647, SN54LS649, SN74LS647, SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649	-55°C to 125°C
SN74LS647, SN74LS649	-0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$ (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, $V_{OH}$			5.5			5.5	V
Low-level output current, $I_{OL}$			12			24	mA
Width of clock pulse, $t_w$	20			20			ns
Setup time, $t_{su}$	Bus to clock		20	Bus to clock		20	ns
Hold time, $t_h$	Bus from clock		0	Bus from clock		0	ns
Operating free-air temperature, $T_A$	-55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS647 SN54LS649		SN74LS647 SN74LS649		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
$V_{IH}$ High-level input voltage		2		2		V	
$V_{IL}$ Low-level input voltage			0.5		0.6	V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5		-1.5	V	
Hysteresis ( $V_{I+} - V_{I-}$ ), A or B input	$V_{CC} = \text{MIN}$	0.1	0.4	0.2	0.4	V	
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$		100		100	μA	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$		0.25	0.4	0.25	0.4	V
	$I_{OL} = 24 \text{ mA}$				0.35	0.5	
$I_I$ Input current at maximum input voltage	A or B				0.1	0.1	mA
	All others	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			0.1	0.1	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.5 \text{ V}$		20		20	μA	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4		-0.4	mA	
$I_{CC}$ Total Supply Current	LS647	$V_{CC} = \text{MAX},$ Outputs open	79	130	79	130	mA
		Outputs high	94	150	94	150	
	LS649	$V_{CC} = \text{MAX},$ Outputs high	76		76		
		Outputs open	90		90		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All Typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

**TYPES SN54LS647, SN54LS649, SN74LS647, SN74LS649**  
**OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	Clock	Bus	$R_L = 687\ \Omega$ , $C_L = 45\ \text{pF}$ , See Note 2	22	35		24		ns	
$t_{PHL}$				28	45		26		ns	
$t_{PLH}$	Bus	Bus		17	26		23		ns	
$t_{PHL}$				18	27		23		ns	
$t_{PLH}$	Select, with bus input high†	Bus		39	60		42		ns	
$t_{PHL}$				19	30		36		ns	
$t_{PLH}$	Select, with bus input low†	Bus		33	50		36		ns	
$t_{PHL}$				29	45		27		ns	
$t_{PLH}$	Enable	Bus		25	40		25		ns	
$t_{PHL}$				33	50		35		ns	
$t_{PLH}$	Direction	Bus		23	35		32		ns	
$t_{PHL}$				25	40		29		ns	

$t_{PLH}$  = propagation delay time, low-to-high-level output

$t_{PHL}$  = propagation delay time, high-to-low-level output

† These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition.