OPERATIONS MANUAL

Early version

DSTD 102 CPU AND SERIAL I/O

DY00449 Rev 4.

dy-4 Systems Inc.

Document No. DSTD-102-M
Revision 4

DSTD-102 CPU AND SERIAL I/O

OPERATION MANUAL

DY00449

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DATED: JANUARY 18, 1983

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SECTION 2

2.0 FUNCTIONAL HARDWARE DESCRIPTION

2.1 Introduction

The DSTD-102 utilizes a Z80 microprocessor as the system controller. It features three 28 pin memory sockets which enables the user to populate the module with any combination of designated ROM and EPROM. Custom address decoding allows the user to configure the memory on any 8K boundary of the 64K memory map. A PAL decoder is supplied to allow the user to choose one of two popular memory configurations, or if desired the user may implement other mixtures of memory devices simply by programming the PAL accordingly.

A 4 channel counter/timer circuit is included for software controlled counting and timing functions. On-board strapping options make it possible to cascade the four CTC channels for long count sequences. The CTC may also be used as a baud rate generator for the serial channels if non-standard baud rates are required.

The DSTD-102 has two serial channels implemented using the Z80-SIO LSI chip. The SIO allows for both asynchronous and synchronous (SDLC, HDLC, BISYNC, etc.) modes. Channel A can be used as both asynchronous and synchronous modes and channel B provides asynchronous operation. (Synchronous operation is available on the DSTD-102A version of the board - not the standard DSTD-102.) Channel A has additional RS-232C drivers and receivers for external clocks. In asynchronous mode both channels will operate up to 19.2k baud using the baud rate generator. The CTC may be used for higher rates. Channel A will run to 307kilo baud in synchronous mode.

A strapping option allows the user to select the reset address to be either 0000H or E000H. The E000H option is required for use of standard software and hardware products including dy-4 SYSTEMS Debug Monitor (DDM) and Disk Control Monitor (DCM) firmware products. Also these products require onboard RAM strapped to reside at location FC00H to FFFFH.

The DSTD-102 is available in 2.5 MHz and 4 Mhz versions.

2.2 Block Diagram Description

Figure 2 - 1 is a block diagram illustrating the flow of system address, data and control signals on the DSTD-102. The following paragraphs describe the function of each of the major blocks.

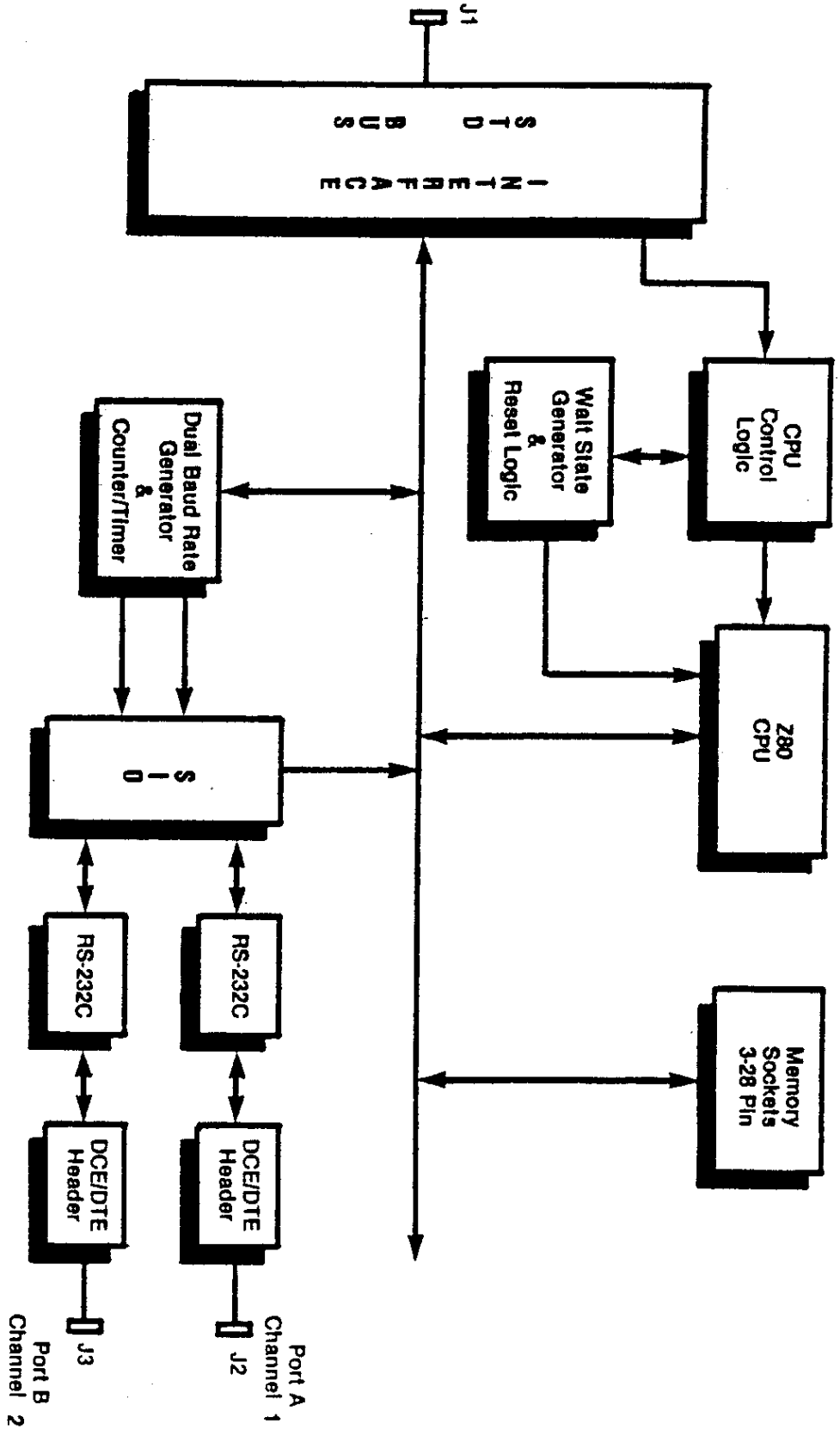


FIGURE 2 - 1 FUNCTIONAL BLOCK DIAGRAM

2.2.1 CPU

The Z80 is the system controller. It fetches, decodes and executes instructions from memory and generates the necessary address and control signals to co-ordinate data flow between the CPU and memory or between the CPU and system I/O devices.

2.2.2 Clock Generator

The DSTD-102 has a crystal controlled oscillator to generate the basic clock signals for the CPU and peripheral chips. A divide-by-two circuit ensures a 50% duty cycle and an active pullup circuit ensures proper clock levels. An inverted clock is supplied to the bus for use by other modules.

2.2.3 CTC (Counter/Circuit)

The Counter/Timer Circuit (MK3882/Z80-CTC) provides four independent, programmable channels for either software or hardware controlled counting and timing functions. Each channel can be configured by the CPU for various modes of operation and the built-in daisy chain priority interrupt logic provides for automatic, independent interrupt vectoring. The I/O port addresses for the CTC are hard-wired as follows:

I/O PORT ADDRESS	CTC CHANNEL
7C	0
7D	1
7E	2
7F	3

A strapping option has also been included to permit any or all of the four CTC channels to be cascaded for long count sequences.

Section 3 provides the necessary information for utilizing this option. For a complete description of the CTC operation, refer to either the Mostek MK3882 or Zilog Z80-CTC Technical Manual.

2.2.4 Memory

The DSTD-102 has been designed to accommodate any combination of the byte-wide RAM, ROM and EPROM devices. Three 28-pin sockets have been provided, each of which may be strapped for any of the allowable memory types. These user-selectable options are fully described in Section 3.

2.2.5 Decode Logic

This section consists primarily of a PAL which decodes the high order six bits of memory address and generates the applicable chip select if on-board memory is to be selected. The PAL provides for two separate memory configurations. The first places the memory starting at 0000H. The second places the memory starting at E000H. A strapping option must be hard-wired to the desired configuration as explained in Section 3.

The DSTD 102 has a latch to disable all on-board memory under software control. On power-up and reset, the latch is preset enabling the on board memory.

On-board memory is disabled by writing an '1' to I/O port 07BH. The on-board memory can be re-enabled by writing a '0' to port 07BH.

2.2.6 Reset Control Logic

This is a strapping option that causes a hardware-forced memory starting address upon system reset. A reset address of either 0000H or E000H may be selected.

This logic is required for use of standard MOSTEK hardware and software products including DDT-80, FLP-80DOS/MDX, MDX-SST, and MDX-DEBUG and dy-4 Debug Monitor (DDM) and CP/M software.

2.2.7 Wait State Generator

This function, if enabled, causes memory read and write cycles to be lengthened by one clock period in order to allow sufficient access time when slower memory devices are used. Wait states can be enabled selectively, namely, - all memory cycles or opcode fetch cycles only or all memory cycles access on-board memory devices or all opcode fetch cycles and all memory cycles accessing onboard memory. An additional wait state may also be inserted during INTAK cycles.

2.2.8 Serial Ports

The DSTD-102 has two RS-232C serial ports implemented using the Z80-SIO/MK3884. Each port has a software programmable baud rate generator. The baud rate is set by writing to port 7AH. The least significant 4 bits set the baud rate for Channel A and the most significant 4 bits are for Channel B. Both Channels will operate from 12.5 baud to 19.2K baud. In additon the CTC may be used to generate the receive and transmit data clocks of Channel A allowing for non-standard baud rates. The CTC can only be used for asynchronous modes because it does not generate a 50% duty cycle clock. Channel A also has additional RS-232C drivers and receivers to enable it to handle external clocks for full synchronous operation (SDLC, HDLC, BYSYNC, MONOSYNC etc.).

SECTION 3

USER-SELECTABLE OPTIONS

3.1 Introduction

The DSTD-102 incorporates many strapping options to provide the user with a high degree of flexibility in system configurations. This section describes the use of the available jumper options.

3.2 Debug/Single Step Configurations

The DSTD-102 supports the MDX-SST module. This module generates a NMI (non-maskable interrupt) and asserts the DEBUG signal. This debug signal when enabled forces a logic '1' onto the most significant three bits of the address bus. Thus the interrupt service routine is located at E066H. If the debug is disabled the interrupt service routine is at the normal address (0066H). To enable the debug line, install a jumper between JB8-2 and JB8-3 and between JB12-3A to JB12-3B. Ensure that the memory option strap position the monitor software at E000H. dy-4 SYSTEMS' DDM firmware supports the single step facilities.

3.3 Memory Options

The PAL memory decoder shipped with DSTD-102 from the factory supports the options discussed in the following sections.

3.3.1 Restart Address

The DSTD-102 is capable of starting execution at either 0000H or E000H after reset. Reset address E000H is implemented in hardware. Since the program counter (internal to the Z80 microprocessor) always resets to 0000H it must be updated to the correct address (E000H) immediately following the reset. The hardware latch forcing the address must then be cleared. This is accomplished automatically by executing any I/O port read or write instruction (or an interrupt acknowledge cycle). If no port access is normally made then a "dummy" I/O read or write to an unused port address must be inserted. Otherwise, memory access will be contrained to address E000H through FFFFH. To ensure proper operation after reset, the following code sequence should be placed in memory at the E000H.

```
E000        C3 03 E0      JP E003H      ; jump instruction
                                        ; to update program
                                          counter
E003        DB nn         IN A,(nn)     ; read unused I/O
                                        ; port nn to clear
                                        ;resetaddress latch
E005                                    ; first instruction
                                        ; of user program
```

If using standard dy-4 SYSTEMS' or Mostek software (including DDM,DCM, DDT-80, FLP-80, DOS/MDX or MDX-DEBUG), the reset address must be E000H. The program counter and address latch modification instructions previously described are already contained with the DDM ROM. Ensure that pins 2 and 3 of JB8 are connected when the MDX-SST module is used.

3.3.2 Memory Configuration

The DSTD-102 incorporates three 28 pin sockets which can be independently configured to accept a variety of pin compatible memory devices. Tables 3 - 1A, 3 - 1B and 3 - 1C list each socket, its corresponding jumper block, and its address space for the standard configurations. Table 3 - 2 illustrates the necessary jumper connections for configuring a socket to accept a particular memory device. The third socket is typically used for RAM. A 4118 (1kx8) chip positioned at FC00H is required for most standard firmware packages.

The DSTD-102 is shipped from the factory with a memory decoding PAL (U26) which supports the two most popular memory configurations (using 2k byte chips). A detailed description of these configurations follows. The factory can supply memory decoding PAL's on request for other standard configuration using 4k byte and 8k byte chips. Consult the factory for PAL programming details for non-standard requirements.

The two standard (EPROM) socket configurations allow for the use of 2k byte chips (2716 EPROMS, 4802 RAMS). Note that 1k byte chips may be used, however, this results in 1k byte gaps in the address space. The chips occupy contiguous memory locations on an 8k byte address boundary. In the first configuration (Address option 0)the memory sockets occupy address 0000H through 17FFH. This is achieved by installing a strap between J13-1A and J13-1B. The memory sockets may be configured for EPROM or RAM as shown in table 3 - 2.

In the second configuration (Address option 1) the memory sockets occupy addresses E000H through FFFFH.

TABLE 3 - 1A

MEMORY SOCKET/JUMPER BLOCK ASSIGNMENT FOR 2K DEVICES

Socket	Address Option 0	Address Option 1	Jumper Block
U20	0000 - 07FF	E000 - E7FF	JB11
U19	0800 - 0FFF	E800 - EFFF	JB10
U18	1000 - 17FF	FC00 - FFFF	JB9

TABLE 3 - 1B

MEMORY SOCKET/JUMPER BLOCK ASSIGNMENT FOR 4K DEVICES

Socket	Address Option 0	Address Option 1	Jumper Block
U20	0000 - 0FFF	D000 - DFFF	JB11
U19	1000 - 1FFF	E000 - EFFF	JB10
U18	2000 - 2FFF	F000 - FFFF	JB9

TABLE 3 - 1C

MEMORY SOCKET/JUMPER BLOCK ASSIGNMENT FOR 8K DEVICES

Socket	Address Option 0	Address Option 1	Jumper Block
U20	0000 - 1FFF	A000 - BFFF	JB11
U19	2000 - 3FFF	C000 - DFFF	JB10
U18	4000 - 5FFF	E000 - FFFF	JB9

Table 3 - 2 shows the straps necessary to configure the sockets for the different memory types. All the sockets are wired independently, allowing any mix of chips within the addressing constraints.

TABLE 3 - 2 MEMORY SOCKET CONFIGURATION

MEMORY	JUMPER CONNECTIONS
2758	B1 - B2 A4 - A3 OPEN A1,A2,B3
2759	B1 - A4 A4 - A3 OPEN A1,A2,B2,B3
2716	B1 - A1 A4 - A3 OPEN B2,A2,B3
2732	B1 - A1 A3 - A2 OPEN B2,A2,B3
2764	B2 - A1 A4 - A2 OPEN B2,A2,B3
4118/4801	B3 - A3 B1 - A4 OPEN A1,A2,B2
4802	B3 - A3 A1 - B1 OPEN A2,B2,A4

Table 3 - 3 shows the JB13 straps necessary for the two standard configurations.

TABLE 3 - 3

MEMORY ADDRESS/ENABLE OPTIONS

ADDRESS	JUMPER CONNECTION JB13
Sockets 0000H - 17FFH	3A - 3B
Sockets E000H - FFFFH	3A,3B open

3.3.3 On-board Memory Disable Latch

All on-board memory can be enabled and disabled under software control. To use this feature jumper JB13 4A-4B is installed. This allows the memory disable latch to be accessed. This latch is located at address 7BH. Writing a '0' to this latch enables on-board memory; writing a '1' disables on-board memory. A power-up or RESET clears the latch enabling on-board memory.

3.4 WAIT State Generator

Three jumpers are provided to allow the use of slow memory devices. The first jumper generates a WAIT state on all memory cycles. The second jumper generates a WAIT state for M1 memory cycles only. Table 3 - 4 lists the access times of memory devices internal and external to the card for the two different memory cycle types for both the 2.5 MHz and 4.0 MHz DSTD 102 cards. The third jumper generates a WAIT state on internal memory accesses only. Thus EPROMS can be used along with a high speed RAM card. A fourth jumper allows the generation of a WAIT state on interrupt acknowledge cycles. Table 3 - 5 gives the connections for the WAIT state options.

TABLE 3 - 4A

M1-MEMORY CYCLE WAIT STATES TIMING 2.5MHz

FUNCTION	JB10 Connections	INTERNAL M1	INTERNAL Other	EXTERNAL M1	EXTERNAL Other
No WAIT states	---	580	780	550	750
WAIT states on M1 cycle	5A to 5B	620	780	950	750
WAIT states on all memory cycles	7A to 7B	620	1180	950	1150

(in nanoseconds)

TABLE 3 - 4B

M1-MEMORY CYCLE WAIT STATES TIMING 4.0MHZ

FUNCTION	JB10 Connections	INTERNAL M1	INTERNAL Other	EXTERNAL M1	EXTERNAL Other
No WAIT states	---	340	455	300	425
WAIT states on M1 cycle	5A to 5B	590	455	560	425
WAIT states on all memory cycles	7A to 7B	590	705	560	675

(in nanoseconds)

TABLE 3 - 5 WAIT STATE OPTIONS

OPTION	JUMPER BLOCK 13
No WAIT states	No Jumpers
All M1 cycles	5A to 5B
All Memory cycles	7A to 7B
Internal Memory cycles only	8A to 8B
Internal Memory cycles and external M1 cycles	8A to 8B 5A to 5B
Interrupt acknowledge cycle	6A to 6B

3.5 Counter/Timer Options

The four Counter/Timer channels may be cascaded for extended counting and timer functions. Table 3 - 6 shows the jumper pin number for the CTC. Refer to the MK3882 Technical Manual or the Zilog Data Book for a complete description of the CTC operation.

Provision is made on the Counter/Timer option block to enable the NMI input of the processor to be connected to one of the outputs of the CTC. NMI is pin 5A of JB5.

In addition the CTC can be used as a baud rate generator for the serial channels to create non-standard baud rates.

Two commonly unused pins on the STD bus (MEMEX and IOEXP) may be connected through JB12 and buffers to the CTC. One pin is used as an input (IOEXP) and the other is used as an output (MEMEX).

3.6 Serial Channel Options

3.6.1 Baud Rate Generator

The DSTD-102 has a dual software-programmable baud rate generator. It is accessed through I/O port 7AH. This port is a write-only port. Bits 0 to 3 control channel A and bits 4 to 7 control channel B. Table 3 - 7 shows the programming information for the baud rate generator.

Table 3 - 6

Baud Rate Generator Programming

BAUD RATE	D3/D7	D2/D6	D1/D5	D0/D4	(HEX)
19,200	1	1	1	1	F
9,600	1	1	1	0	E
7,200	1	1	0	1	D
4,800	1	1	0	0	C
3,600	1	0	1	1	B
2,400	1	0	1	0	A
2,000	1	0	0	1	9
1,800	1	0	0	0	8
1,200	0	1	1	1	7
600	0	1	1	0	6
300	0	1	0	1	5
150	0	1	0	0	4
134.5	0	0	1	1	3
110	0	0	1	0	2
75	0	0	0	1	1
50	0	0	0	0	0

Thus to set port A to 9600 baud and port B to 1200 baud output a 7EH to I/O address 7AH.

3.6.2 DTE/DCE Configurations

3.6.2.1 DCE Configuration

When connecting to a CRT, printer or similar equipment the serial port is wired as Data Comunications Equipment. The signal names indicate control and data flow with respect to the CRT. Table 3 - 7 itemizes the jumper configurations for this mode of operation.

TABLE 3 - 7

RS-232C DCE Jumper Configuration

EIA Signal Name	Installed Jumpers JB3,JB4	J1/J2 Pin Numbers
RX	1A to 1B	2
TX	2A to 2B	3
CTS	3A to 3B	4
RTS	4A to 4B	5
DCD	6A to 6B	9
DTR	7A to 7B	8
DSR	JB3-8A to B, JB4-12A to B	6

3.6.2.2 DTE Configuration

When connecting to a MODEM or similar equipment the serial port is wired as Data Terminal Equipment. The signal names indicate control and data flow with respect to the DSTD-102. Table 3 - 8 itemizes the jumper configuration for the mode of operation.

TABLE 3 - 8

RS-232C DTE Jumper Configuration

Signal Name	Installed Jumpers	J1/J2 Pin Numbers
RX	1B to 2B	2
TX	1A to 2A	3
CTS	4A to 5A	4
RTS	4B to 5B	5
DCD	7A to 6B	9
DTR	6A to 7B	8
DSR	--	6

3.6.3 Synchronous Operation

The DSTD-102A allows synchronous operation on Channel A. That is, additional RS-232C drivers and receivers are provided for interfacing external clocks. Two configurations are possible.

i) The DCE provides both transmit and receive timing information. When the DSTD-102A is the DCE, two RS-232C drivers are required. When the DSTD-102A is the DTE two RS-232C receivers are required.

ii) The DCE provides the transmit timing information and the DTE provides the receive timing information. The DSTD-102A provides the receive timing information. The DSTD-102 uses both the RS-232C driver and the RS-232C receiver.

Table 3 - 9 shows the jumpering required for each configuration. Note that the same drivers used for the external clocks are also used to drive the on-board TX and RX LED's. When these drivers are to be used for external clocking the LED's should be disconnected.

TABLE 3 - 9

DCE provides both clocks. DSTD-102A is the DCE

	JB2	JB3	J2	EIA
TX Clock	2A - 2B 1A - 2A	9A - 9B	10	15
RX Clock	3A - 4A 4A - 4B	11A - 11B	11	17

DCE provides both clocks. DSTD-102A is the DTE

	JB2	JB3	J2	EIA
TX Clock	1A - 1B	8A - 8B	10	15
RX Clock	3A - 3B	10A - 10B	11	17

DTE provides the transmit clock. DCE provides the receive clock. DSTD-102A is DCE.

	JB2	JB3	J2	EIA
TX Clock	1A - 2A 2A - 2B	9A - 9B	10	24
RX Clock	3A - 3B	10A - 10B	11	17

DTE provides the transmit clock, DCE provides the receive clock. DSTD-102A is DTE.

	JB2	JB3	J2	EIA
RX Clock	1A - 1B	8A - 8B	10	24
TX Clock	2A - 3A 4A - 4B	11A - 11B	11	17

Note that the clock names given above refer to data flow with respect to the DTE. EIA refers to the DB25 pin numbers assigned to these signals by the EIA RS-232C specifications.

Table 3-10 shows the cable connections to a standard RS-232C DB25S connector. Typically the cable is the same for both DCE and DTE systems with the configuration being determined by the on-based jumpers.

TABLE 3-10

SERIAL CABLE CONNECTIONS

J2/J3	RS232C/DB25S	EIA CIRCUIT
1	1	AA
2	2	BA
3	3	BB
4	4	CA
5	5	CB
6	6	CC
7	7	AB
8	8	CF
9	20	CD
10	15	DB
11	17	DD
12	19	

SECTION 4

SPECIFICATIONS

4.1 Functional Specifications

4.1.1 Word Size

Instructions:	8, 16, 24, or 32 bits
Data:	8 bits

4.1.2 Cycle Time

Clock period (T state):	400 ns for DSTD-102-2.5 250 ns for DSTD-102-4.0
Instruction Cycle:	Min. 4 T states Max. 23 T states

4.1.3 Memory Capacity

Three 28 pin sockets are provided which may be populated with any mixture of the following devices:

2758 (1K x 8 EPROM)
2716 (2K x 8 EPROM)
2732 (4K x 8 EPROM)
2764 (8K x 8 EPROM)
MK 34000 (2K x 8 EPROM)
4118 (1K x 8 Static RAM)
4801 (1K x 8 Static RAM)
4802 (2K x 8 Static RAM)
TMS4016 (2K x 8 RAM)

4.1.4 Memory Access Time

The time required to access on-board memory by external DMA controllers is 100 ns plus the access time of the memory device. This is defined as the time interval between the time that the memory address is valid on the STD-BUS and the time that the output data is valid on the STD-BUS.

4.1.5 I/O Addressing

The on-board I/O addressing is hard wired to the following port addresses:

PORT				ADDRESS
BAUD RATE GENERATOR				7A
ON-BOARD DISABLE LATCH				7B
CTC	CH	0		7C
CTC	CH	1		7D
CTC	CH	2		7E
CTC	CH	3		7F
SIO	CH	A	DATA	BC
SIO	CH	A	CONTROL	BD
SIO	CH	B	DATA	BE
SIO	CH	B	CONTROL	BF

4.1.6 I/O Capacity

The Z80 CPU utilizes the lower 8 bits of its address bus for I/O addressing to yield a total of 256 possible port addresses.

4.1.7 Interrupts

The CPU may be programmed to process interrupts in any of three different modes (mode 0, 1, or 2 as described in any Z80 Technical Manual). Mode 2 operation (vectored interrupts) is by far the most powerful and is compatible with dy-4 DSTD and MOSTEK MDX Series cards.

Multi-level interrupt processing is also possible with the Z80 CPU. The level of stacking is limited only by available memory space.

The DSTD-102 will also accept non-maskable interrupts which force a restart at location 0066H.

4.1.8 System Clock

DSTD-102-2.5 2.5MHz + 0.05%

DSTD-102-4.0 4.0MHz + 0.05%

4.2 Electrical Specification

4.2.1 STD Bus Interface

Bus Inputs: One 74LS load max.

Bus Outputs: I_{OL} = 24 mA min. @ V_{OL} = 0.5 Volts
I_{OH} = 15 mA min. @ V_{OH} = 2.4 Volts

4.2.2 Serial Ports

Inputs: One 74LS load max.

Outputs: +/- 12V Current Limited to 10mA

4.2.3 Operating Temperature

0 Degrees C to 50 Degrees C
95% humidity non-condensing

4.2.4 Power Supply Requirements

+5V +/- 5% @ 1.2A
+12V +/- 5% @ 0.1A
-12V +/- 5% @ 0.1A
(excluding memory power requirements)

4.3 Mechanical Specifications

4.3.1 Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm) long

0.48 in. (1.22 cm.) maximum height

0.062 in. (0.16 cm.) printed circuit board thickness

4.3.2 STD Bus Edge Connector

56 pin Dual Readout; 0.125 in. centers

Mating Connector

Viking 3VH28/1CE5 (printed circuit)
Viking 3VH28/1CND5 (wire wrap)
Viking 3VH28/1CN5 (solder lug)

4.3.3 Serial Port Connector

12 Pin Dual Readout; 0.100 inch grid

Mating Connector

Amp 87631-8 (housing)
Amp 86016-2 (contact)
or equivalent

SECTION 5

5.0 FACTORY NOTICES

5.1 Factory Repair Service

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information with the returned circuit board:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

Service Department,
dy-4 SYSTEMS INC.
888 Lady Ellen Place
Ottawa, Ontario
K1Z 5M1 Canada

or

Service Department,
dy-4 SYSTEMS INC.
3582 Dubarry Rd.
Indianapolis, IN 46226

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 Limited Warranty

dy-4 warrants this product against defective materials and workmanship for a period of 1 year. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.There are no warranties which extend beyond those herein specifically given.

APPENDIX A

OPTION PROGRAMMING SUMMARY

APPENDIX A

OPTION PROGRAMMING SUMMARY

A - 1 OPTIONAL JUMPER BLOCKS

The following is a list of the option Jumper Blocks on the STD-102 card.

JB1	LED connection
JB2	Serial Channel A Clock TTL Side
JB3	Serial Channel A DTE/DCE Configuration Block
JB4	Serial Channel B DTE/DCE Configuration Block
JB5	Counter Timer Jumper Block
JB6	LED Transmit
JB7	LED Receive
JB8	Restart Address Jumper Block
JB9	Memory Socket Configuration Block for U18
JB10	Memory Socket Configuration Block for U19 and WAIT State Generator options
JB11	Memory Socket Configuration Block of U20
JB12	CTC/Bus Interface Jumper Block
JB13	On-board Memory Options

A - 2 LED Connections (JB1)

These jumpers are installed to drive the LED's. Note the jumpers should not be installed if Serial Channel A is used in synchronous mode and is supplying the clocks to external equipment.

		A	B	
Driver 1	1	o	o	LED 1
Driver 2	2	o	o	LED 2

---- Indicates Factory Default

A - 3 Serial Channel A Clock Jumpers TTL Side (JB2)

This jumper block allows the selection of the Transmit and receive clocks for Channel A.

		A	B	
Transmit Clock (input)	1	o	o	RS232 Clock Receiver 1
		!		
Internal Baud Rate Generator	2	o	o	RS232 Clock Transmitter 1
Receiver Clock (input)	3	o	o	RS232 Clock Receiver 2
Internal Baud Rate Generator	4	o	o	RS232 Clock Transmitter 2
Receiver Clock (input)	5	o	o	CTC output
		!		
Transmit Clock (input)	6	o	o	CTC output

A - 4 Channel A DTE/DCE Configuration Block (JB3)

These jumpers allow the board to be configured as Data Terminal Equipment or Data Communications Equipment when used with a standard dy-4 SYSTEMS Cable.

		A	B	
Transmit Data	1	o	o	Connector J2 Pin 2
		|	|	
Connector J2 Pin 3	2	o	o	Received Data
Request to Sent (RTS)	3	o	o	Connector J2 Pin 4
Clear to Send (CTS)	4	o	o	Connector J2 Pin 5
Connector J2 Pin 4	5	o	o	Request to Send (RTS)
Data Terminal Ready (DTR)	6	o	o	Connector J2 Pin 9
Data Carrier Detect (DCD)	7	o	o	Connector J2 Pin 8
RS-232C Receiver 1	8	o	o	Connector J2 Pin 10
RS-232C Transmit 1	9	o	o	Connector J2 Pin 10
RS-232C Receiver 2	10	o	o	Connector J2 Pin 11
RS-232C Transmit 2	11	o	o	Connector J2 Pin 11
+12 through 3k ohms	12	o	o	Connector J2 Pin 6

A - 5 Channel B DTE/DCE Configuration Block (JB4)

This jumper block allows the channel to be configured as Data Terminal Equipment or Data Communications Equipment.

		A	B	
Transmit Data	1	o	o	Connector J2 Pin 2
		!	!	
Connector J2 Pin 3	2	o	o	Received Data
Request to Sent (RTS)	3	o	o	Connector J2 Pin 4
		!	!	
Clear to Send (CTS)	4	o	o	Connector J2 Pin 5
Connector J2 Pin 4	5	o	o	Request to Send (RTS)
Data Terminal Ready (DTR)	6	o	o	Connector J2 Pin 9
Data Carrier Detect (DCD)	7	o	o	Connector J2 Pin 8
+12 through 3k ohms	8	o--o		Connector J2 Pin 6

A - 6 Counter Timer Jumper Block (JB5)

This jumper block allows the counter/timer channels to be cascaded for longer sequences. It also provides access to the auxiliary input and output buffers which are connected through JB12 to MEMEX and IOEXP bus signals. The SIO clock is used when the CRT is used as a baud rate generator.

		A	B	
Auxiliary Input	1	o	o	SIO Clock
CTC Channel 0 input	2	o	o	CTC Channel 0 zero detect
CTC Channel 1 Zero detect	3	o	o	CTC Channel 1 input
CTC Channel 2 input	4	o	●	CTC Channel 2 zero detect
Internal Non-Maskable Interrupt	5	o	o	Auxiliary Output
CTC Channel 3 input	6	⊙	o	N/C

A - 7 JB6/7 LED Blocks

These jumpers are installed to drive the LEDs. They should be removed when Channel A is operated in Synchronous mode.

	A B	
TX Driver	o--o	LED Driver U7 (JB6)
RX Driver	o--o	LED Driver U6 (JB7)

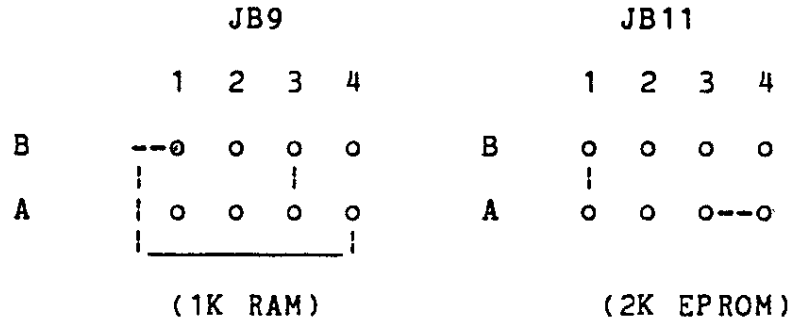
A - 8 Restart Address Jumper Block JB8

Installing the jumper between pins 2 and 3 forces the restart address to E000H. Installing the jumper between pins 1 and 2 forces a restart address to 0000H.

JB8

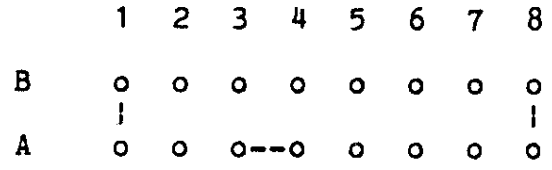
1	o	Force 0000H
2	o |	Restart address control
3	o	Force E000H

A - 9 Memory Socket Configuration Blocks JB9, JB11



A1	Processor address bit 10
B1	Memory socket A10/L
A2	Processor address bit 11
B2	Ground
A3	Memory socket A11/WE/VPP
B3	Processor write line
A4	VCC
B4	N/C

A - 10 Memory Socket Configuration Block & Wait State Generator JB10



(2K EPROM)

A1	Processory Address Bit 10
B1	Memory Socket A10/L
A2	Processor Address Bit 11
B2	Ground
A3	Memory Socket A11/WE/VPP
B3	Processor write line
A4	VCC
B4	N/C
A5,B5	Wait on M1 cycles
A6,B6	Wait on Interrupt Acknowledge cycles
A7,B7	Wait on MREQ cycles
A8,B8	Wait on On-board Memory Cycles

A - 11 CTC/BUS Interface (JB12)

These jumpers are installed to allow counter/timer I/O to be accessed using two lines of the backplane that are not normally used by the Z80 STD bus cards. These signals use the BUS lines normally referred to as MEMEX and IOEXP. This jumper block also contains the Debug function enable jumper.

	A	B	
MEMEX (J1-36)	o	o	CTC Output
Ground	o	o	Ground
CTC Input	o	o	IOEXP (J1-35)
DEBUG (J1-38)	o	--o	debug f/f

A - 12 On Board Memory Options (JB13)

Memory option 1 positions the on-board memory at either 0000H or E000H. Installing the jumper between 1A and 1B positions the memory at 0000H, leaving it out positions the memory at E000H.

Memory options 2 and 3 are not used in the standard version of the DSTD 102. To use the on-board memory disable feature jumper 4A - 4B has to be installed. Port 7B can then be used to control the memory.

		A	B	
Memory Option 1	1	O	O	Ground
Memory Option 2	2	O	O	Ground
Memory Option 3	3	O	O	Ground
DSMEN Latch Input	4	O	--O	DSMEN Option Output

APPENDIX B

STD-Z80 BUS PIN OUT

APPENDIX B

STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	
8	D7	
9	D2	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	
16	A15	
17	A6	Address Bus (Tri-state, output, active high).
18	A14	

19	A5	A0-A15 make up a 16-bit address bus The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least signficant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate than an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

42	/BUSRQ	Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
43	/INTAK	Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
44	/INTRQ	Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
45	/WAITRQ	WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C

DSTD-102 PARTS LIST

APPENDIX C

DSTD-102 PARTS LIST

DY00449-I-11-1

QTY	DESIGNATION	PART NUMBER
1	U5	74LS14
1	U15	74LS08
1	U10	74LS20
2	U3,U14	74LS74
1	U12	74S74
1	U11	74LS112
1	U4	74LS164
1	U27	74LS243
2	U28,U29	74LS244
3	U22,U24,U25	74LS245
1	U13	74LS257A
2	U1,U2	75188
2	U6,U7	75189
1	U17	Z80[A]-CPU/MK3880[-4]
1	U16	Z80[A]-SIO/O/MK3884[-4]
1	U8	Z80[A]-CTC/MK3882[-4]
1	U21	K1135A
1	U26	P12L6-102-1-11
1	U23	P12L6-102-1-21
1	U9	P12L6-102-1-30
	RESISTORS	
1	RN4	109-472G SIP
2	RN2,3	807-472G SIP
2	R1, R7	3k 1/4 watt 5%
2	R2,3	4.7K 1/4 watt 5%
1	R4	1.2k 1/4 watt 5%
1	R5	220 1/4 watt 5%
1	R6	22 1/4 watt 5%
1	R10	47K 1/4 watt 5%
1	R12	100 1/4 watt 5%
1	R13	680 1/4 watt 5%

PARTS LIST

QTY	DESIGNATOR	PART NUMBER
	CAPACITORS	
1	C2	CK05BX330M
8	C6-C13	CK05BX331M
1	C18	TAG10M25
1	C3	DG46B2474M
1	C5	TAG3M25
1	C35	TAG150M25
20	C14-17,C19-34,C36	8121-050-Z51-104M
	DIODES	
2	D1, D2	1N4001
1	LED1	5082-4190
1	LED2	5082-4100
	OSCILLATOR	
1	X1	K1160A 8.00MHz/5.0MHz
	TRANSISTOR	
1	Q1	2N3906
	SOCKETS	
2	U16,U17	640379-1 40 Pin Socket
4	U8,U18,U19,U20	640362-1 28 Pin Socket
3	U9,U23,U26	640464-1 20 Pin Socket
	JUMPER BLOCKS	
2	JB1-JB5,JB9-JB13	CHD6950W1S
1	JB6, 7, 8	CHS6940W1S
2	J2,J3	1-87476-1 12 Pin Connectors

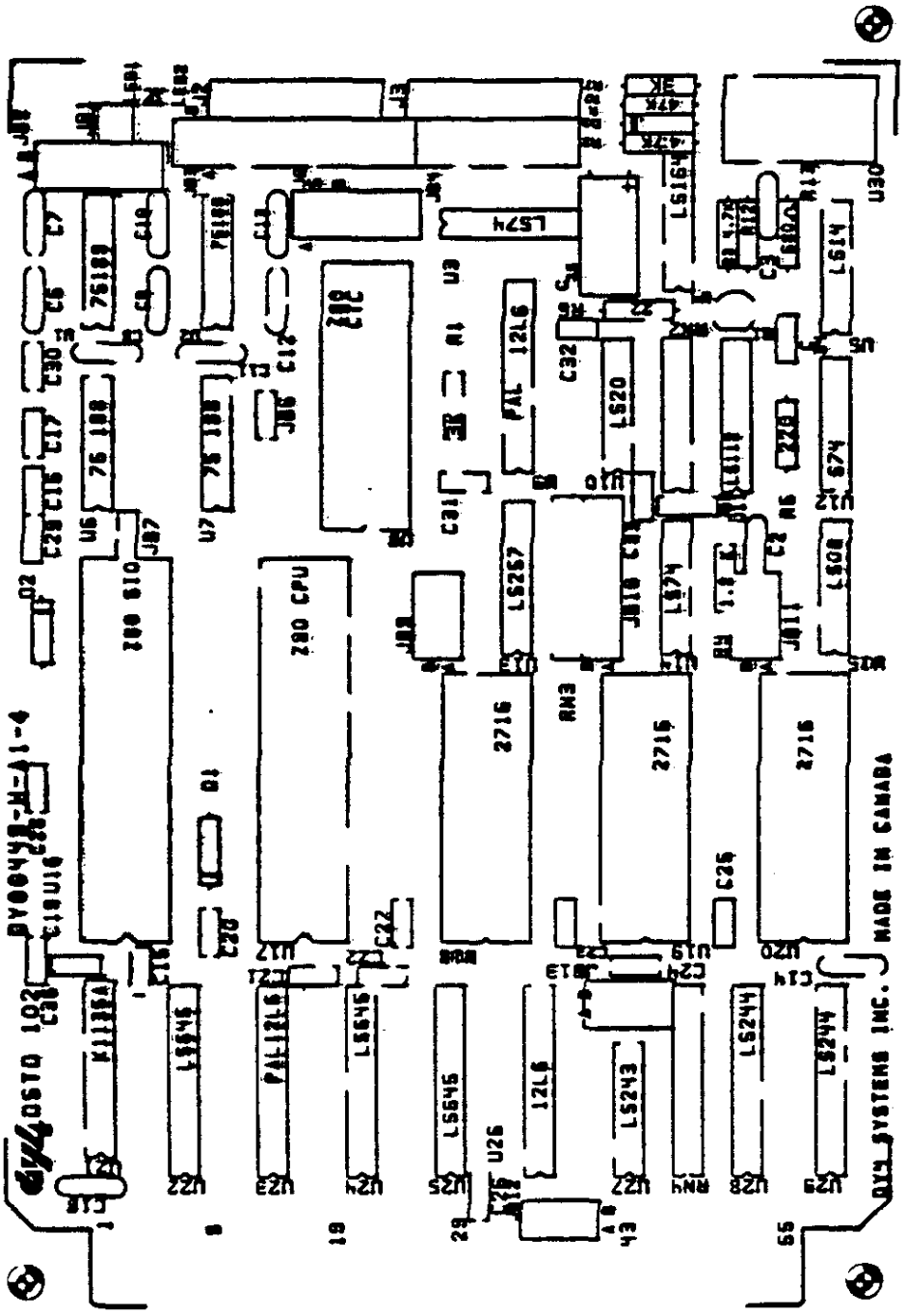


FIGURE C-1 DSTD-102-4 SILK SCREEN