



## ***3 Volt and 5 Volt FlashFile™ Memory***

***28F160S3, 28F320S3, 28F160S5, 28F320S5  
(x8/x16)***

***Specification Update***

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***July 1999***

**Notice:** The 28F160S3, 28F320S3, 28F160S5 and 28F320S5 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 297849-011



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The 28F160S3, 28F320S3, 28F160S5 and 28F320S5 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

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## Revision History

Date of Revision	Version	Description
06/12/97	-001	Document includes all known errata to date (original version)
07/07/97	-002	Added 28F160S5 RP# High Voltage erratum. Added documentation changes for DC characteristics Added documentation changes for ordering codes. Updated A-1 stepping identifier information in this document.
11/06/97	-003	Updated Affected Documents/Related Documents section so that it refers to latest datasheet revision. Corrected documentation error in erratum 2, 28F160S5 RP# High Voltage. Removed documentation changes since these are included in the Rev -002 datasheets.
12/01/97	-004	Added Erratum 3. Erroneous Erase Failure Indicated in Status Register Bit 5 (SR.5).
01/16/98	-005	Added Erratum 4. 28F160S3/S5 Write Buffer Overwrite. Changed name of Erratum 1.
02/04/98	-006	Added Erratum 5. 28F160S5 Status Register Polling During Erase.
04/03/98	-007	Updated fixed status of Errata 2, 3, 4, 5 on 28F160S3/S5 Added Erratum 6. 28F320S3 Write Enable Pulse Width ( $t_{WLWH}$ ) Added Erratum 7. 28F320S3 Address to Output Delay ( $t_{AVQV}$ ) and Chip Enable to Output delay ( $t_{ELQV}$ ) Added Specification Change for 28F320S3/S5 $V_{CC}$ Read Current ( $I_{CCR}$ ) Added Specification Clarification for <i>Word-Wide FlashFile™ Memory Family 28F160S5, 28F320S5</i> datasheet (290609-003), Table 18, <i>Reset AC Specifications</i> , specification P3 Added documentation error in Documentation Changes for <i>Word-Wide FlashFile™ Memory Family 28F160S5, 28F320S5</i> datasheet (290609-003), Figure 11, <i>Set Lock-Bit Flowchart</i> , comments
06/18/98	-008	Added specification change for new 28F160S3/S5 line items with decreased maximum read access time
11/06/98	-009	Added Specification Change for 28F320S3/S5 and 28F160S3/S5 Erase, Write, and Lock-Bit Configuration Performance. Added Erratum 8. 28F320S5 3 V $V_{IH}$ on RP# Updated Erratum 6 and 7 to reflect fixed status. Fixed typographical errors in document relating to steppings and density information. Indicated the erratum 3, 4, and 5 which has been fixed also affected 32-Mbit density.
02/16/99	-010	Previous Specification Clarification and Documentation Changes incorporated into <i>5 Volt FlashFile™ Memory; 28F160S5, 28F320S5 (x8/x16)</i> datasheet). Specification Update renamed form <i>Word-Wide FlashFile™ Memory Family 28F160S3, 28F160S5, 28F320S3, 28F320S5 Specification Update</i> . References to datasheet modified to reflect new datasheet name.
07/02/99	-011	Added certain 28F160S3/S5, 28F320S3/S5 write timing information that was previously listed "TBD." Changed extended temp (–40 °C/+85 °C) to 100K cycles maximum. Changed Pin 29 to NC for 28F320S3/S5 56-Lead SSOP. Changed R1 ( $t_{AVAV}$ ) from 100 to 75 for 16-Mbit 3.3 V $\pm$ 0.3 V.

## Preface

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As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

### Affected Documents/Related Documents

Title	Order
3 Volt FlashFile™ Memory; 28F160S3, 28F320S3 (x8/x16) datasheet	290608-005
5 Volt FlashFile™ Memory; 28F160S5, 28F320S5 (x8/x16) datasheet	290609-004

## Nomenclature

**Errata** are design defects or errors. These may cause the 28F160S3/S5, 28F320S3/S5's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

**Note:** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

# Summary Table of Changes

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The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 28F160S3/S5, 28F320S3/S5 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark)	
or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

### Page

(Page):	Page location of item in this document.
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### Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

### Row



Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.



## Errata

No.	Density						Page	Status	Errata
	16-Mbit Steppings				32-Mbit Steppings				
	A-1	A-2	A-5	A-7	A-2	A-3			
1	X						8	Fixed	28F160S3/S5 Buffer Writes in Byte Mode
2		X					8	Fixed	28F160S5 RP# High Voltage
3	X	X			X		8	Fixed	28F160S5 and 28F320S5 Erroneous Erase Failure Indicated in Status Register Bit 5 (SR.5)
4	X	X			X		8	Fixed	28F160S3/S5 and 28F320S3/S5 Write Buffer Overwrite
5	X	X			X		9	Fixed	28F160S5 and 28F320S5 Status Register Polling during Erase
6					X		9	Fixed	28F320S3 2.7 V Write Enable Pulse Width $t_{WLWH}$
7					X		9	Fixed	28F320S3 2.7 V Address to Output Delay ( $t_{AVQV}$ ) and Chip Enable to Output Delay ( $t_{ELQV}$ )
8						X	9	Fixed	28F320S5 3 V $V_{IH}$ Erratum on RP#

## Specification Changes

No.	Page	Specification Changes
1	10	28F320S3/S5 $V_{CC}$ Read Current ( $I_{CCR}$ )
2	10	28F160S3/S5 Read Access Time
3	11	28F160S3/S5, 28F320S3/S5 Erase, Write, and Lock-Bit Timings
4	14	Extended temp (-40 °C/+85 °C) maximum number of cycles increased to 100K; 10K was erroneous

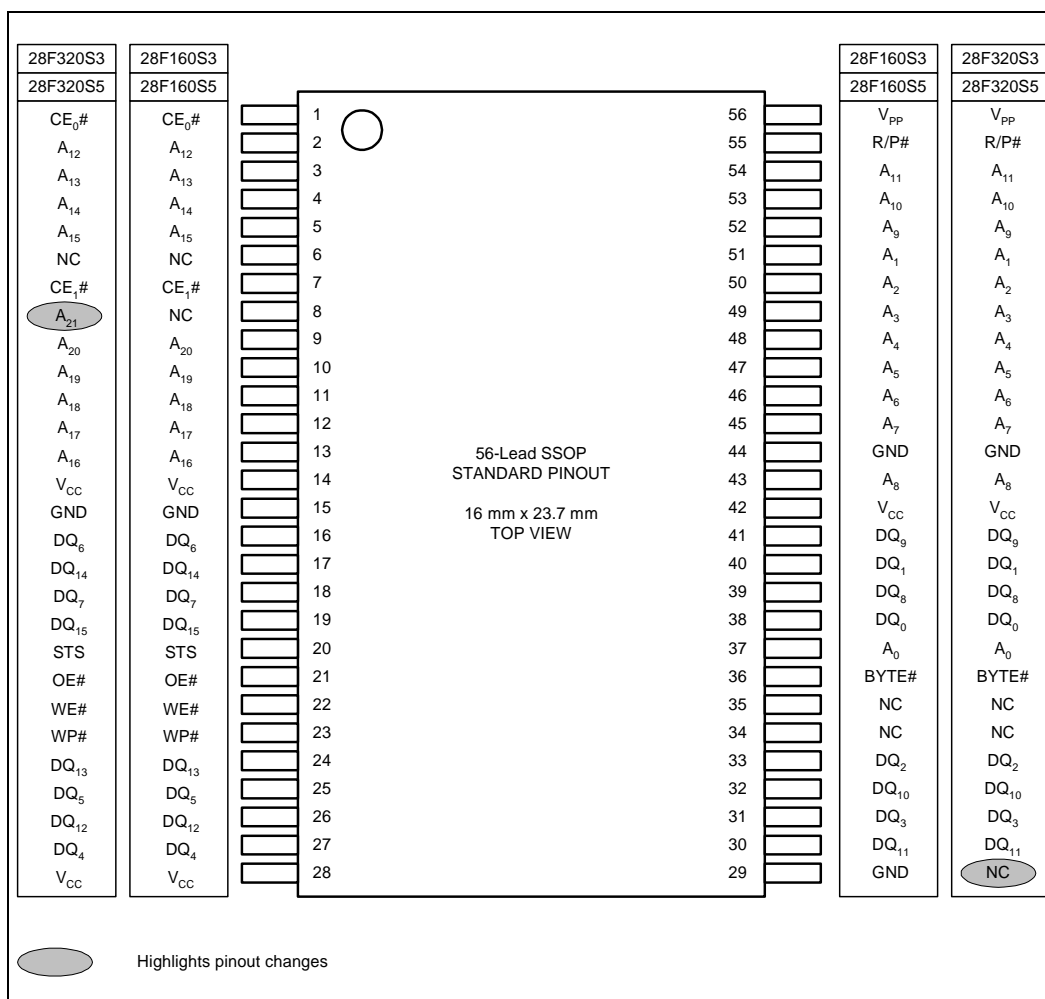
## Specification Clarifications

No.	Page	Specification Clarifications
1	15	R1 t <sub>AVAV</sub> changed to 75 for 16-Mbit devices

## Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
N/A		16		None in this specification update revision

Figure 1. Pin 29 for the 28F320S3/S5 was changed from GND to NC (no connect). NC is defined as: lead is not internally connected; it may be driven or floated.



# Identification Information

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## Markings

The Finished Processing Order (FPO) number correlates to a specific device stepping as illustrated in the table below:

Density	Stepping <sup>(1)</sup>	Identifier
16 Mbit	A-1	Ninth digit on topside FPO mark (third line) = A
16 Mbit	A-2	Ninth digit on topside FPO mark (third line) = C
16 Mbit	A-5	Ninth digit on topside FPO mark (third line) = D
16 Mbit	A-6	Ninth digit on topside FPO mark (third line) = E
16 Mbit	A-7	Ninth digit on topside FPO mark (third line) = F
16 Mbit	A-8	Ninth digit on topside FPO mark (third line) = G
32 Mbit	A-3	Ninth digit on topside FPO mark (third line) = F

**NOTE:** 1. Device steppings are based on continuous updates made in manufacturing and testing of the device and represent the current material shipped.

# Errata

## 1. 28F160S3/S5 Buffer Writes in Byte Mode

**Problem:** With BYTE# low (byte mode), buffer write operations may not function correctly.

**Implication:** Incorrect data may be written into the buffer and subsequently into the flash array.

**Workaround:** Write to buffers with BYTE# high (word mode)

**Status:** This problem has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## 2. 28F160S5 RP# High Voltage

**Problem:** While programming at 5 V  $V_{CC}$ , noise on ground pins, may cause RP#  $V_{IH}$  to deviate from published value. Please replace the existing datasheet specification with the following information.

Sym	Parameter	Notes	Min	Max	Unit	Conditions
$V_{IH}$	Input High Voltage	7	3.3	$V_{CC} + 0.5$	V	

**Implication:** Programming at 5 V  $V_{CC}$  may fail due to noise on GND pins.

**Workaround:** Ensure that  $V_{IH}$  value on RP# is greater than or equal to 3.3 V.

**Status:** This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## 3. 28F160S5 and 28F320S5 Erroneous Erase Failure Indicated in Status Register Bit 5 (SR.5)

**Problem:** During an erase at  $V_{CC}$  and  $V_{PP} = 5 \text{ V} \pm 10\%$ , the Write State Machine (WSM) may indicate that the part did not erase properly, even though the part has successfully erased. This erase error will be indicated by bit 5 of the status register (SR.5) being set.

**Implication:** Applications that use status register bit 5 to verify erase may act as if the erase operation has failed when it has completed successfully.

**Workaround:** If status register bit 5 is set, ignore it and verify that each byte/word contains FFh/FFFFh (all bits in byte/word equal 1).

**Status:** This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## 4. 28F160S3/S5 and 28F320S3/S5 Write Buffer Overwrite

**Problem:** When both the 32-byte write buffers are full, and the first write buffer data has not yet been copied to the flash array, the eXtended Status Register bit XSR.7 may erroneously read 1 indicating that a write buffer is available.

**Implication:** With both write buffers full, a write to buffer operation may succeed – thus overwriting the contents of the second write buffer. However, the contents of the first write buffer will be successfully copied to the flash array.

**Workaround:** Before issuing the third (or subsequent) write to buffer command(s) sequence ensure the Write State Machine (WSM) is ready by reading the status register for SR.7 = 1 and SR.2 = 0. Reading for SR.2 = 0 ensures that the WSM is not in Program Suspend State.

**Status:** This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## 5. 28F160S5 and 28F320S5 Status Register Polling During Erase

**Problem:** During erase operation, polling the status register with multiple Read Status Register commands may result in an erase failure with the status register indicating SR.5 = 1.

**Implication:** If the device fails to erase, it may not program properly.

To monitor erase completion one of the following methods is recommended:

1. While erase is in progress issue the Read Status command only once and toggle OE# or CE<sub>x</sub># to read the status register.
2. While erase is in progress toggle OE# or CE<sub>x</sub># to read the status register.

**Status:** This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## 6. 28F320S3 2.7 V Operation Write Enable Pulse Width $t_{WLWH}$

**Problem:** When operating the 28F320S3 device with  $V_{CC}$  at 2.7 V, the Write Enable Pulse Width  $t_{WLWH}$  needs to be increased from a minimum of 50 ns to 60 ns.

**Implication:** With  $t_{WLWH}$  less than 60 ns, the device may not properly latch data.

**Workaround:** Extend the Write Enable Pulse Width by holding WE# active for one additional write cycle

**Status:** This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## 7. 28F320S3 2.7 V Operation Address to Output Delay ( $t_{AVQV}$ ) and Chip Enable to Output Delay ( $t_{ELQV}$ )

**Problem:** When operating the 28F320S3 device with  $V_{CC}$  at 2.7 V, the Address Valid to Output Delay ( $t_{AVQV}$ ) and Chip Enable to Output delay ( $t_{ELQV}$ ) needs to be increased from 130 ns to 160 ns.

**Implication:** The device may not output valid data until 160 ns after either a valid address on the inputs, or a valid Chip Enable logic low ( $V_{IL}$ ).

**Workaround:** Extend the read cycle time from 130 ns to 160 ns. Do not attempt to latch valid data until 160 ns after either a valid address on the inputs, or a valid Chip Enable (CE<sub>0</sub>#,CE<sub>1</sub>#) logic low ( $V_{IL}$ ).

**Workaround:** This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## 8. 28F320S5 3 V $V_{IH}$ Erratum on RP#

**Problem:** With  $V_{CC}$  and  $V_{PP}$  5 V mode below 0 °C, program, erase and block locking failures may occur if  $V_{IH}$  on RP# control input is lower than 3.0 V.

**Implication:** Status register might report the operation as finished without writing data into the array or erasing array, and the part might be read array mode after the operation.

**Workaround:** In 5 V  $V_{CC}$  and  $V_{PP}$  mode, when input control signal pin RP# is supplied  $V_{IH}$ , ensure that  $V_{IH}$  (min) level is higher than 3 V. For CPUs that specify minimum  $V_{OH}$  level of less than 3.0 V, a pull-up resistor should be tied between  $V_{CC}$  and RP# to ensure  $V_{IH}$  of > 3.0 V. The value of the resistor is determined, in part, by the current sink capability of the CPU when driving the RP# control input to  $V_{IL}$  as follows:  $V_{load}/R_{load} = I_{load}$

For example, with a 10 K $\Omega$  resistor, at  $V_{CC}$  Max (5.5 V), and  $V_{IL}$  at 0 V (worst case minimum), the voltage dropped across the 10K resistor is 5.5 V. The current will be  $5.5/10K = 550 \mu A$ . This work around will ensure proper  $V_{IL}$  logic levels, provided the CPU can sink the required current.

**Status:** This erratum has been fixed. Refer to the *Summary Tables of Changes* to determine the affected products and stepping(s).

## Specification Changes

### 1. 28F320S3/S5 $V_{CC}$ Read Current ( $I_{CCR}$ )

**Issue:** The  $V_{CC}$  read current ( $I_{CCR}$ ) for the 28F320S3/S5 devices is increased as follows:

#### 28F320S3

Sym	Parameter	Old	New	Max	Unit	Conditions
$I_{CCR}$	$V_{CC}$ Read Current	25	30		mA	CMOS
$I_{CCR}$	$V_{CC}$ Read Current	30	35		mA	TTL

#### 28F320S5

Sym	Parameter	Old	New	Max	Unit	Conditions
$I_{CCR}$	$V_{CC}$ Read Current	50	60		mA	CMOS
$I_{CCR}$	$V_{CC}$ Read Current	65	75		mA	TTL

### 2. 28F160S3/S5 Read Access Time

**Issue:** New line items and/or capabilities for the 28F160S3/S5 have been added. The new maximum read cycle times and line items are highlighted below:

Order Code by Density		Valid Operation Combinations	
16 Mb	32 Mb	$t_{AVAV}/t_{AVQV}$ 2.7 V–3.6 V $V_{CC}$ 50 pF load (16 Mb / 32 Mb)	$t_{AVAV}/t_{AVQV}$ 3.3 V $\pm$ 0.3 V $V_{CC}$ 50 pF load (16 Mb / 32 Mb)
<b>TE28F160S3-75</b>		<b>-100</b>	<b>-75</b>
TE28F160S3-100		-120	-100
TE28F160S3-130		-150	-130
<b>DT28F160S3-75</b>		<b>-100</b>	<b>-75</b>
DT28F160S3-100	DT28F320S3-110	-120 / -130	-100 / -110
DT28F160S3-130	DT28F320S3-140	-150 / -160	-130 / -140

Order Code by Density		Valid Operations			
16 Mb	32 Mb	$t_{AVAV}/t_{AVQV}$ 5 V 10% $V_{CC}$ 100 pF load (16 Mb/32 Mb)	$t_{AVAV}/t_{AVQV}$ 5 V 5% $V_{CC}$ 30 pF load (16 Mb/32 Mb)	$t_{AVAV}/t_{AVQV}$ 5 V 10% $V_{CC}$ 50 pF load (16 Mb <sup>1</sup> ) 0 °C – 70°C Only	$t_{AVAV}/t_{AVQV}$ 5 V 5% $V_{CC}$ 30 pF load (16 Mb <sup>1</sup> ) 0 °C – 70°C Only
TE28F160S5-70		-75	-70	-70	-65
TE28F160S5-100		-100			
DT28F160S5-70	DT28F320S5-90	-75 / -100	-70 / -90	-70	-65
DT28F160S5-100	DT28F320S5-120	-100 / -120			

**NOTE:** 1. These improvements match fastest 28F016SV-75 for easier migrations to 28F160S5-70.

### 3. **28F160S3/S5, 28F320S3/S5 Erase, Write, and Lock-Bit**

New timings for the 28F160S3/S5, 28F320S3/S5 have been added. The new erase, write, and lock-bit timings are shaded in the following tables:

**Erase, Write, and Lock-Bit Configuration Performance for the 28F160S3 and 28F320S3, 2.7 V–3.6 V V<sub>CC</sub>**<sup>(3,4)</sup>

Version				2.7 V–3.6 V V <sub>CC</sub>						Unit
				2.7 V V <sub>PP</sub>		3.3 V V <sub>PP</sub>		5 V V <sub>PP</sub>		
#	Sym	Parameter	Note	Typ <sup>(1)</sup>	Max <sup>(6)</sup>	Typ <sup>(1)</sup>	Max <sup>(6)</sup>	Typ <sup>(1)</sup>	Max <sup>(6)</sup>	
W16		Byte/Word Program Time (using write buffer)	5	5.76	250	5.76	250	2.76	180	μs
W16	t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Per Byte Program Time (without write buffer)	2	18.0	160	17.0	150	12.0	100	μs
W16	t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Per Word Program Time (without write buffer)	2	20.0	190	19.0	180	12.0	100	μs
W16		Block Program Time (byte mode)	2	1.2	2.0	1.1	1.7	0.87	1.2	sec
W16		Block Program Time (word mode)	2	0.7	1.1	0.6	1.0	0.44	0.6	sec
W16		Block Program Time (using write buffer)	2	0.37	4.1	0.37	4.1	0.16	2	sec
W16	t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Erase Time	2	0.56	6.0	0.35	4.0	0.3	3.5	sec
W16		Full Chip Erase Time	16 Mbit	17.9	192	12.0	128	9.6	112	sec
			32 Mbit	35.8	384	24.0	256	19.2	224	sec
W16	t <sub>WHQV3</sub> t <sub>EHQV3</sub>	Set Lock-Bit Time	2	20.0	190	19.0	180	12.0	100	μs
W16	t <sub>WHQV4</sub> t <sub>EHQV4</sub>	Clear Block Lock-Bits Time	2	0.56	6.0	0.35	4.0	0.3	3.5	sec
W16	t <sub>WHRH1</sub> t <sub>EHRH1</sub>	Program Suspend Latency Time to Read		7.24	10.2	7.24	10.2	6.73	9.48	μs
W16	t <sub>WHRH2</sub> t <sub>EHRH2</sub>	Erase Suspend Latency Time to Read		15.5	21.5	15.5	21.5	12.54	17.54	μs

**NOTES:**

1. Typical values measured at T<sub>A</sub> = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. Uses whole buffer.
6. Maximum values represent less than 1% of units exposed to greater than 100K cycles.



**Erase, Write, and Lock-Bit Configuration Performance for the 28F160S3 and 28F320S3, 3.3 V–0.3 V  $V_{CC}$  <sup>(3,4)</sup>**

Version				3.3 V $\pm$ 0.3 V $V_{CC}$				Units
				3.3 V $V_{PP}$		5 V $V_{PP}$		
#	Sym	Parameter	Note	Typ <sup>(1)</sup>	Max <sup>(6)</sup>	Typ <sup>(1)</sup>	Max <sup>(6)</sup>	
W16		Byte/Word Program Time (using write buffer)	5	5.66	250	2.7	180	$\mu$ s
W16	$t_{WHQV1}$ $t_{EHQV1}$	Per Byte Program Time (without write buffer)	2	19.51	250	12.95	180	$\mu$ s
W16	$t_{WHQV1}$ $t_{EHQV1}$	Per Word Program Time (without write buffer)	2	21.75	250	12.95	180	$\mu$ s
W16		Block Program Time (byte mode)	2	1.6	16.5	0.85	10.9	sec
W16		Block Program Time (word mode)	2	0.89	8.2	0.43	4.8	sec
W16		Block Program Time (using write buffer)	2	0.36	4.1	0.18	2	sec
W16	$t_{WHQV2}$ $t_{EHQV2}$	Block Erase Time	2	0.55	10	0.41	10	sec
W16		Full Chip Erase Time	16 Mbit	17.6	320	13.1	320	sec
			32 Mbit	35.2	640	26.2	640	sec
W16	$t_{WHQV3}$ $t_{EHQV3}$	Set Lock-Bit Time	2	22.75	250	12.95	180	$\mu$ s
W16	$t_{WHQV4}$ $t_{EHQV4}$	Clear Block Lock-bits Time	2	0.55	10	0.41	10	sec
W16	$t_{WHRH1}$ $t_{EHRH1}$	Program Suspend Latency Time to Read		7.1	10	6.6	9.3	$\mu$ s
W16	$t_{WHRH2}$ $t_{EHRH2}$	Erase Suspend Latency Time to Read		15.2	21.1	12.3	17.2	$\mu$ s

**NOTES:**

1. Typical values measured at  $T_A = +25^\circ\text{C}$  and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. Uses whole buffer.
6. Maximum values represent less than 1% of units exposed to greater than 100K cycles.

**Erase, Write, and Lock-Bit Configuration Performance for the 28F160S3 and 28F320S3, 5 V  $\pm$  5%, 5 V  $\pm$  10% V<sub>CC</sub> <sup>(3,4)</sup>**

Version			Notes	5 V $\pm$ 5%, 5 V $\pm$ 10% V <sub>CC</sub>		Units
				5 V V <sub>PP</sub>		
#	Sym	Parameter		Typ <sup>(1)</sup>	Max <sup>(6)</sup>	
W16		Byte/Word Program Time (using write buffer)	5	2	120	$\mu$ s
W16	t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Per Byte Program Time (without write buffer)	2	9.24	90.0	$\mu$ s
W16	t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Per Word Program Time (without write buffer)	2	9.24	90.0	$\mu$ s
W16		Block Program Time (byte mode)	2	0.5	1.0	sec
W16		Block Program Time (word mode)	2	0.38	0.5	sec
W16		Block Program Time (using write buffer)	2	0.13	1.5	sec
W16	t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Erase Time	2	0.34	3.5	sec
W16		Full Chip Erase Time	16 Mbit	10.7	112	sec
			32 Mbit	21.4	224	sec
W16	t <sub>WHQV3</sub> t <sub>EHQV3</sub>	Set Lock-Bit Time	2	9.24	90.0	$\mu$ s
W16	t <sub>WHQV4</sub> t <sub>EHQV4</sub>	Clear Block Lock-bits Time	2	0.34	3.5	sec
W16	t <sub>WHRH1</sub> t <sub>EHRH1</sub>	Program Suspend Latency Time To Read		5.6	7	$\mu$ s
W16	t <sub>WHRH2</sub> t <sub>EHRH2</sub>	Erase Suspend Latency Time To Read		9.4	13.1	$\mu$ s

**NOTES:**

1. Typical values measured at T<sub>A</sub> = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. Uses whole buffer.
6. Maximum values represent less than 1% of units exposed to greater than 100K cycles.

#### 4. Extended Temperature (–40 °C/+85 °C) Maximum Number of Cycles Increased to 100K

**Issue:** Extended temperature (–40 °C/+85 °C) maximum number of cycles increased to 100K.

# Specification Clarifications

## 1. R1 $t_{AVAV}$ Changed to 75 for 16-Mbit Devices

**Issue:** Changed R1  $t_{AVAV}$  from 100 to 75 for 16-Mbit 3.3 V  $\pm$  0.3 V; highlighted in table below.

### 6.5 AC Characteristics—Read-Only Operations<sup>(1, 5)</sup>

$T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  (Extended) and  $T_A = 0\text{ }^\circ\text{C}$  to  $+70\text{ }^\circ\text{C}$  (Commercial)

Versions (All Units in ns Unless Otherwise Noted)		3.3V $\pm$ 0.3V $V_{CC}$		16Mb/32Mb -75/-110				16Mb/32Mb -130/-140				
		2.7V - 3.6V $V_{CC}$				16Mb/32Mb -100/-130				16Mb/32Mb -150/-160		
#	Sym	Parameter	Note	Min	Max	Min	Max	Min	Max	Min	Max	
R1	$t_{AVAV}$	Read/Write Cycle Time	16 Mbit	1	75		100		130		150	
			32 Mbit	1	110		130		140		160	
R2	$t_{AVQV}$	Address to Output Delay	16 Mbit	1		75		100		130		150
			32 Mbit	1		110		130		140		160
R3	$t_{ELQV}$	$CE_x\#$ to Output Delay	16 Mbit	2		75		100		130		150
			32 Mbit	2		110		130		140		160
R4	$t_{GLQV}$	OE# to Output Delay	2		45		50		50		55	
R5	$t_{PHQV}$	RP# High to Output Delay			600		600		600		600	
R6	$t_{ELQX}$	$CE_x\#$ to Output in Low Z	3	0		0		0		0		
R7	$t_{GLQX}$	OE# to Output in Low Z	3	0		0		0		0		
R8	$t_{EHQZ}$	$CE_x\#$ High to Output in High Z	3		50		50		55		55	
R9	$t_{GHQZ}$	OE# High to Output in High Z	3		20		20		25		25	
R10	$t_{OH}$	Output Hold from Address, $CE_x\#$ , or OE# Change, Whichever Occurs First	3	0		0		0		0		
R11	$t_{ELFL}$ $t_{ELFH}$	$CE_x\#$ Low to BYTE# High or Low	3		5		5		5		5	
R12	$t_{FLQV}$ $t_{FHQV}$	BYTE# to Output Delay	16 Mbit	3		100		120		130		150
			32 Mbit	3		110		130		140		160
R13	$t_{FLQZ}$	BYTE# to Output in High Z	3		30		30		40		40	

**NOTES:**

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to  $t_{ELQV} - t_{GLQV}$  after the falling edge of  $CE_x\#$  without impact on  $t_{ELQV}$ .
3. Sampled, not 100% tested.
4. See *Ordering Information* for device speeds (valid operational combinations).
5. See Figures 14 through 16 for testing characteristics.

# ***Documentation Changes***

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There are no Documentation Changes in this Specification Update.