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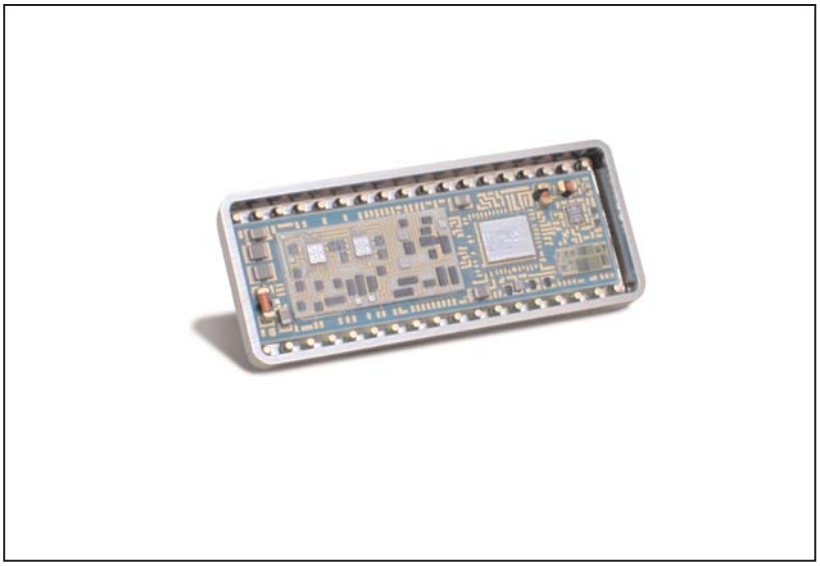
# DTC-19300
# LVDT/RVDT-TO-DIGITAL CONVERTER



## FEATURES

- Internal Oscillator: Programmable for Voltage and Frequency
- Programmable Signal Gain
- Programmable for 12- or14-Bit Resolution
- Velocity Output
- Built-In-Test Output
- Three-State, Two-Byte Digital Output

## DESCRIPTION

The DTC-19300 is a 12- or 14-bit LVDT (Linear Variable Differential Transformer)- or RVDT (Rotary Variable Differential Transformer)-to- digital converter which also supplies the AC excitation to drive the LVDT. Internal AC excitation voltage, frequency, signal gain and resolution are all programmable for optimum system performance. Packaged in a 36-pin hybrid, the DTC-19300 also features Velocity (VEL) and Built-In-Test ($\overline{\text{BIT}}$) outputs. The three-state digital outputs are provided in a two byte format, for easy computer interface.

The DTC-19300 has been designed precisely for use with an LVDT. Inherent characteristics of the DTC-19300, such as the input to output phase shift, have been given considerable attention. The converter's reference voltage is derived from, and is in phase with, the LVDT output signal. Therefore, any errors due to the transducer's phase shift are virtually eliminated. Additionally, the programmability of the DTC-19300 will accomodate a broad range of LVDT's.

## APPLICATIONS

The DTC-19300 provides many features previously supplied by individual system components. Because of its internal AC source, programmable features, fault indicator ($\overline{\text{BIT}}$), and velocity output (VEL), the need for other system circuits is minimized. The DTC-19300 is an excellent choice for applications using the LVDT transducer for position feedback, such as military, commercial aerospace and industrial control systems.



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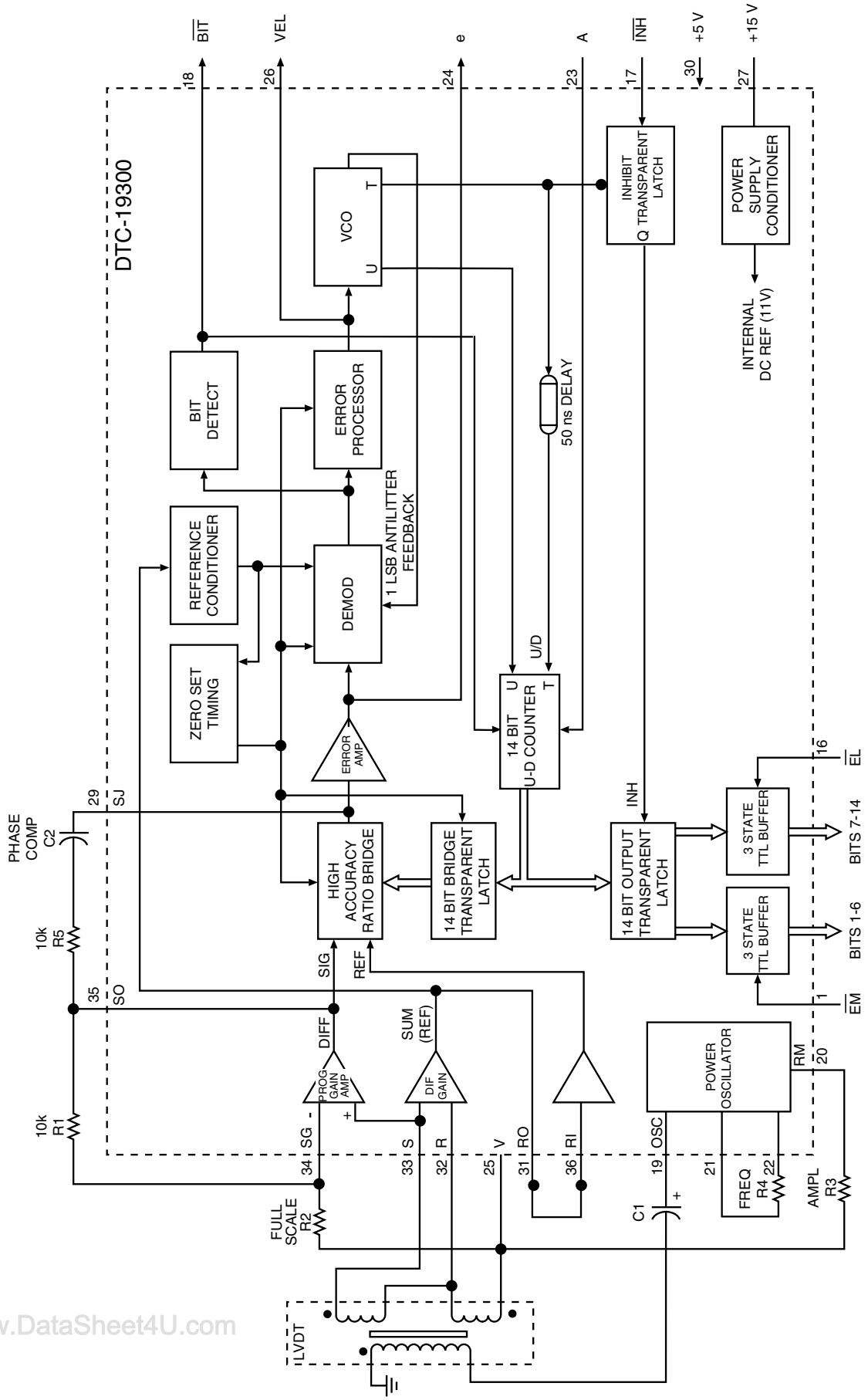



**FIGURE 1. DTC-19300 BLOCK DIAGRAM**

**TABLE 1. DTC-19300 SPECIFICATIONS**
Specifications apply over temperature and power supply ranges

| PARAMETER | VALUE | DESCRIPTION |
|---|---|---|
| **RESOLUTION** | 12 or 14 bits | Programmable |
| **ACCURACY** | 0.25, 0.05% of Reading | See Ordering Information. |
| **REPEATABILITY** | 1 LSB max | |
| **DIFFERENTIAL LINEARITY** | 1 LSB max | |
| **FREQUENCY OUT**<br>(OSC Pin 18)<br>Frequency<br>Voltage<br><br>Current Drive<br>Protection | <br>5 kHz ± 10%<br>2.7 Vrms ± 20%<br><br><br>20 mA rms min | Tunable down to 400 Hz; disable with R4 = oo (See Setting Up and Programming). 20% @ room temp, add 20% @ overtemp. Scalable down (See Setting Up and Programming).<br><br>Short circuit, overcurrent, and voltage transient protected. |
| **REFERENCE IN (RI)**<br>Full Scale Voltage<br>Input Impedance | <br>2 Vrms ± 10%<br>20 MOhms min | Transient protected voltage follower. |
| **REFERENCE IN (R)**<br>Voltage<br>Input Impedance | <br>1 Vrms ± 10%<br>20 MOhms min | Transient protected voltage follower. |
| **SIGNAL IN (S)**<br>Full Scale Voltage<br>Input Impedance | <br>2 Vrms<br>20 MOhms min | Transient protected voltage follower. |
| **DIGITAL INPUTS / OUTPUTS**<br>Logic Type<br>Inputs<br><br>Loading<br>INH (Inhibit)<br><br>$\overline{EM}$ (Enable Bits 1-6)<br>EL (Enable Bits 7-14)<br><br>A (Resolution Control) | <br><br>Logic 0 = 0.8 V max<br>Logic 1 = 2.0 V min<br>10 µA max | TTL/CMOS compatible<br><br>Pull up current source to +5V//5 pF, CMOS transient protection.<br><br>Logic 0 inhibits, data valid within 0.5 µs.<br>Logic 1 enables.<br>Logic 0 enables, data valid within 150 ns.<br>Logic 1 = high impedance, data high Z within 100 ns.<br><br>Logic 1 = 14-bit resolution.<br>Logic 0 = 12-bit resolution. |
| **OUTPUTS**<br>Parallel Data<br><br>$\overline{BIT}$ (Built-In-Test)<br>Drive Capability | <br>12 or 14 bits<br><br>Logic 0 = 1 TTL load<br>Logic 1 = 10 TTL loads<br>High Z = 10 µA//5 pF max | Bi-Polar two's compliment.<br>Bit 1 = MSB; Bit 14 or Bit 12 = LSB.<br>Logic 0 for BIT condition (converter malfunction).<br>1.6 mA @ 0.4V max +50 pF.<br>-0.4V mA at 2.8 V min +50 pF.<br>When in the third state. |
| **ANALOG OUTPUTS**<br>V (Analog Ground)<br>VEL (Velocity)<br>Scaling<br>Scaling TC<br>Reversal Error<br>Linearity<br>Zero Offset<br>Noise and Ripple<br>AC peak/DC Average<br>Load | 5.5 VDC nom<br><br>+4V ± 15%<br>200 PPM / °C max<br>2 % max<br>2 % of output max<br>10 mV max<br>50 mV rms<br>0.5 % max<br>40 kOhms min | VEL is with respect to V.<br>1 (14-bit) or 4 (12-bit) ranges per second. |

| TABLE 1. DTC-19300 SPECIFICATIONS (CONT.)<br>Specifications apply over temperature and power supply ranges | | |
|---|---|---|
| **PARAMETER** | **VALUE** | **DESCRIPTION** |
| **DYNAMIC CHARACTERISTICS**<br>Tracking Rate<br>Bandwidth, Closed Loop<br>Ka<br>A1<br>A2<br>A<br>B<br>Acc for 1 LSB lag<br>Setting Time - half scale step | <br>1 full range per sec, min<br>18 Hz<br>1600 1/sec2<br>0.4 1/sec<br>4000 1/sec<br>40 1/sec<br>20 1/sec<br>0.1 full ranges per sec2<br>150ms | |
| **POWER SUPPLIES**<br>**+5V SUPPLY**<br>Nominal Voltage and Range<br>Max Voltage w/o Damage<br>Current, Peak<br>Current, Average<br>**+15V SUPPLY**<br>Nominal Voltage and Range<br>Max Voltage w/o Damage<br>Current Peak<br>Current, Average | <br>+5 VDC ± 10%<br>+8 VDC<br>10 mA max<br>10 mA max<br><br>+15 VDC ±5%<br>+18 VDC<br>25 mA max, $+\sqrt{2}$ x $I_{osc}$ rms.<br>35 mA max, + 0.9 x 0.5 x $I_{osc}$ rms | |
| **TEMPERATURE RANGES**<br>Operating, Ambient<br>-3XX<br>-1XX<br>Storage | <br>0°C to +70°C<br>-55°C to +125°C<br>-65°C to +150°C | |
| **PHYSICAL CHARACTERISTICS**<br>Size<br><br>Weight | <br>0.78 x 1.9 x 0.21 inches<br>(20 x 48 x 5.3 mm)<br>1 oz<br>(28 gm) | <br>36-pin DDIP |

## INTRODUCTION

The circuit shown in FIGURE 1 (DTC-19300 Block Diagram) consists of four main parts:

1. Signal input conditioner

2. Feedback loop (whose elements include a high accuracy ratio bridge, a demodulator, an error processor, a VCO and an up-down counter)

3. Power oscillator to excite the LVDT

4. Digital interface circuit (including various latches and buffers)

In the LVDT, position output is transmitted as a differential voltage that varies linearly with changes in the core position. The DTC-19300 receives the differential and sum voltage at its inputs and internally produces a digital position $\delta$ which tracks the differential position $\lambda$ to within the specified accuracy of the converter.

A high accuracy ratio bridge is used to compute ($\lambda$ - $\delta$), where:

$\lambda$ = the LVDT's core position.

$\delta$ = the digital position contained in the converter's up-down counter.



The tracking process consists of continually adjusting $\delta$ to make ($\lambda$ - $\delta$) → 0, so that $\delta$ will represent the core's position, $\lambda$.

The ratio bridge output is fed to a demodulator whose output is an analog DC level proportional to ($\lambda$ - $\delta$). The error processor receives its input from the demodulator and integrates the error signal ($\lambda$ - $\delta$) which then drives a Voltage-Controlled Oscillator (VCO).

Functionally, the up-down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a type II tracking servo. In a type II servo the VCO always settles to the counting rate which makes the $d\delta/dt$ equal to $d\lambda/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

## POWER OSCILLATOR

The DTC-19300 contains an internal power oscillator. The OSC output (pin 19) can be programmed for voltage and frequency. The default output voltage is 2.7 Vrms, scalable down with an external resistor R3 connected between RM (pin 20) and V (pin 25). The default frequency is 5 kHz, tunable to 400 Hz with an external resistor R4 connected between RF1 (pin 21) and RF2 (pin 22). If desired, an external oscillator can be used in place of the internal oscillator.

## SOLID STATE BUFFERED INPUTS

The signal and reference inputs are voltage follower inputs with high impedance that do not load the LVDT. The maximum transient peak voltage should not exceed 100 V.

## DIGITAL INTERFACE

The digital interface circuitry has three main functions:

1. Latch the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the DTC-19300

2. Furnish parallel tri-state data formats

3. Act as a buffer between the internal CMOS logic and the external TTL logic

In the DTC-19300, applying an INHIBIT ($\overline{INH}$) command will lock the data in the Output Transparent Latch without interfering with the continuous tracking of the feedback loop. Therefore, the digital position always updates, and the INHIBIT can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50 ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 17) paragraph.

## LOGIC OUTPUT

Logic outputs from the DTC-19300 consist of the LVDT core's digital position in 12 or 14 parallel data bits. All logic outputs are short-circuit proof to ground and +5 V. The internal Timing signal (T) is a positive, 0.4 to 0.7 µs pulse. Data changes approximately 50 ns after the leading edge of T, and the position is determined by the sum of the bits at logic 1. Digital outputs are three-state and are provided in two bytes: bits 1 through 6 (MSBs) which are enabled by the signal EM, and bits 7 through 14 (LSBs) which are enabled by the signal EL. Outputs are valid (logic 1 or 0) 150 ns maximum after setting EM or EL low, and are high impedance within 100 ns maximum of setting EM or EL high. Both EM and EL are internally pulled-up to +5 V at 100 nA maximum .

## INHIBIT ($\overline{INH}$, PIN 17)

The $\overline{INH}$ input locks the Output Transparent Latch (See FIGURE 1) so the bits will remain stable while data is being transferred. The output is stable 0.5 µs after $\overline{INH}$ is driven to logic 0.



A logic 0 applied to the T input latches data, and a logic 1 applied to T allows the bits to change. The Inhibit Transparent Latch prevents the transmission of invalid data when there is an overlap between T (VCO clock to up-down counter) and $\overline{INH}$. While the counter is not being updated, T is at a logic 0 and the Inhibit Latch is transparent. When T goes to a logic 1, the Inhibit Latch is locked. If T occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until T returns to logic 0; if $\overline{INH}$ is applied during T, the latch will not lock until the T pulse is a logic 0. The purpose of the 50 ns delay is to prevent a race condition between T and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied.

FIGURE 2 illustrates the Inhibit Timing. Whenever an input position change occurs, the converter changes the digital position in 1 LSB steps and generates a T pulse, delayed by 50 ns, nominal. Valid data is available at the outputs 0.2 µs after the leading edge of T. An $\overline{INH}$ input, regardless of its duration, does not affect the converter update.

A simple method of interfacing to a computer is:

1. apply $\overline{INH}$

2. wait 0.5 µs minimum

3. transfer data and release $\overline{INH}$

As long as the converter's maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as when power is initially applied, the response will be critically damped. FIGURE 3 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (inherent in a type II servo). The overshoot settling to final value is a function of the small signal settling to final value.

## BUILT-IN-TEST ($\overline{BIT}$, PIN 18)

The $\overline{BIT}$ output monitors the level of the demodulator (D). If D exceeds approximately 65 bits, the logic level at $\overline{BIT}$ will change from logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also be set for an over-velocity condition because the converter loop cannot maintain input-output sync, or if the converter malfunctions where it cannot maintain the loop at a null.

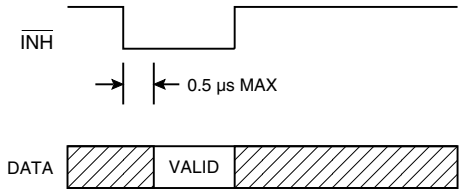



**FIGURE 2. INHIBIT TIMING**

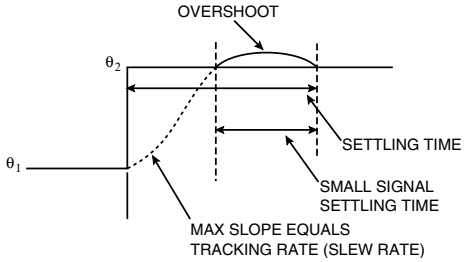



**FIGURE 3. RESPONSE TO A STEP INPUT**

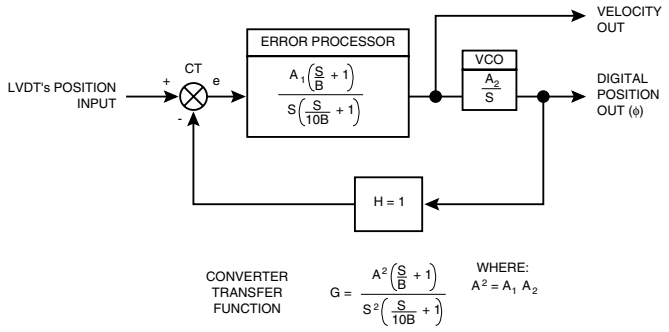



**FIGURE 4.CONTROL LOOP BLOCK DIAGRAM**

## VELOCITY (VEL, PIN 26)

The Velocity output (VEL) from the DTC-19300 is a DC voltage proportional to the angular velocity (dl/dt = dd/dt). The velocity is input to the second integrator, as shown in FIGURE 4. Its linearity is dependent solely on the linearity of the voltage controlled oscillator (VCO). An open loop Bode plot is shown in FIGURE 5. Bandwidth (BW) and the acceleration constant (Ka) can be determined by the following formula:

$$\text{Closed Loop Bandwidth (Hz)} = \frac{\sqrt{2 \times A}}{\pi}$$

Output VEL is not required for normal operation of the converter; V is used as an internal DC reference. Maximum loading on V and VEL is 40k.

The simple filter shown in FIGURE 6 will eliminate the one overshoot for a step velocity input and filter the carrier frequency ripple from the velocity output.



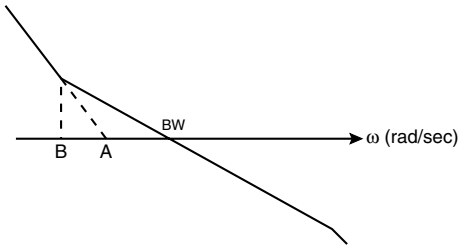



**FIGURE 5. OPEN LOOP BODE PLOT**

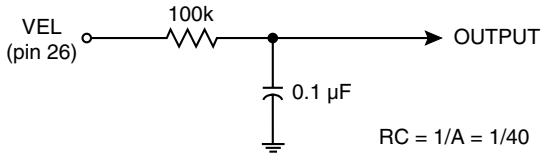



**FIGURE 6. VELOCITY FILTER**

## ELECTRONIC LIMIT STOPS

The DTC-19300 incorporates electronic limit stops and will not count up past +FS-1 LSB or down past -FS. Once + Full scale is reached, over-ranging the converter further generates error in the feedback loop. If this error reaches ~ 65 LSB's of the selected resolution , the BIT signal will come on. The Bit is tied to an internal resolution input which will lower the resolution by 4 bits. Therefore when an over-range of about ~ 65 LSB's of error is reached, the 4 LSB's will turn off.

## OUTPUT CODING

TABLE 2 lists the digital output codes of the DTC-19300 for various positions of the LVDT, including full scale (FS) and half scale (HS). Table 3 lists the weight of each bit with respect to the full scale output.

**TABLE 2. DIGITAL OUTPUT CODES**

| SCALE | (MSB) | | | | | | DIGITAL OUTPUT | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| +FS - 1 LSB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| +HS | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| +1 LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| ZERO | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -1 LSB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| -HS | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -FS | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## SETTING UP AND PROGRAMMING THE DTC-19300

To set up and operate the DTC-19300, refer to FIGURE 7 and proceed as follows:

### *INTERNAL OSCILLATOR*

1. Select the LVDT's operating frequency.

2. Calculate the value of R4 (the oscillator frequency setting resistor) by using the LVDT frequency in the equation below.

$$R4\ (\text{in Ohms}) = \frac{1.14 \times 10^{12}}{(\text{Frequency in Hz})^2} - 45.6k$$

3. Calculate the value of R3 (the oscillator amplitude setting resistor), to result in 0.8 Vrms between pin 32 (R) and pin 25 (V), when the LVDT is at its null position (core in the center). This usually requires a 0.8 Vrms input to the LVDT primary. Proceed as follows:

a. Use the LVDT turns ratio (usually 1:1) to calculate the oscillator output with the following equation:

$$Vosc = 0.8 \text{ volts} \times \text{turns ratio}$$

b. Calculate the value of R3 with the equation below:

$$R3 = \frac{Vosc \times 100k}{2.7 - Vosc}$$

c. Calculate the value of the coupling capacitor C1 so that its impedance will be less than 1/10 the impedance of the LVDT at the operating frequency.

### *CONVERTER FULL SCALE*

4. Calculate the value of R2 (full-scale setting resistor) with the LVDT at full travel. This results in 1.6 Vrms between pin 35 (SO) and pin 25 (V). Use the following equation:

$$R2 = \frac{10k \times \text{pin 33 (S) voltage}}{1.6 - \text{pin 33 (S) voltage}}$$

### *PHASE COMPENSATION*

5. At full travel, monitor pin 24 (e) voltage with an oscilloscope and determine the value for C2 that gives minimum output. This value (of C2) can be used for all applications which use the same LVDT.

### *CONVERTER RESOLUTION*

6. Select 12-bit or 14-bit operating mode. The 12-bit mode provides faster response to input variations and is set by grounding pin 23 (A). The 14-bit mode provides higher resolution and is set by connecting pin 18 ($\overline{\text{BIT}}$ output) to pin 23 (A).

In both modes, if the $\overline{\text{BIT}}$ line goes low indicating an error condition (the error signal to error processor and VCO is too large), the DTC-19300 is set to 12-bit mode so that the error can be driven to null faster. Once this happens, the converter returns to the original setting.



Note: Consult factory for information concerning the use of the converter with the 2-wire LVDTs.

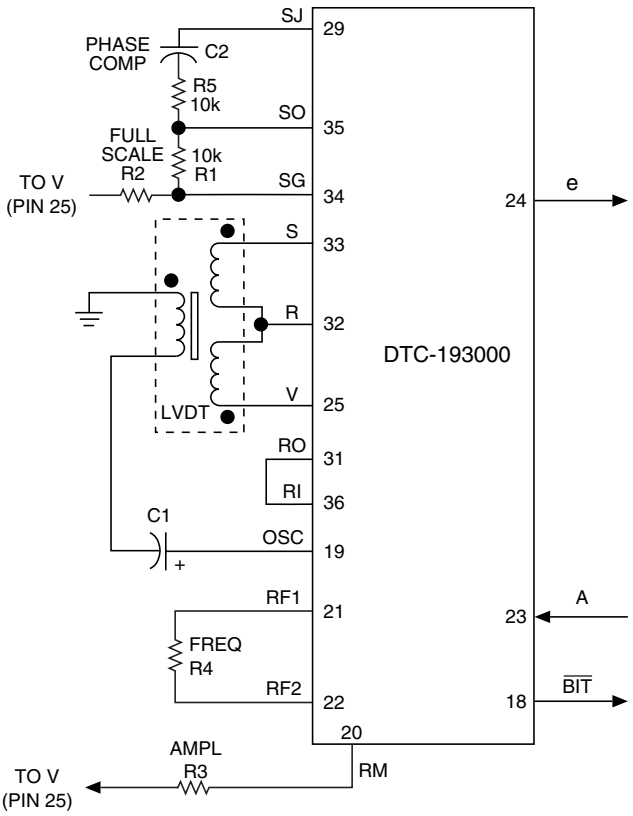
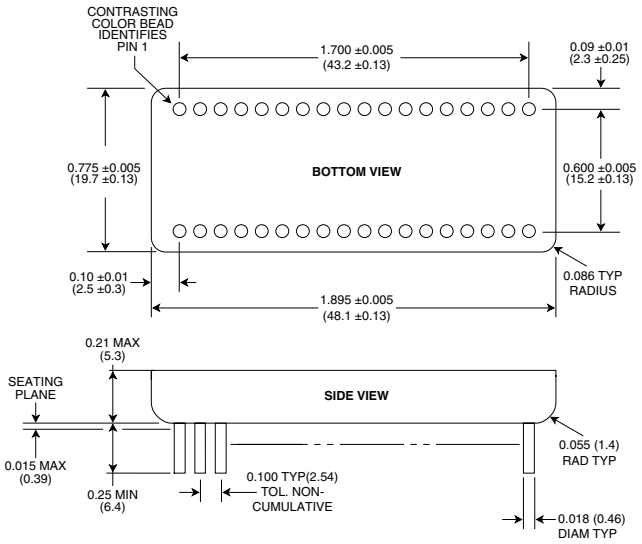



**FIGURE 7. DTC-19300 SET-UP**

**TABLE 3. BIT WEIGHTS**

| BIT | WEIGHT |
|---|---|
| 1 (MSB) | 0.5 full range = FS |
| 2 | 0.25 full range = HS |
| 3 | 0.125 full range |
| 4 | 0.0625 full range |
| 5 | 0.03125 full range |
| 6 | 0.015625 full range |
| 7 | 0.0078125 full range |
| 8 | 0.0039063 full range |
| 9 | 0.0019531 full range |
| 10 | 0.0009766 full range |
| 11 | 0.0004883 full range |
| 12 | 0.0002441 full range |
| 13 | 0.0001221 full range |
| 14 (LSB) | 0.0000610 full range |




Notes:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is electrically floating.

**FIGURE 8. DTC-19300 MECHANICAL OUTLINE**

**TABLE 4. DTC-19300 PIN FUNCTIONS**

| PIN | TITLE | I/O | FUNCTION |
|---|---|---|---|
| 1 | $\overline{EM}$ | I | Enable MSBs. Logic 0 enables digital output bits 1-6. Logic 1 disables these bits. |
| 2 | 1 | O | Digital Output Bit 1 (MSB all modes). |
| 3 | 2 | O | Digital Output Bit 2. |
| 4 | 3 | O | Digital Output Bit 3. |
| 5 | 4 | O | Digital Output Bit 4. |
| 6 | 5 | O | Digital Output Bit 5. |
| 7 | 6 | O | Digital Output Bit 6. |
| 8 | 7 | O | Digital Output Bit 7. |
| 9 | 8 | O | Digital Output Bit 8. |
| 10 | 9 | O | Digital Output Bit 9. |
| 11 | 10 | O | Digital Output Bit 10. |
| 12 | 11 | O | Digital Output Bit 11. |
| 13 | 12 | O | Digital Output Bit 12 (LSB 12 Bit Mode). |
| 14 | 13 | O | Digital Output Bit 13. |
| 15 | $\overline{14}$ | O | Digital Output Bit 14 (LSB 14 Bit Mode). |
| 16 | $\overline{EL}$ | I | Enable LSBs. Logic 0 enables digital output bits 7-14. Logic 1 disables these bits. |
| 17 | $\overline{INH}$ | I | Inhibit. Output valid 0.5 µs after $\overline{INH}$ is logic 0. |
| 18 | $\overline{BIT}$ | O | Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds approximately 65 bits. |
| 19 | OSC | O | Power oscillator output. |
| 20 | RM | I | Reference Magnitude. Power amplifier amplitude adjust. |
| 21 | RF1 | I | Reference Frequency. Power amplifier frequency adjust. |
| 22 | RF2 | I | Reference Frequency. Power amplifier frequency adjust. |
| 23 | A | I | Resolution Control. Sets resolution to 12 or 14 bits. Set for 14 bit mode by connecting the $\overline{BIT}$ (pin 18) to A (pin 23). Set for 12-bit mode by grounding A. |
| 24 | e | O | AC Error. |
| 25 | V | O | Internal DC reference voltage +5.5 V. |
| 26 | VEL | O | Velocity. |
| 27 | +15 V | I | Supply Voltage. |
| 28 | GND | — | Ground. |
| 29 | SJ | I | Summing Junction. |
| 30 | +5 V | I | Supply Voltage. |
| 31 | RO | O | Reference Out. |
| 32 | R | I | LVDT Reference input. |
| 33 | S | I | LVDT Signal input. |
| 34 | SG | I | Signal Amplifier Gain Point. |
| 35 | SO | O | Signal Amplifier Output. |
| 36 | RI | I | Full Scale Reference Input. |

## ORDERING INFORMATION

DTC-19300-XXXX

**Supplemental Process Requirements:**
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

**Accuracy:**
- 1 = 0.25% of Full Scale reading + 3 LSB (at room temp.)
- 2 = 0.05% of Full Scale reading + 3 LSB (at room temp.)

**Process Requirements:**
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

**Temperature Grade/Data Requirements:**
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

*Standard DDC Processing with burn-in and full temperature test — see table below.

**STANDARD DDC PROCESSING FOR HYBRID AND MONOLITHIC HERMETIC PRODUCTS**

| TEST | MIL-STD-883 | |
|---|---|---|
| | METHOD(S) | CONDITION(S) |
| INSPECTION | 2009, 2010, 2017, and 2032 | — |
| SEAL | 1014 | A and C |
| TEMPERATURE CYCLE | 1010 | C |
| CONSTANT ACCELERATION | 2001 | 3000g |
| BURN-IN | 1015 (note 1), 1030 (note 2) | TABLE 1 |

Notes:
1. For Process Requirement "B*" (refer to ordering information), devices may be non-compliant with MIL-STD-883, Test Method 1015, Paragraph 3.2. Contact factory for details.
2. When applicable.

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