

LVDS Product

DTC34LF86L/DTC34LR86L (Rev. 2.2)

REVISED APR. 2009

+3.3V LVDS 24Bit Flat Panel Display (FPD) Receiver - 85MHz

General Description

The DTC34LF86L/LR86L receivers convert the LVDS (Low Voltage Differential Signaling) data streams back into 28 bits of CMOS/TTL data with falling edge (DTC34LF86L) or rising edge (DTC34LR86L) clock for convenient interface with a variety of LCD panel controllers.

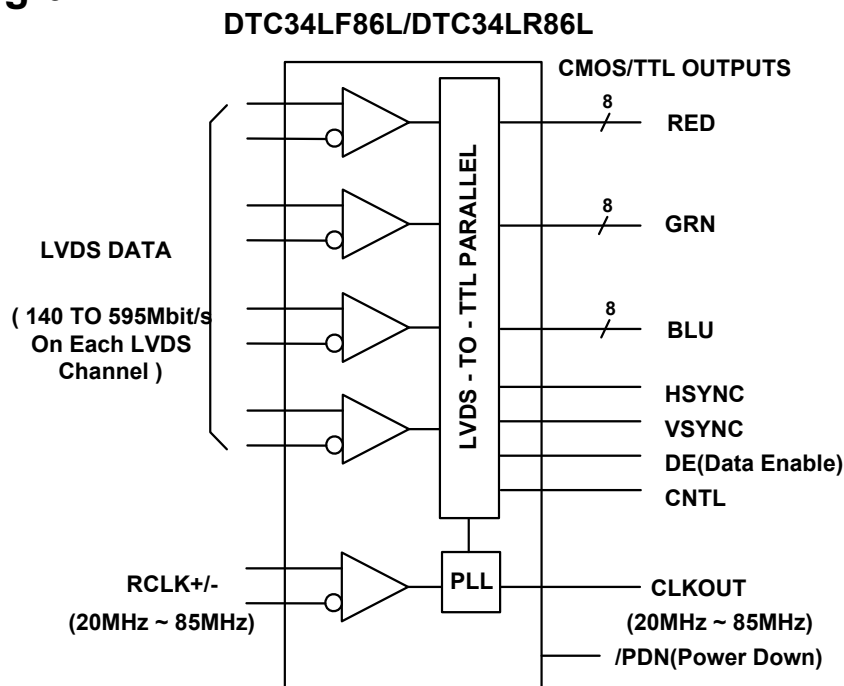
A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. A transmitter (DTC34LM85L) will inter-operate with a Falling/Rising edge receiver (DTC34LF86L/LR86L) without any translation logic.

Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec. This chip set is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Wide frequency range : 20 to 85 MHz shift clock support
- Narrow bus (10 lines) reduces cable size
- Single 3.3V supply
- Power-Down Mode
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and SXGA
- Up to 297.5 Megabytes/sec bandwidth
- Up to 2.38 Gbps throughput
- 300mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 56-lead TSSOP package (PB Free)
- Compatible with TIA/EIA-644 LVDS standard
- Compatible with the National DS90C386, THine THC63LVDF84A

Block Diagram



Electrical Characteristics

$V_{CC}=3.0 \sim 3.6V$ @ $T_a=-10 \sim +70^{\circ}C$

CMOS/TTL DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -4mA$	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 4mA$			0.4	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{CC}$			± 10	μA
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$			-50	mA

LVDS RECEIVER DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	$V_{OC} = +1.2V$			+100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{IN}	Input Current	$V_{IN} = +2.4V/0V, V_{CC} = 3.6V$			± 10	μA

RECEIVER SUPPLY CURRENT

Symbol	Parameter	Conditions	Typ	Max	Units
ICC_{RG}	Receiver Supply Current (16 Grayscale)	$CL = 8pF, f = 85MHz, V_{CC} = 3.3V$ 16 Grayscale Pattern	60		mA
ICC_{RW}	Receiver Supply Current (Worst Case)	$CL = 8pF, f = 85MHz, V_{CC} = 3.3V$ Worst Case Pattern	95		mA
ICC_{RP}	Receiver Supply Current (Power Down)	/PDN=0V 10			μA

Absolute Maximum Ratings (Note1)

Supply Voltage (V_{CC}) -0.3 to +4.0V
 CMOS/TTL Input Voltage -0.3V to ($V_{CC} + 0.3V$)
 CMOS/TTL Output Voltage -0.3V to ($V_{CC} + 0.3V$)
 LVDS Driver Output Voltage -0.3V to ($V_{CC} + 0.3V$)
 Output Short Circuit Duration Continuous
 Junction Temperature +150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 4 sec.) +260°C
 Maximum Power Dissipation @ 25°C 1.4W

(Note 1)

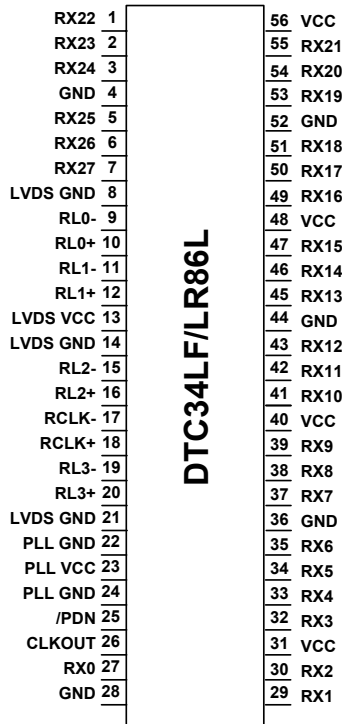
"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation

Receiver Switching Characteristics

Vcc=3.0 ~ 3.6V @ Ta=-10 ~ +70°C, T=1/f

Symbol	Para meter	Min	Typ	Max	Units
t _{RCP}	CLKOUT Period	11.76	T	50	nS
t _{RCH}	CLKOUT High Time	4.5	5.0	7.0	nS
t _{RCL}	CLKOUT Low Time	4.0	5.0	6.5	nS
t _{RCD}	RCLK+/- to CLKOUT Delay		7.0		nS
t _{RS}	TTL Data Setup to CLKOUT	3.5			nS
t _{RH}	TTL Data Hold from CLKOUT	3.5			nS
t _{TLH}	TTL Low to High Transition Time		3		nS
t _{THL}	TTL High to Low Transition Time		3		nS
t _{RDP5}	Receiver Input Data Position 0 (85MHz)	-0.4	0	0.4	nS
t _{RDP6}	Receiver Input Data Position 1 (85MHz)	T/7-0.4	T/7	T/7+0.4	nS
t _{RDP0}	Receiver Input Data Position 2 (85MHz)	2T/7-0.4	2T/7	2T/7+0.4	nS
t _{RDP1}	Receiver Input Data Position 3 (85MHz)	3T/7-0.4	3T/7	3T/7+0.4	nS
t _{RDP2}	Receiver Input Data Position 4 (85MHz)	4T/7-0.4	4T/7	4T/7+0.4	nS
t _{RDP3}	Receiver Input Data Position 5 (85MHz)	5T/7-0.4	5T/7	5T/7+0.4	nS
t _{RDP4}	Receiver Input Data Position 6 (85MHz)	6T/7-0.4	6T/7	6T/7+0.4	nS
t _{RPLLS}	Receiver Phase Lock Loop Set			10	mS

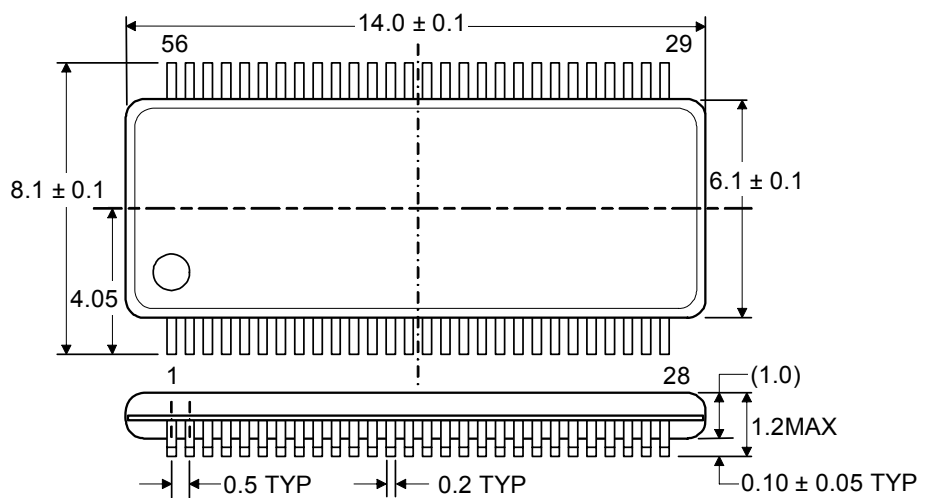
PIN OUT



PACKAGE

56 Lead Molded Thin Shrink Small Outline Package, JEDEC

U nit : millimeters



AC Timing Diagram

FIGURE 1. Test Pattern “16 Grayscale Test Pattern”

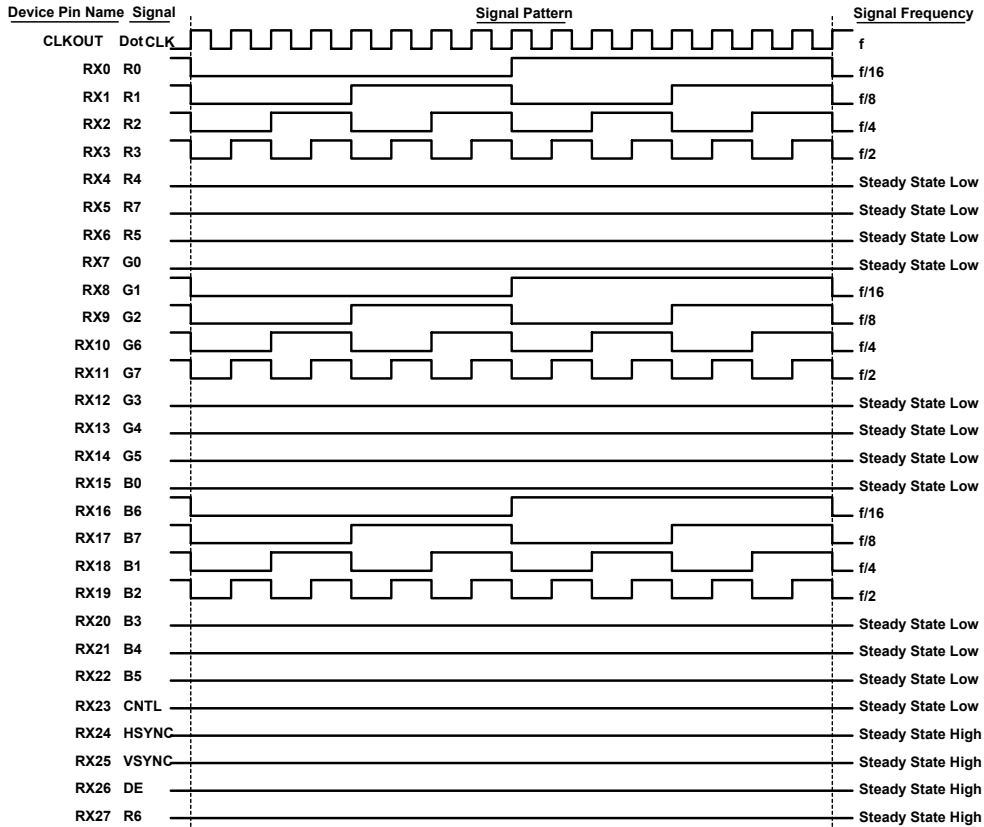


FIGURE 2. Test Pattern “Worst Case Pattern”

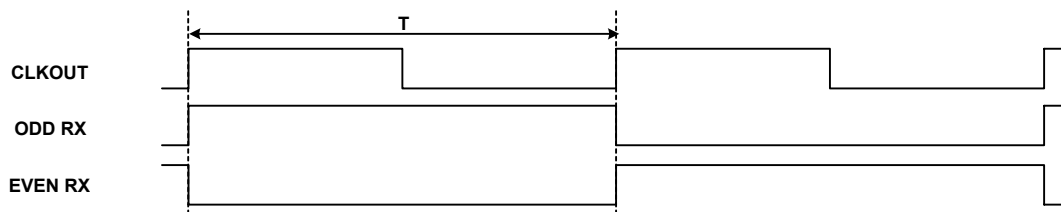
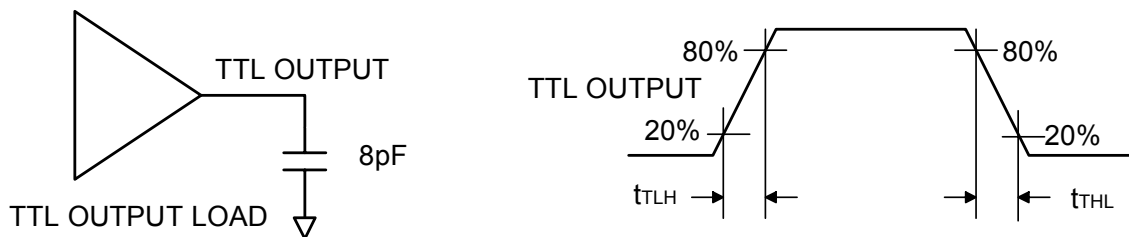


FIGURE 3. TTL Output



AC Timing Diagram (Continued)

FIGURE 4. Phase Lock Loop Set Time

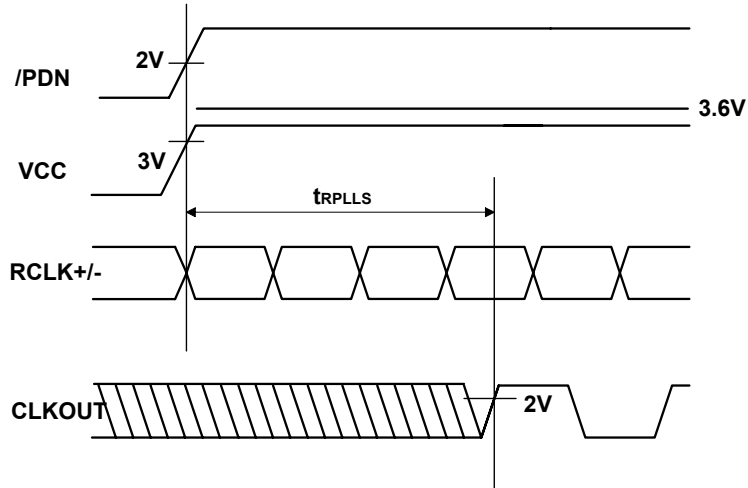
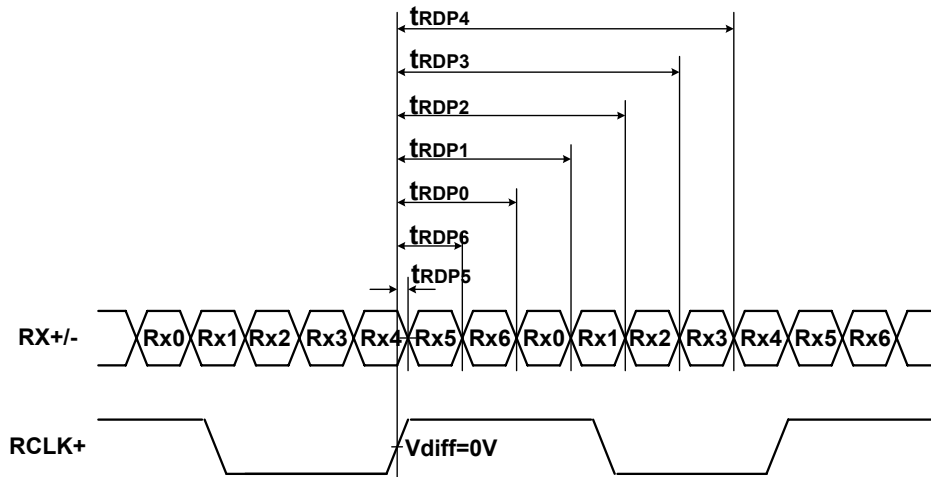


FIGURE 5. Receiver Device Operation



Note : 1) $V_{diff} = (RL+) - (RL-), \dots (RCLK+) - (RCLK-)$

FIGURE 6. LVDS Inputs Mapped Parallel TTL Data Outputs – DTC34LF86L/DTC34LR86L

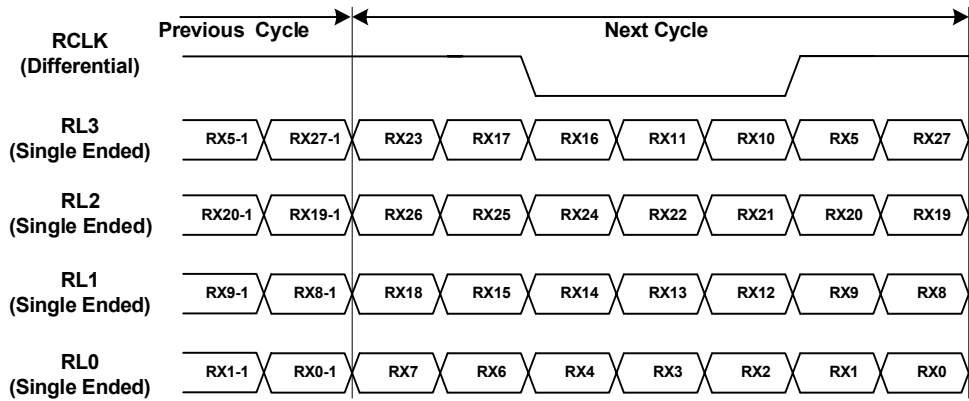
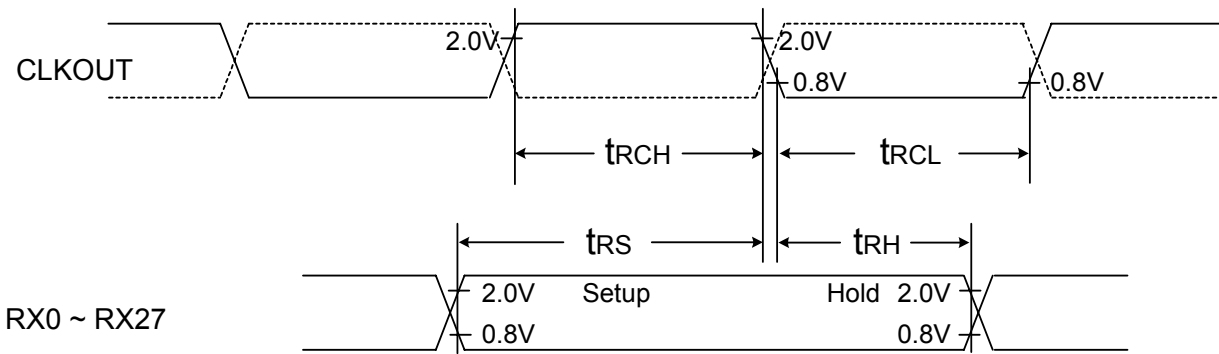
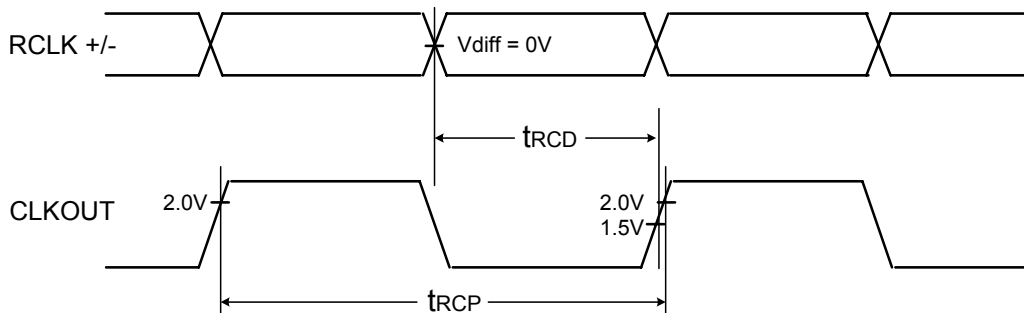


FIGURE 7. Setup/Hold and High/Low Times



Note : 1) CLKOUT: for DTC34LF86L, denoted as solid line(dotted line is for DTC34LR86L),

FIGURE 8. RCLK to CLKOUT Delay



Note : 1) $V_{diff} = (RL+) - (RL-), \dots (RCLK+) - (RCLK-)$

FIGURE 9. Package Pin Description

Pin Name	Pin #	Type	Description
RL0+, RL0-	9, 10	LVDS IN	LVDS differential data inputs.
RL1+, RL1-	11, 12	LVDS IN	
RL2+, RL2-	15, 16	LVDS IN	
RL3+, RL3-	19, 20	LVDS IN	
RCLK+, RCLK-	17, 18	LVDS IN	LVDS differential clock inputs.
RX0 ~ RX6	27,29,30,32,33,35,37	OUT	TTL level data outputs. This includes : 8 Red, 8 Green, 8 Blue, and 4 control lines (HSYNC, VSYNC, DE, CNTL)
RX7 ~ RX13	38,39,43,45,46,47,51	OUT	
RX14 ~ RX20	53,54,55,1,3,5,6	OUT	
RX21 ~ RX27	7,34,41,42,49,50,2	OUT	
CLKOUT	26	OUT	TTL level clock output. This falling edge acts as data strobe
/PDN	25	IN	TTL level input. H : Normal operation L : Power down (all output are low)
VCC	31,40,48,56	Power	Power supply pins for TTL outputs.
GND	28,36,44,52	Ground	Ground pins for TTL outputs.
LVDS VCC	13	Power	Power supply pin for LVDS inputs.
LVDS GND	8,14,2,1	Ground	Ground pins for LVDS inputs.
PLL VCC	23	Power	Power supply for PLL.
PLL GND	22,24	Ground	Ground pins for PLL.

IMPORTANT NOTICE :

- The contents of this data sheet are subject to change without prior notice.

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