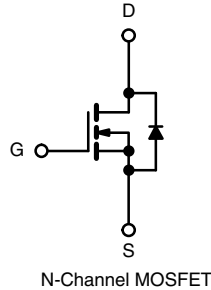


# N-Channel 80 V (D-S) MOSFET

## PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ ) Max.	$I_D$ (A)	$Q_g$ (Typ.)
80	0.0062 at $V_{GS} = 10$ V	80 <sup>a</sup>	17.1 nC



## FEATURES

- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested

## APPLICATIONS

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	80	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	80 <sup>a</sup>	A
	$T_C = 70$ °C		72	
	$T_A = 25$ °C		35 <sup>b, c</sup>	
	$T_A = 70$ °C		30 <sup>b, c</sup>	
Pulsed Drain Current ( $t = 100$ $\mu$ s)		$I_{DM}$	320	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	80 <sup>a</sup>	
	$T_A = 25$ °C		9.5 <sup>b, c</sup>	
Single Pulse Avalanche Current	$L = 0.1$ mH	$I_{AS}$	70	mJ
Single Pulse Avalanche Energy		$E_{AS}$	450	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	295	W
	$T_C = 70$ °C		160	
	$T_A = 25$ °C		5 <sup>b, c</sup>	
	$T_A = 70$ °C		3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260	

## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$t \leq 10$ s	$R_{thJA}$	12	16	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	0.39	0.54	

### Notes

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- The TO-263 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

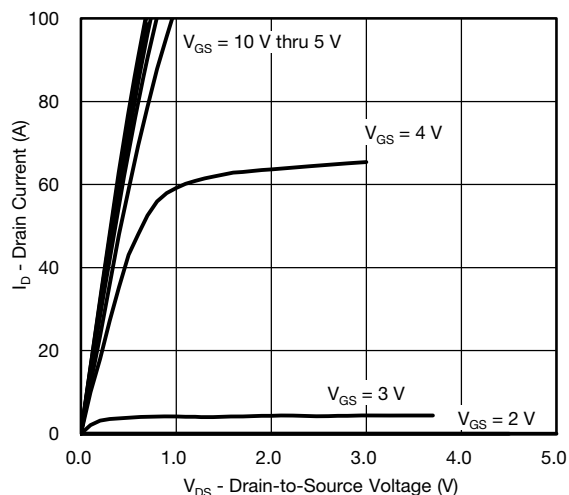
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		37		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 6		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 65 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 65 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	320			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0062	0.007	Ω
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A		60		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4255		pF
Output Capacitance	C <sub>oss</sub>			750		
Reverse Transfer Capacitance	C <sub>rss</sub>			66		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V,V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		55	84	nC
		V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 6 V, I <sub>D</sub> = 10 A		22	33	
		V <sub>DS</sub> = 50 V,V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		20	26	
Gate-Source Charge	Q <sub>gs</sub>			5.3		
Gate-Drain Charge	Q <sub>gd</sub>			7.3		
Output Charge	Q <sub>oss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		61	88	
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.5	1.4	2	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		14		ns
Rise Time	t <sub>r</sub>			10		
Turn-Off DelayTime	t <sub>d(off)</sub>			33		
Fall Time	t <sub>f</sub>			8		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 40 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 6.0 V, R <sub>g</sub> = 1 Ω		15		
Rise Time	t <sub>r</sub>			13		
Turn-Off DelayTime	t <sub>d(off)</sub>			34		
Fall Time	t <sub>f</sub>			8		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			80	A
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>				320	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A		0.76	1.3	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		36		ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			37		nC
Reverse Recovery Fall Time	t <sub>a</sub>			20		ns
Reverse Recovery Rise Time	t <sub>b</sub>			20		

**Notes**

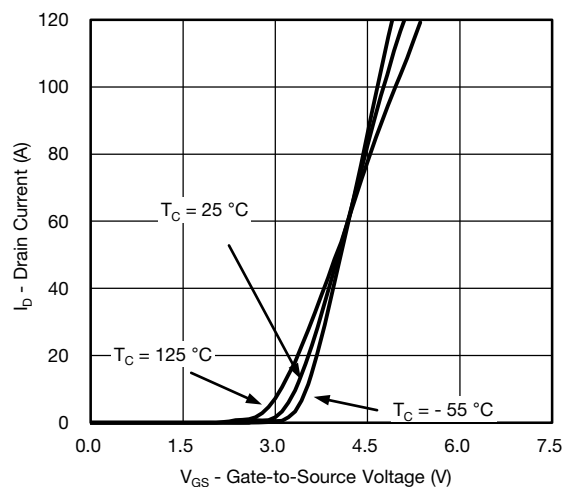
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

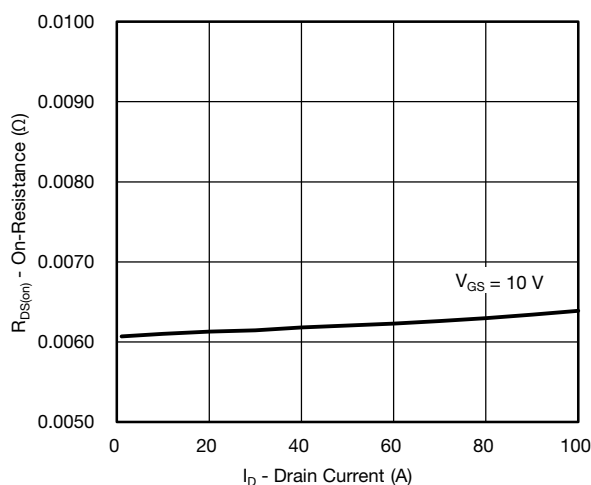
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



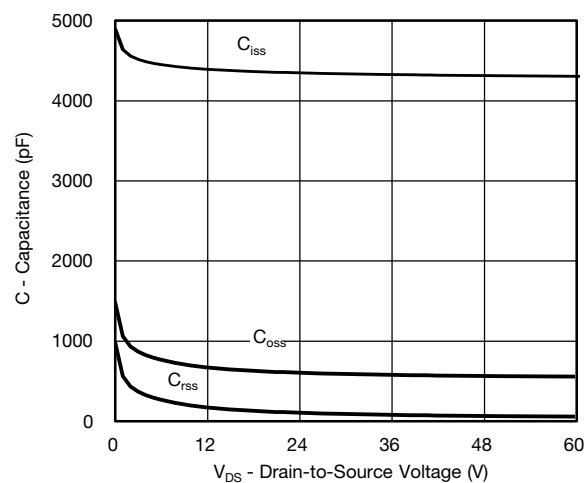
**Output Characteristics**



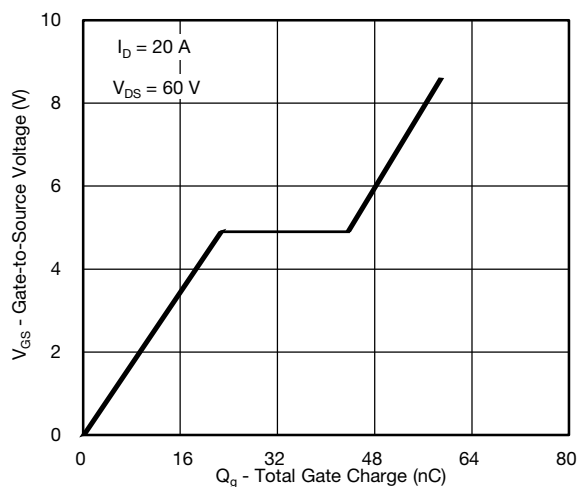
**Transfer Characteristics**



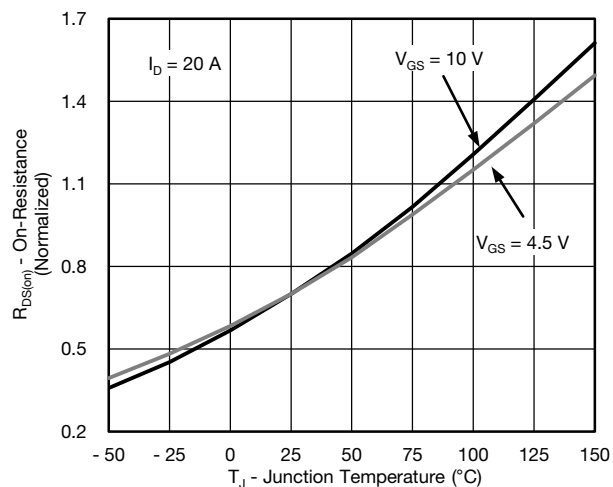
**On-Resistance vs. Drain Current**



**Capacitance**

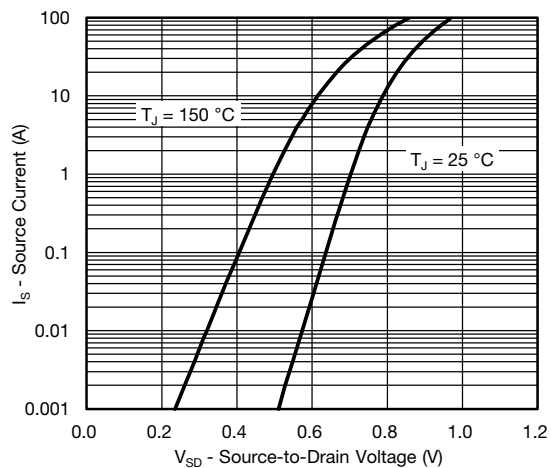


**Gate Charge**



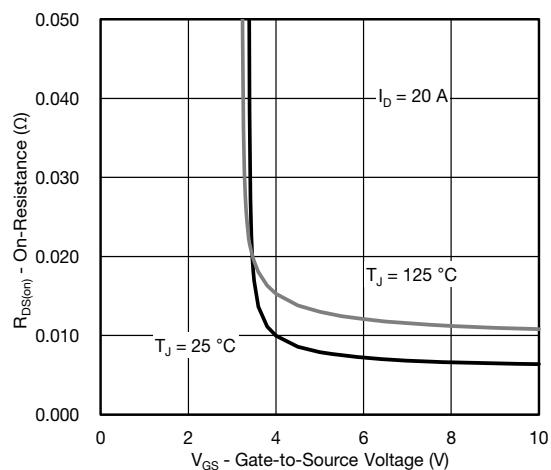
**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

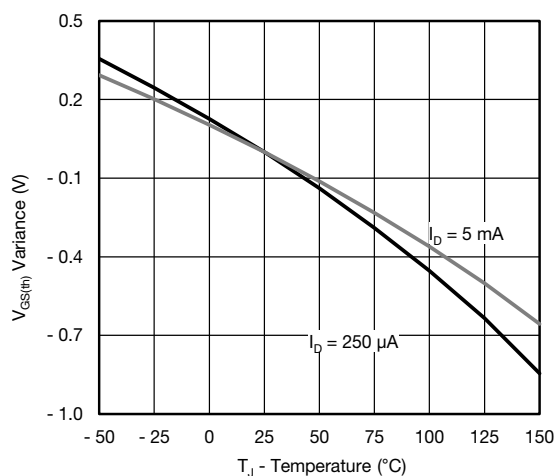


**Source-Drain Diode Forward Voltage**

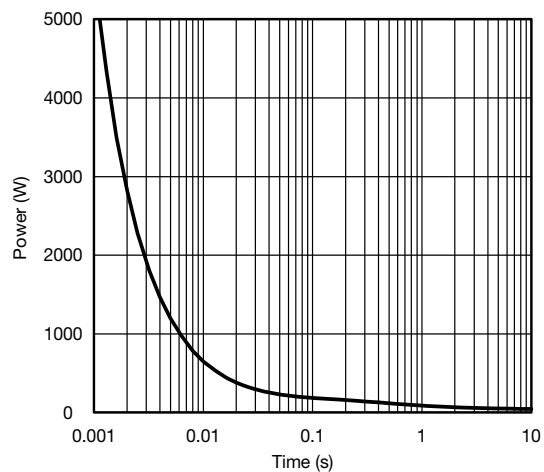
3



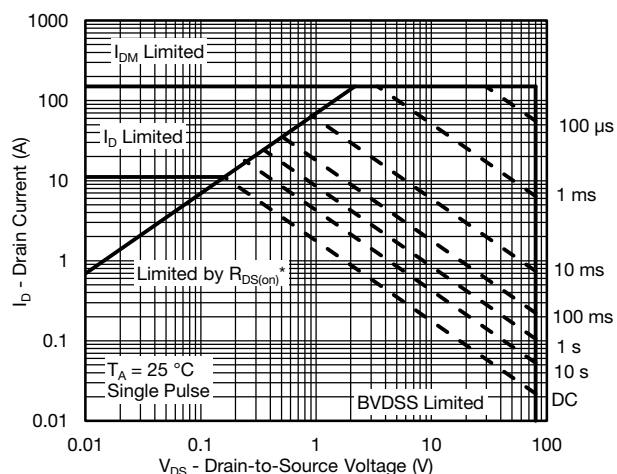
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



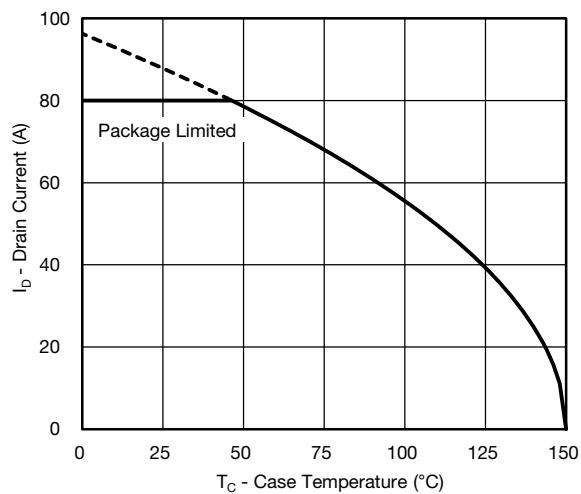
**Single Pulse Power, Junction-to-Ambient**



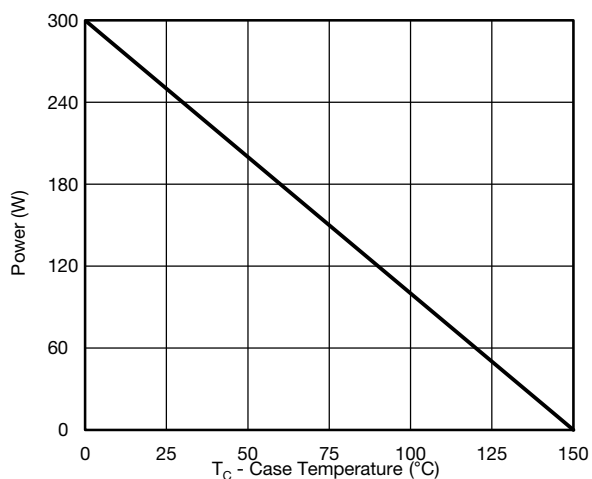
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

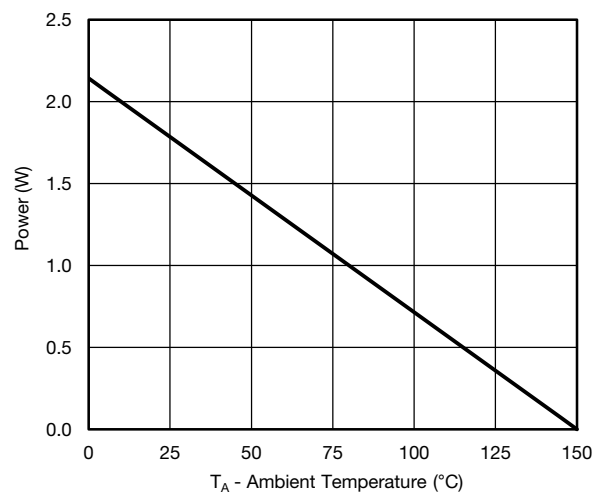
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



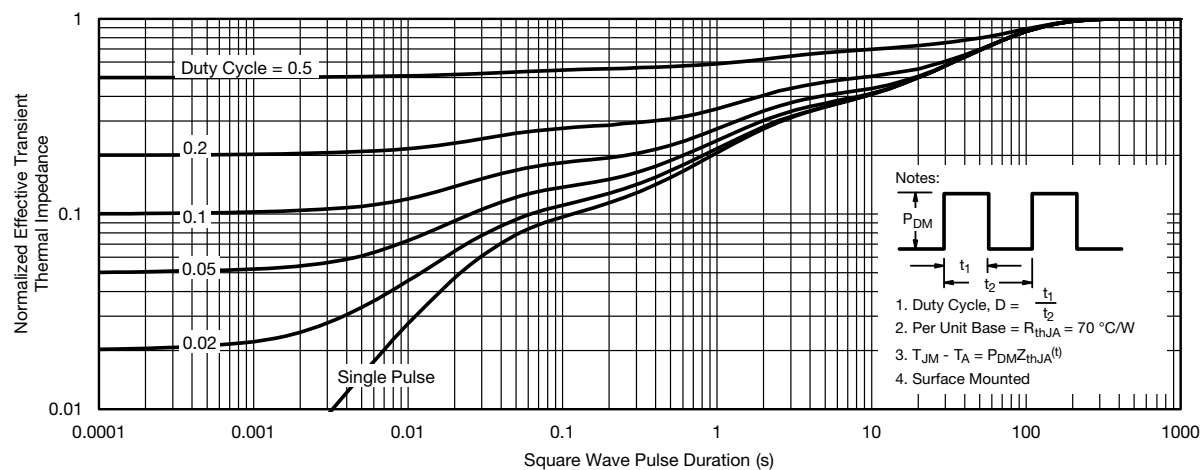
**Power, Junction-to-Case**



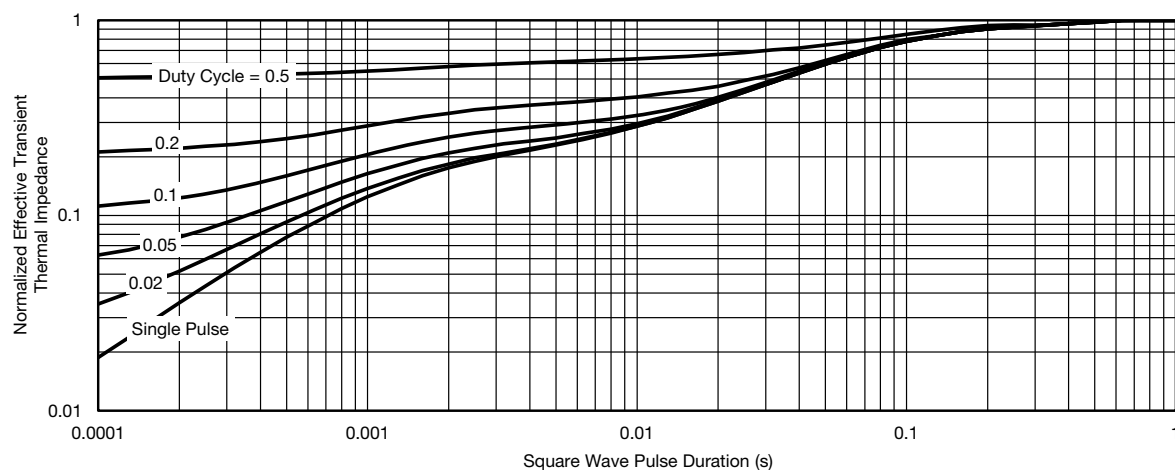
**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



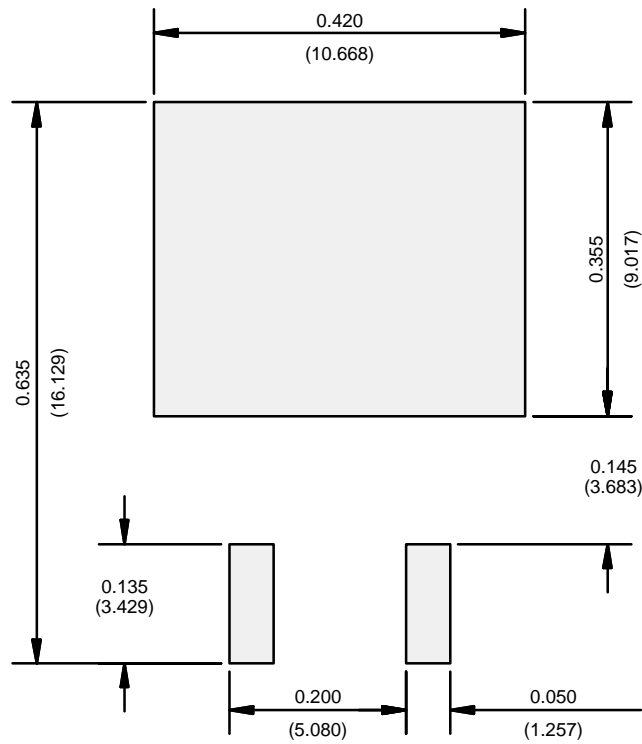
**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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