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# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
30	0.0045 at V <sub>GS</sub> = 10 V	18	8 nC			
	0.0065 at V <sub>GS</sub> = 4.5 V	14.5	OIIC			

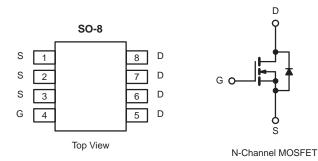
#### **FEATURES**

- Halogen-free According to IEC 61249-2-21
- TrenchFET® Power MOSFET
   100 % R<sub>g</sub> and UIS Tested

# COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

- Notebook CPU Core
  - High-Side Switch



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage Gate-Source Voltage		V <sub>DS</sub>	30 ± 20	V	
		V <sub>GS</sub>			
	T <sub>C</sub> = 25 °C		18		
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I-	13.5		
Continuous Diain Current (1 j = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	12 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		9.6 <sup>b, c</sup>		
Pulsed Drain Current		I <sub>DM</sub>	50	A	
Continuous Source Proin Diade Current	T <sub>C</sub> = 25 °C	1	4.5		
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.2 <sup>b, c</sup>		
Single Pulse Avalanche Current	1 0.1 ml l	I <sub>AS</sub>	20		
Avalanche Energy L = 0.1 mH		E <sub>AS</sub>	20	mJ	
	T <sub>C</sub> = 25 °C		5		
Maniana Barras Biasis atias	T <sub>C</sub> = 70 °C	D .	3.2	10/	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5 <sup>b, c</sup>	W	
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>		
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	$R_{thJA}$	38	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	20	25	C/ V V		

- a. Based on T<sub>C</sub> = 25 °C.
  b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.



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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V, } I_D = 250  \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	J 050 WA		34		mV/°0	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I <sub>D</sub> = 250 μA		- 4.7			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.0		2.2	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zara Oata Valla va Brain Oaraant	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1		
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C		10		μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
	<b>D</b>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.0045	0.0050		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 7 A		0.0065	0.0072	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		30		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			985		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		205			
Reverse Transfer Capacitance	C <sub>rss</sub>	1		76			
Total Gate Charge		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		18	27	nC	
	Q <sub>g</sub>			8	12		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 10 \text{ A}$		2.4			
Gate-Drain Charge	Q <sub>gd</sub>			2.3			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.3	1.3	2.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			14	25		
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		12	24		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		19	35		
Fall Time	t <sub>f</sub>	1		9	18	no	
Turn-On Delay Time	t <sub>d(on)</sub>			8	16	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		16	30		
Fall Time	t <sub>f</sub>			9	18		
<b>Drain-Source Body Diode Characteristi</b>	cs						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			4.5	^	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				50	Α	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 3 A		0.76	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			14	28	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I = 10 A dl/dt = 100 A/va T = 05 °C		5	10	nC	
Reverse Recovery Fall Time	ta	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$		8			
Reverse Recovery Rise Time	t <sub>b</sub>			6		ns	

#### Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

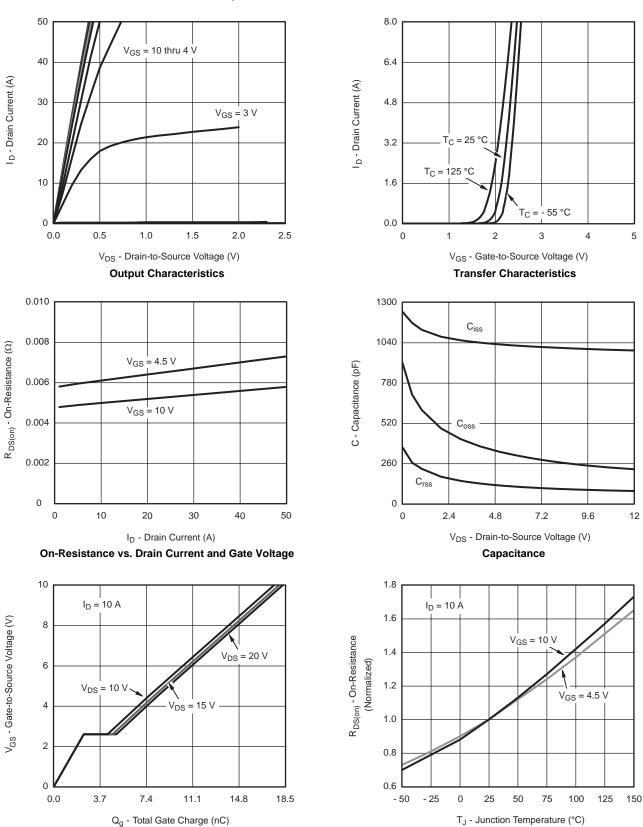
a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$ 

b. Guaranteed by design, not subject to production testing.



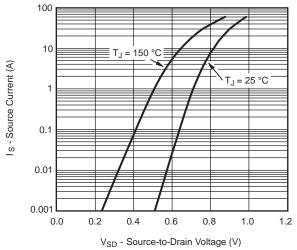


**Gate Charge** 

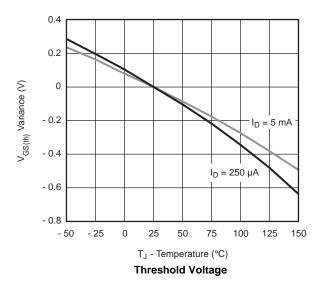


On-Resistance vs. Junction Temperature





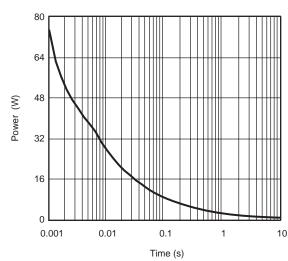
#### Source-Drain Diode Forward Voltage



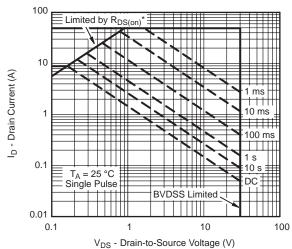
0.05  $I_D = 10 \text{ Å}$ 0.04  $R_{DS(on)}$  - On-Resistance  $(\Omega)$ 0.03 0.02  $T_J = 125$  °C 0.01 T<sub>J</sub> = 25 °C 0.00 0 3 4 5 8 9 10

V<sub>GS</sub> - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



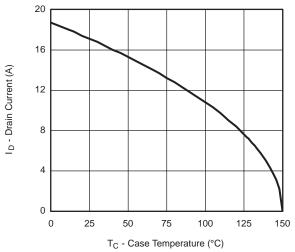
Single Pulse Power, Junction-to-Ambient



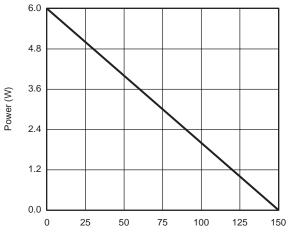
VDS - Drain-to-Source voltage (V)

\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified Safe Operating Area, Junction-to-Ambient

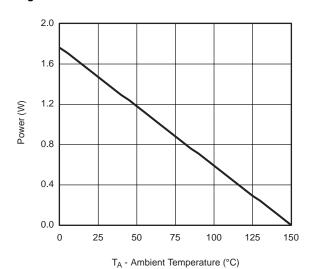




Current Derating\*



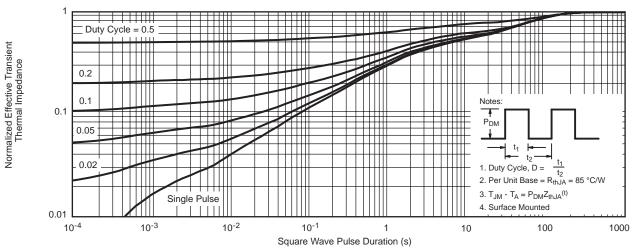




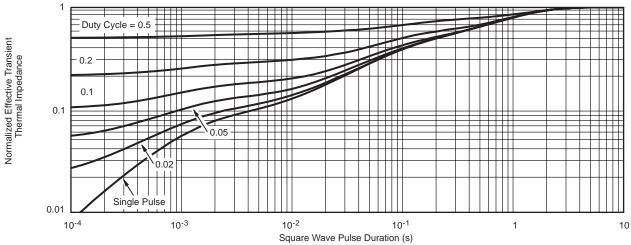
Power Derating, Junction-to-Foot

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient

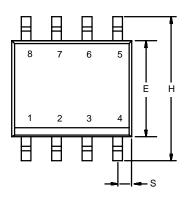


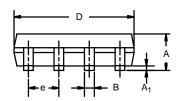
Normalized Thermal Transient Impedance, Junction-to-Foot

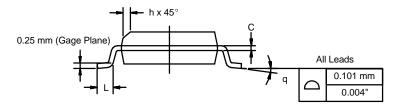




**SOIC (NARROW): 8-LEAD** JEDEC Part Number: MS-012





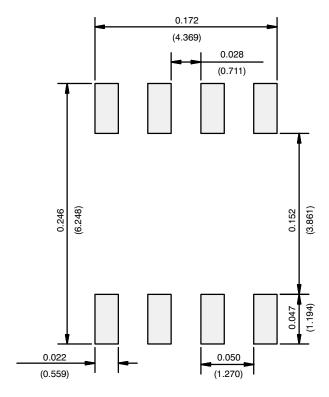


	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C 06527 Pay L 11 San 06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498

# **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)





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