P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)	Q_g (Typ.)
- 100	0.195 at V_{GS} = - 10 V	- 5.8	12
	0.200 at V_{GS} = - 7.5 V	- 5.7	
	0.207 at V_{GS} = - 6 V	- 5.6	

FEATURES

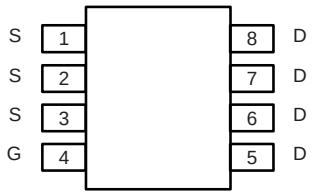
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE

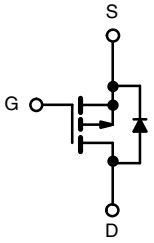
APPLICATIONS

- DC/DC Converters
- Motor Control

SO-8



Top View



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 5.8	A
	T_C = 70 °C		- 5.1	
Pulsed Drain Current		I_{DM}	- 17.4	
Avalanche Current		I_{AS}	- 12	
Single Avalanche Energy[a]	L = 0.1 mH	E_{AS}	12.2	mJ
Maximum Power Dissipation[a]	T_C = 25 °C	P_D	32.1[b]	W
	T_A = 25 °C[c]		2.5	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Limit**	**Unit**
Junction-to-Ambient (PCB Mount)[c]	R_{thJA}	50	°C/W
Junction-to-Case (Drain)	R_{thJC}	3.9	

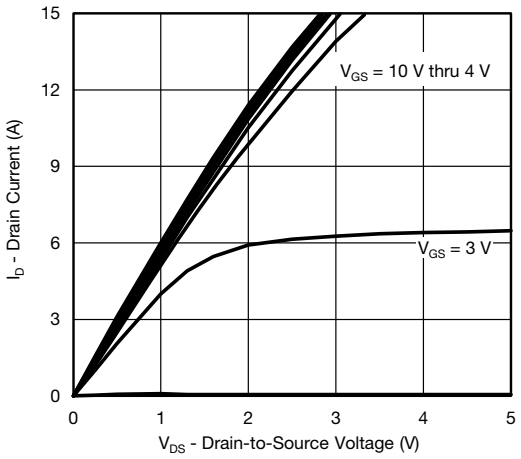
Notes:
a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. When mounted on 1" square PCB (FR-4 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{DS} = 0 V, I_D = - 250 µA	- 100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1.5		- 3.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 100 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 100 V, V_{GS} = 0 V, T_J = 125 °C			- 50	
		V_{DS} = - 100 V, V_{GS} = 0 V, T_J = 150 °C			- 250	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 10 V, V_{GS} = - 10 V	- 10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 3.6 A		0.162	0.195	Ω
		V_{GS} = - 7.5 V, I_D = - 3.5 A		0.166	0.200	
		V_{GS} = - 6 V, I_D = - 3.5 A		0.172	0.207	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 20 V, I_D = - 3.6 A		12		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 50 V, f = 1 MHz		1110		pF
Output Capacitance	C_{oss}			64		
Reverse Transfer Capacitance	C_{rss}			40		
Total Gate Charge[c]	Q_g	V_{DS} = - 50 V, V_{GS} = - 10 V, I_D = - 3.6 A		23.5	35.3	nC
		V_{DS} = - 50 V, V_{GS} = - 4.5 V, I_D = - 3.6 A		12	18	
Gate-Source Charge[c]	Q_{gs}			4		
Gate-Drain Charge[c]	Q_{gd}			5.3		
Gate Resistance	R_g	f = 1 MHz	1.3	6.5	13	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 17.2 Ω $I_D \cong$ - 2.9 A, V_{GEN} = - 10 V, R_g = 1 Ω		6	12	ns
Rise Time[c]	t_r			9	18	
Turn-Off Delay Time[c]	$t_{d(off)}$			35	53	
Fall Time[c]	t_f			10	20	
Drain-Source Body Diode Ratings and Characteristics T_C = 25 °C[b]						
Continuous Current	I_S				- 5.8	A
Pulsed Current	I_{SM}				- 17.4	
Forward Voltage[a]	V_{SD}	I_F = - 2.9 A, V_{GS} = 0 V		- 0.83	- 1.5	V
Reverse Recovery Time	t_{rr}	I_F = - 2.9 A, dI/dt = 100 A/µs		46	69	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			- 4.5	- 5.8	A
Reverse Recovery Charge	Q_{rr}			98	147	nC

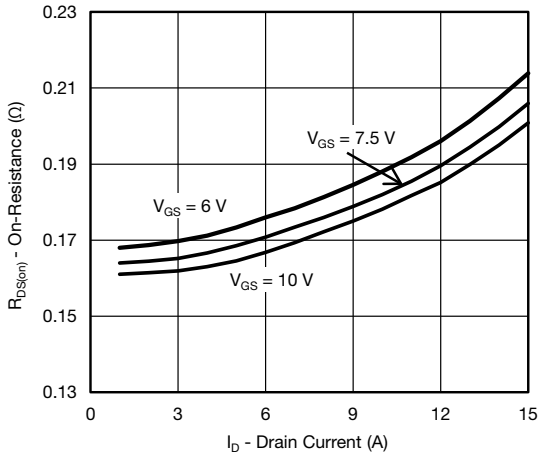
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

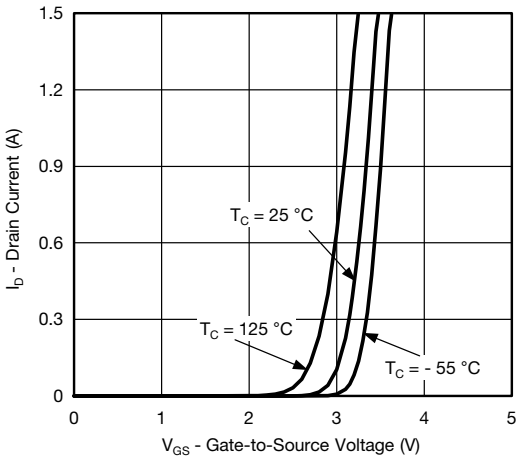
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



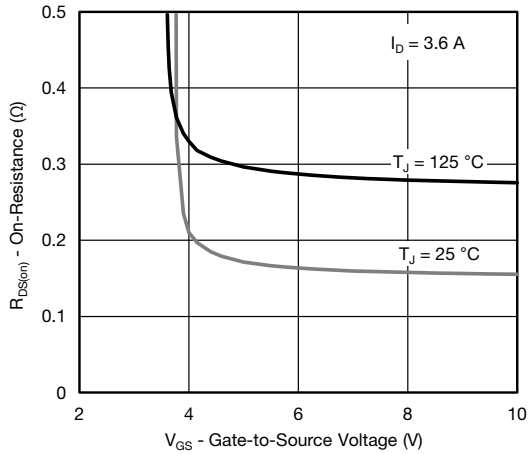
Output Characteristics



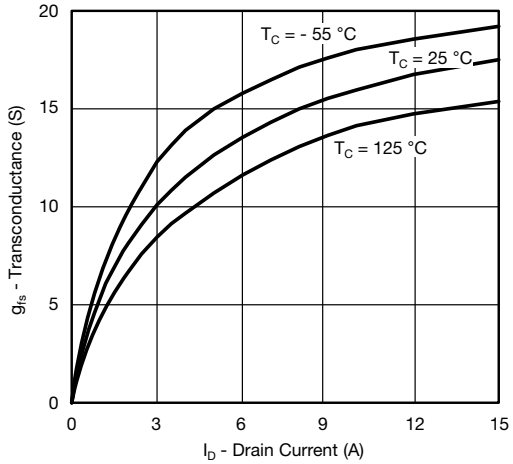
On-Resistance vs. Drain Current



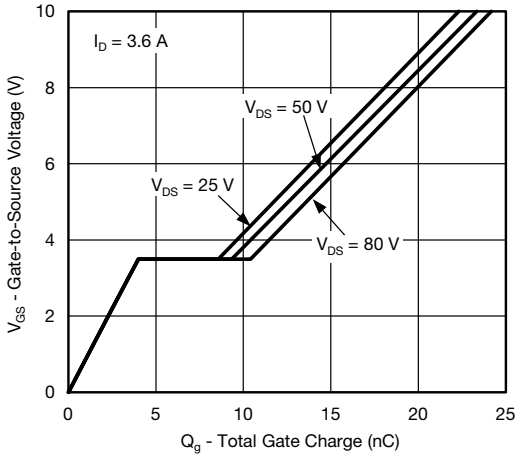
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage

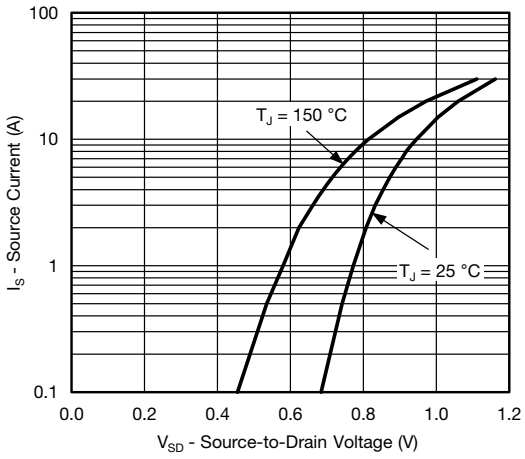


Transconductance

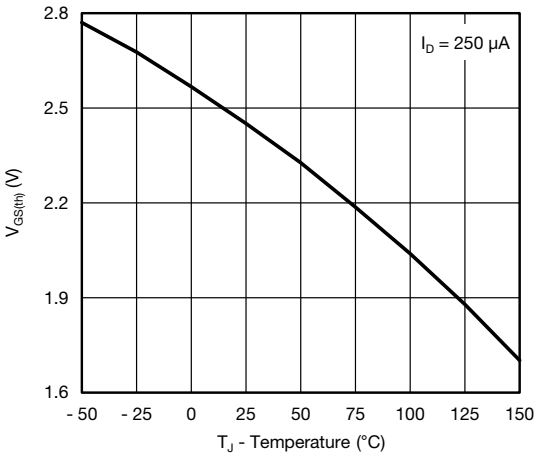


Gate Charge

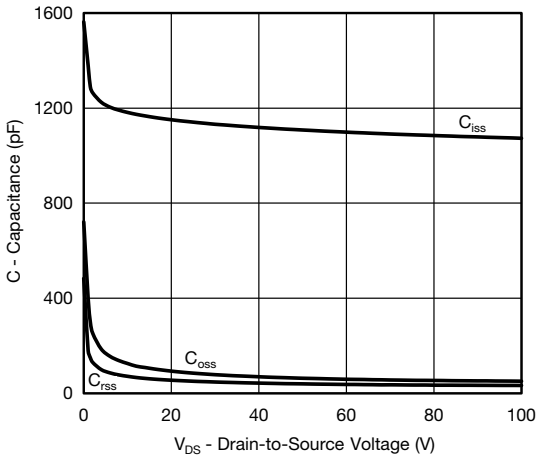
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



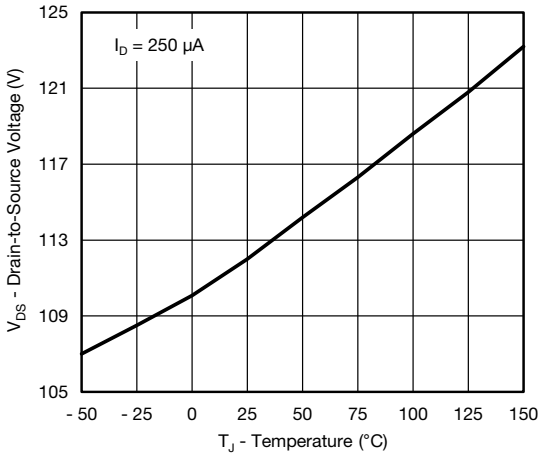
Source-Drain Diode Forward Voltage



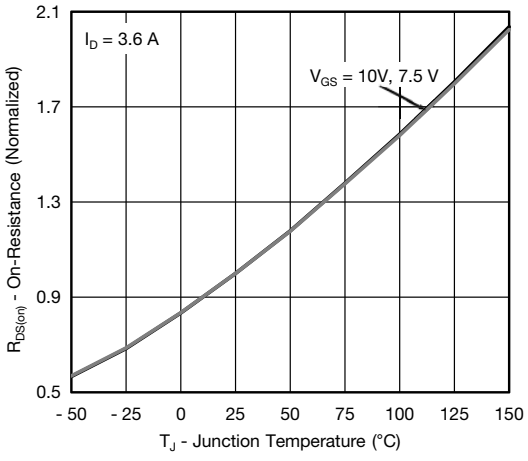
Threshold Voltage



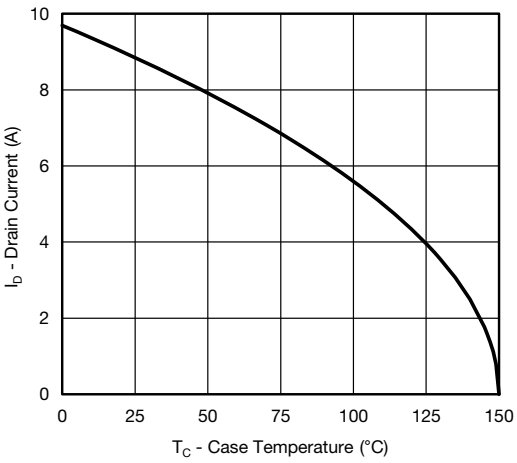
Capacitance



Drain Source Breakdown vs. Junction Temperature

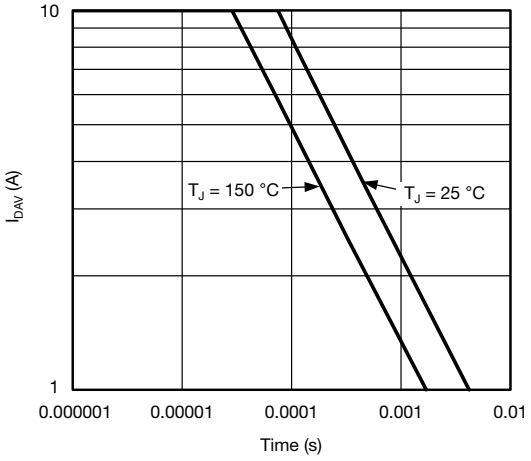


On-Resistance vs. Junction Temperature

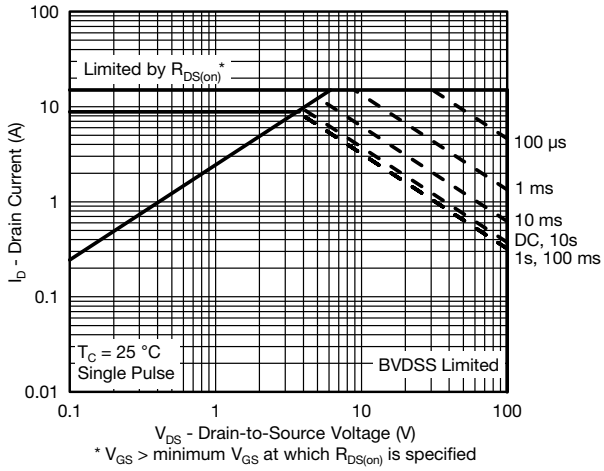


Current Derating

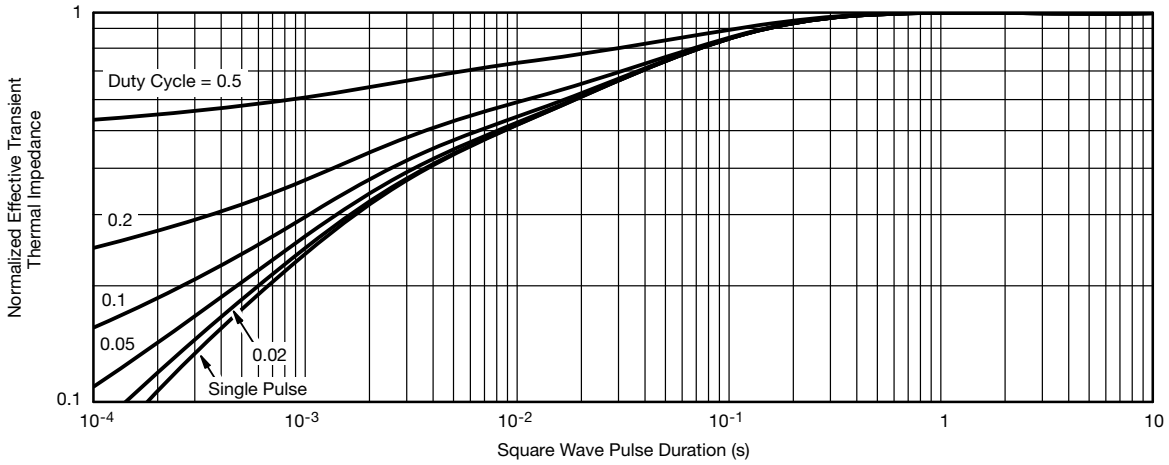
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time



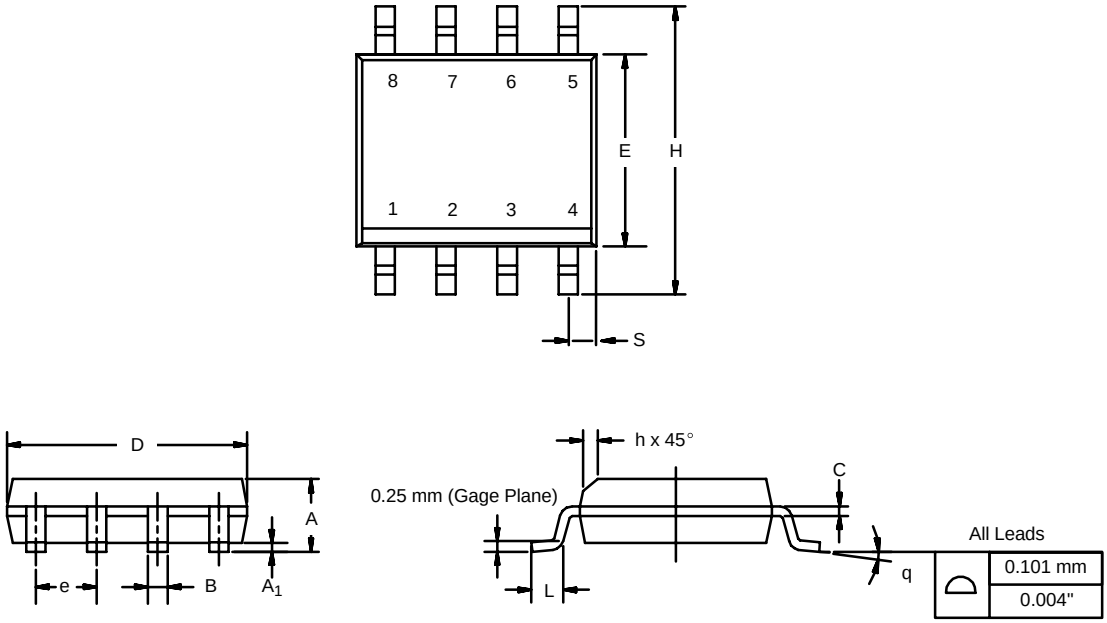
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

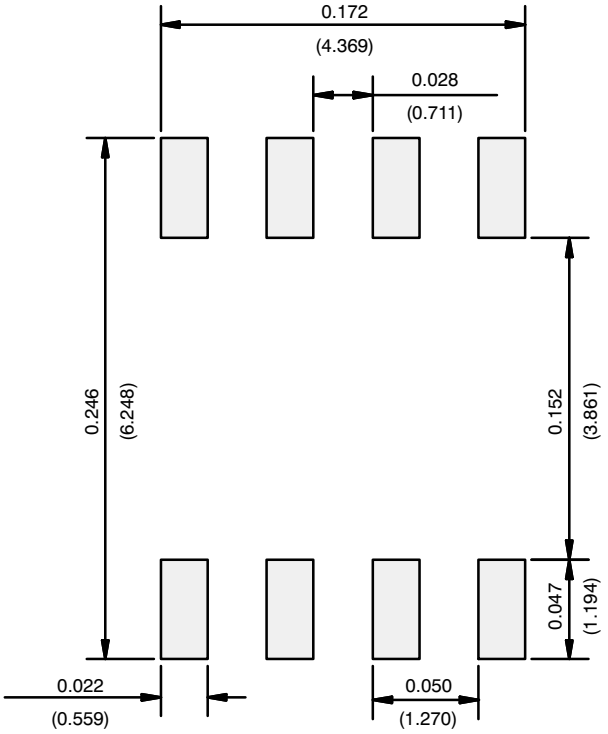
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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