

N-Channel 500-V (D-S) Super Junction MOSFET



RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	500	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.243
Q_g max. (nC)	66	
Q_{gs} (nC)	8	
Q_{gd} (nC)	14	
Configuration	Single	

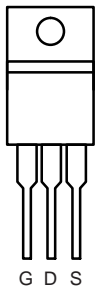
FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Low gate charge (Q_g)
- Avalanche energy rated (UIS)

APPLICATIONS

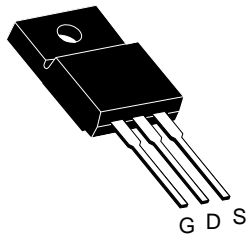
- Computing
 - PC silver box / ATX power supplies

TO-220AB



Top View

TO-220 FULLPAK

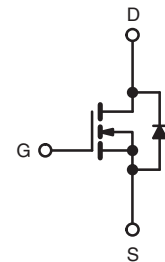


Top View

TO-247AC



Top View




N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V_{DS}	500	V	
Gate-Source Voltage	V_{GS}	± 30		
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	14.5	A
		$T_C = 100$ °C	9.2	
Pulsed Drain Current ^a	I_{DM}	28		
Linear Derating Factor		1.25	W/°C	
Single Pulse Avalanche Energy ^b	E_{AS}	136	mJ	
Maximum Power Dissipation	P_D	156	W	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	$V_{DS} = 0$ V to 80 % V_{DS}	70	V/ns	
Reverse Diode dV/dt ^d		27		
Soldering Recommendations (Peak Temperature) ^c	for 10 s	300	°C	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 3.1$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.62	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	10	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	25	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 7.5\text{ A}$	-	0.243	0.280	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 7.5\text{ A}$	-	3.9	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	1162	-	pF
Output Capacitance	C_{oss}		-	51	-	
Reverse Transfer Capacitance	C_{rss}		-	7	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$		$V_{DS} = 0\text{ V to } 400\text{ V}$, $V_{GS} = 0\text{ V}$	-	55	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	164	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$ $I_D = 7.5\text{ A}$, $V_{DS} = 400\text{ V}$	-	33	66	nC
Gate-Source Charge	Q_{gs}		-	8	-	
Gate-Drain Charge	Q_{gd}		-	14	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 400\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	15	30	ns
Rise Time	t_r		-	24	48	
Turn-Off Delay Time	$t_{d(off)}$		-	34	68	
Fall Time	t_f		-	18	36	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	0.85	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14.5	A
Pulsed Diode Forward Current	I_{SM}		-	-	28	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 7.5\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = I_S = 7.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 25\text{ V}$	-	265	-	ns
Reverse Recovery Charge	Q_{rr}		-	3.2	-	μC
Reverse Recovery Current	I_{RRM}		-	23	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

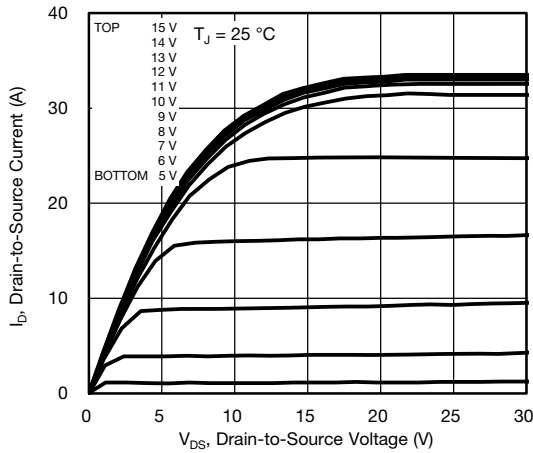


Fig. 1 - Typical Output Characteristics

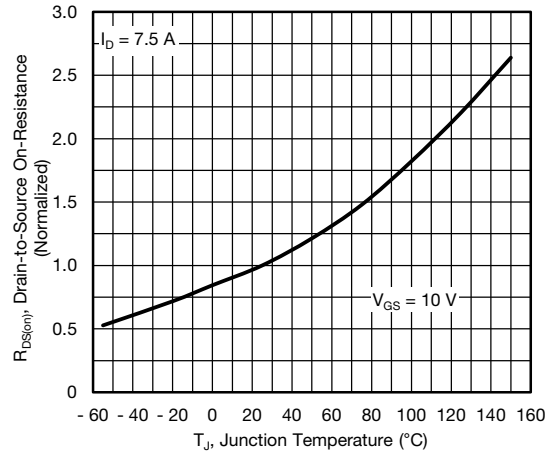


Fig. 4 - Normalized On-Resistance vs. Temperature

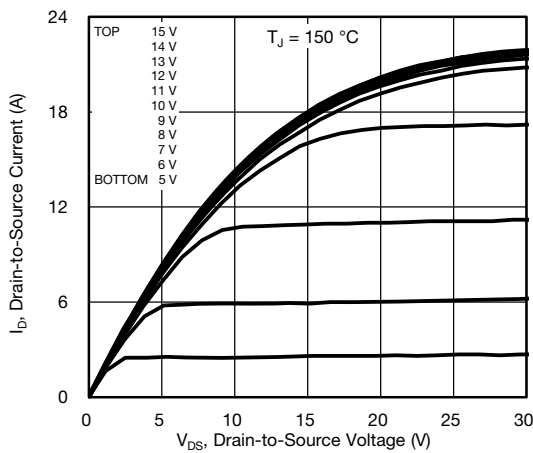


Fig. 2 - Typical Output Characteristics

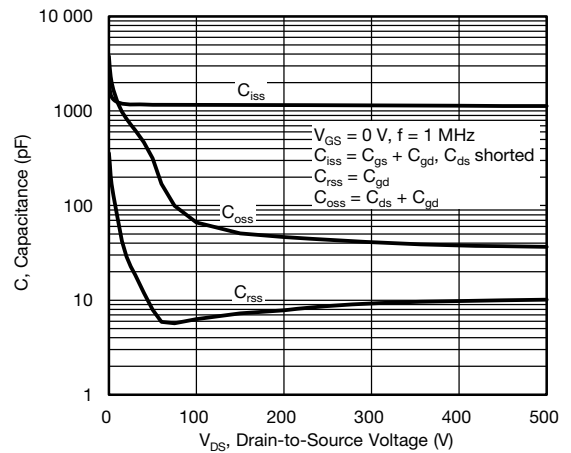


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

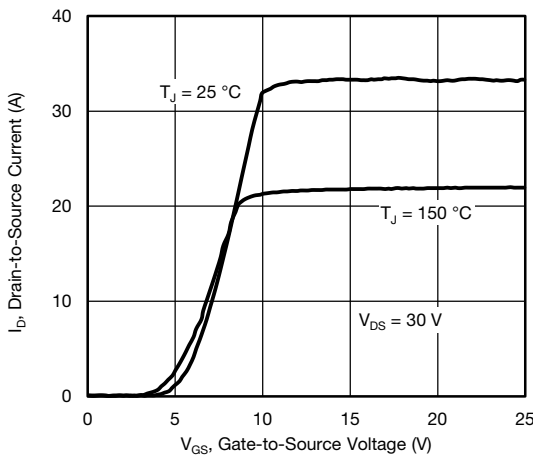


Fig. 3 - Typical Transfer Characteristics

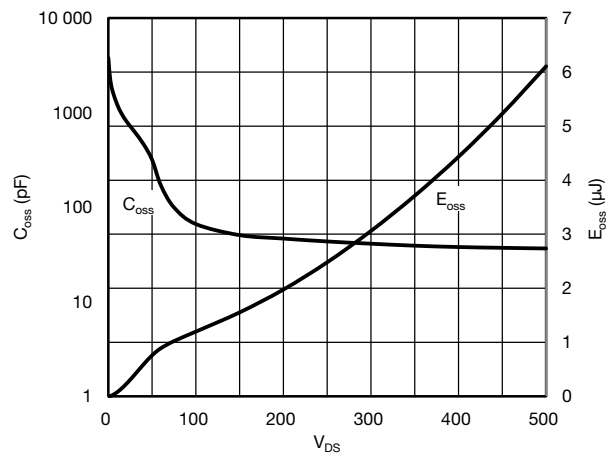


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

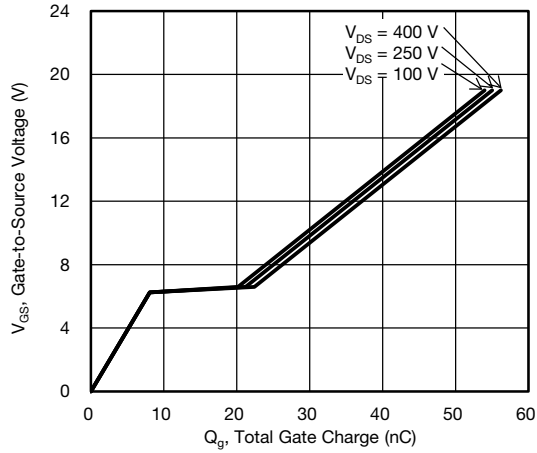


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

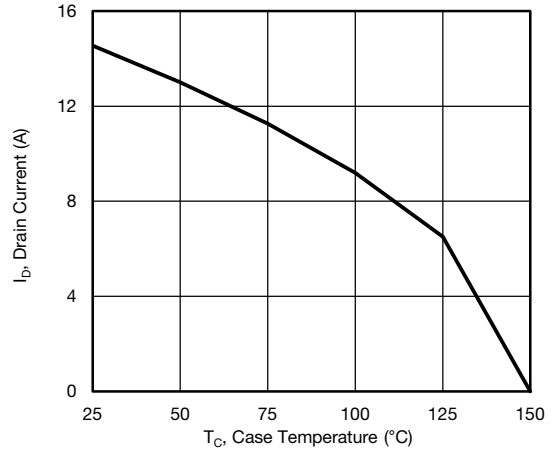


Fig. 10 - Maximum Drain Current vs. Case Temperature

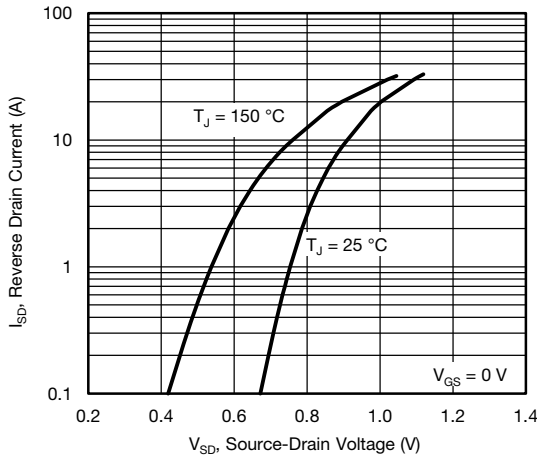


Fig. 8 - Typical Source-Drain Diode Forward Voltage

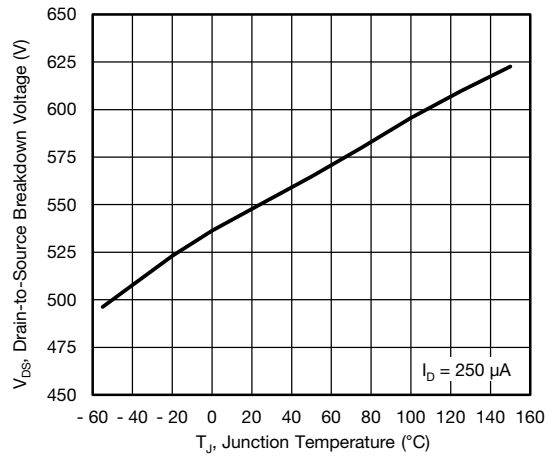


Fig. 11 - Temperature vs. Drain-to-Source Voltage

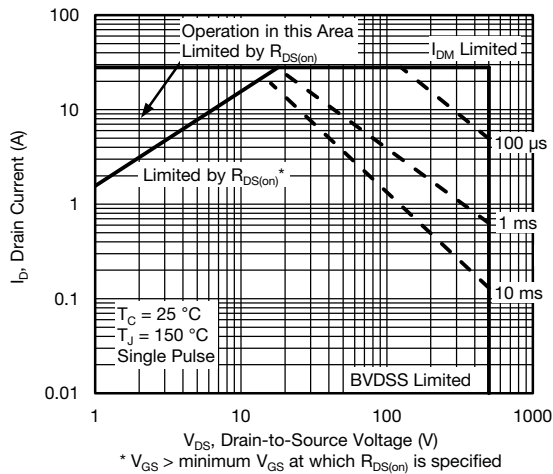


Fig. 9 - Maximum Safe Operating Area

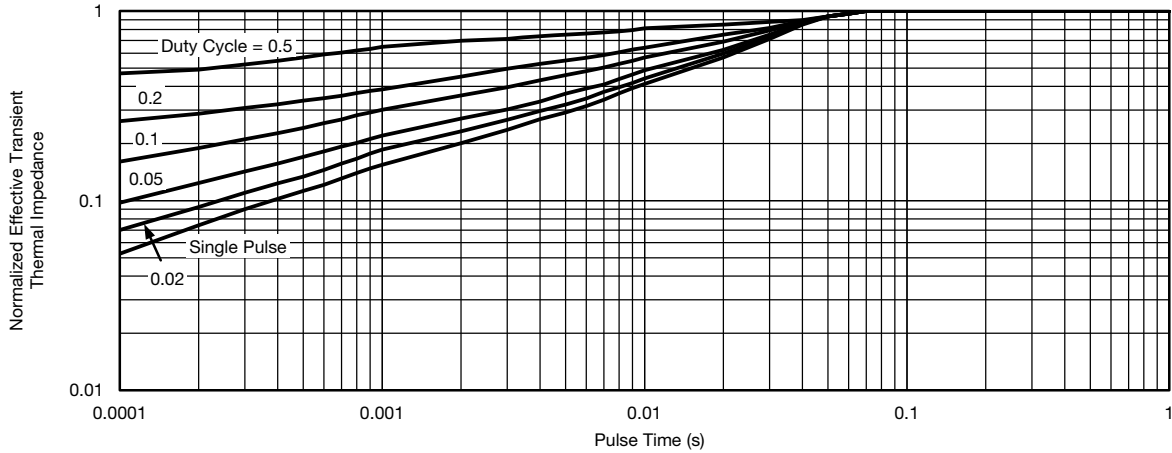


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

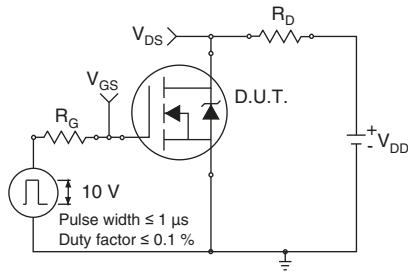


Fig. 13 - Switching Time Test Circuit

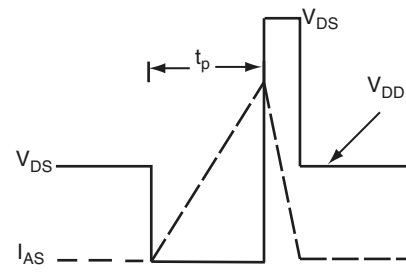


Fig. 16 - Unclamped Inductive Waveforms

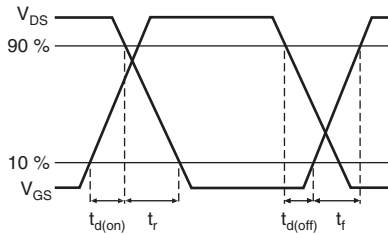


Fig. 14 - Switching Time Waveforms

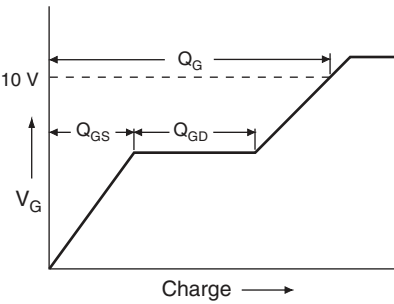


Fig. 17 - Basic Gate Charge Waveform

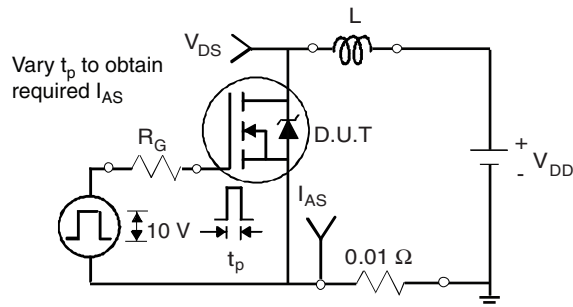


Fig. 15 - Unclamped Inductive Test Circuit

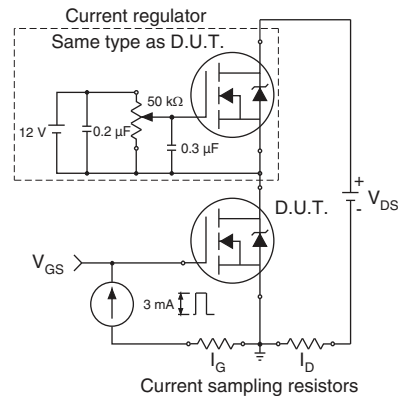
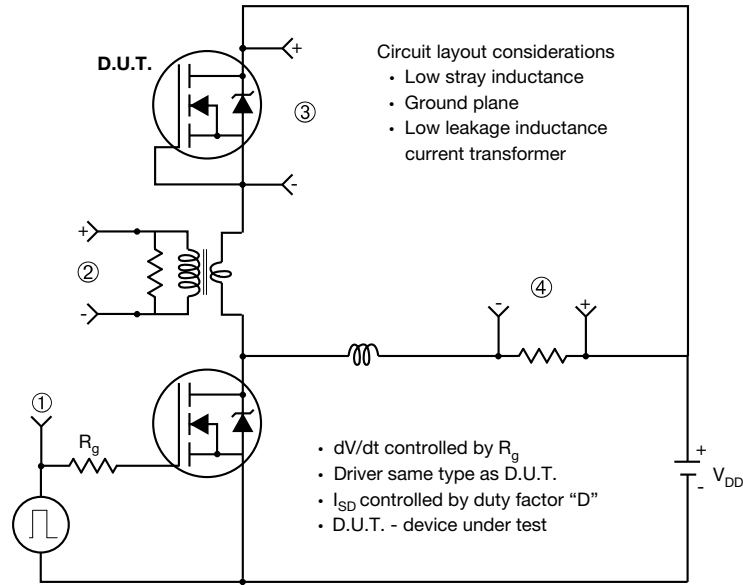


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

TO-220AB



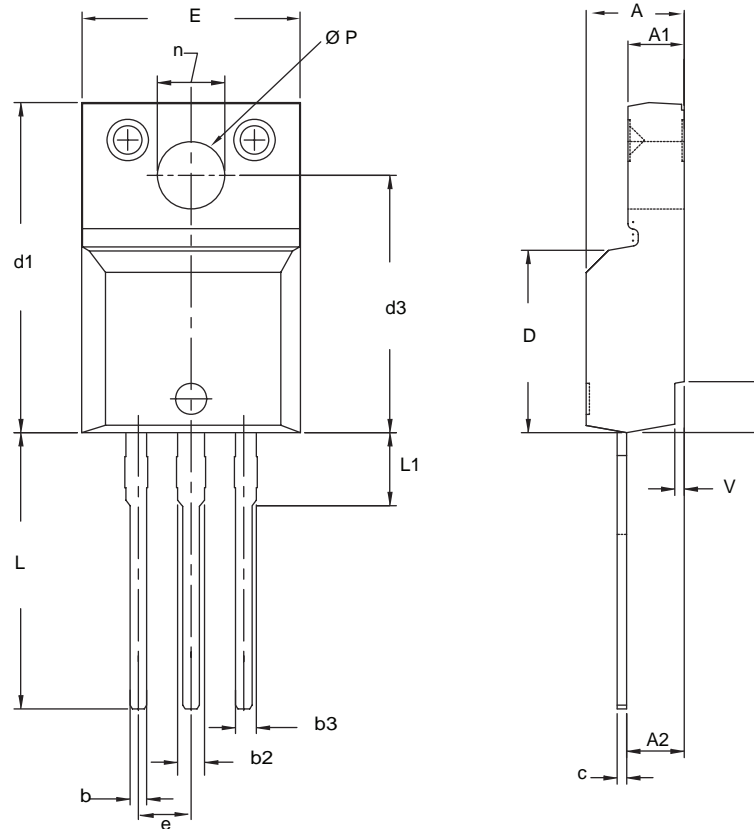
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12
DWG: 5471

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

TO-220 FULLPAK (HIGH VOLTAGE)



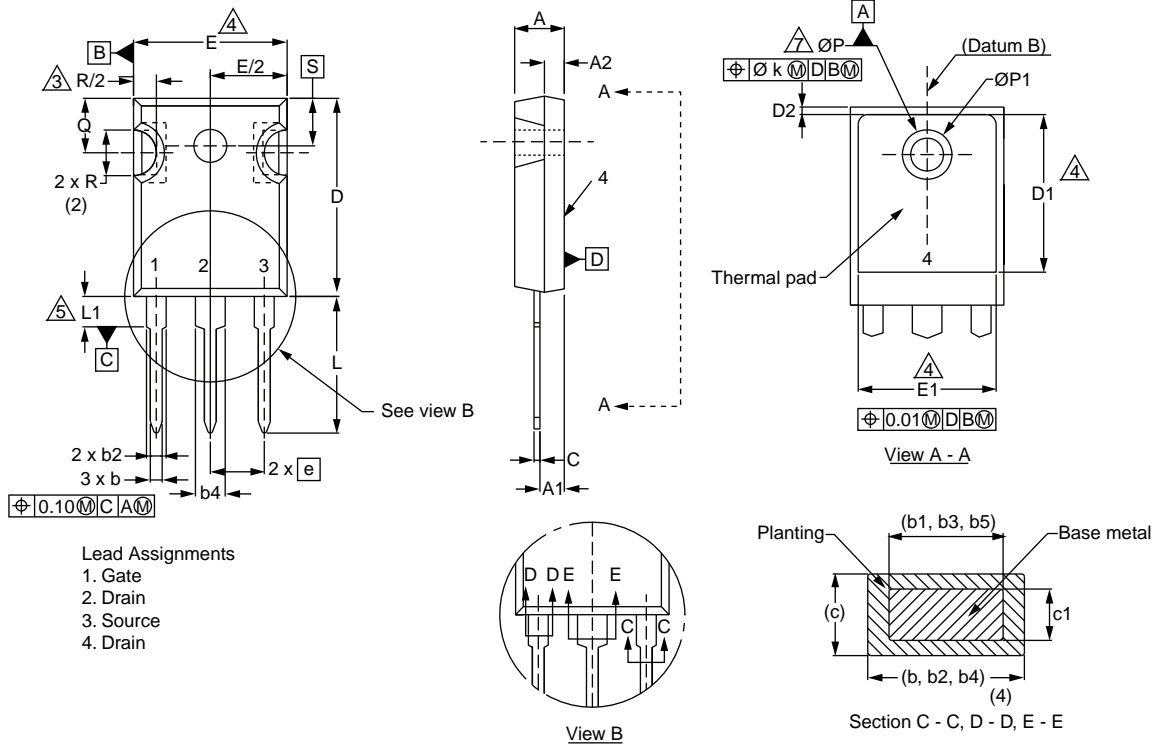
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
$\varnothing P$	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09
DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

TO-247AC (High Voltage)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
ϕk	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
ϕP	3.51	3.66	0.138	0.144
$\phi P1$	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

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