

## N-Channel 30 V (D-S) Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
30	19 at $V_{GS} = 10$ V	7.2
	23 at $V_{GS} = 4.5$ V	

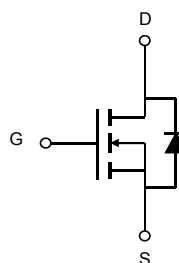
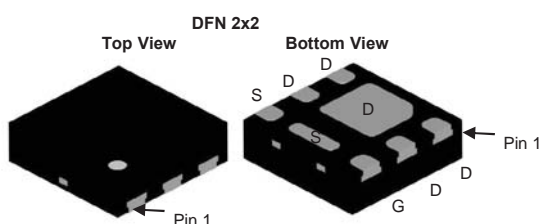
### FEATURES

- DT-Trench Power MOSFET
- Ultra Small DFN2X2 ChipScale Packaging Reduces Footprint Area


**RoHS**  
 COMPLIANT

### APPLICATIONS

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$ 7.2 <sup>a</sup>	A
		$T_C = 70^\circ\text{C}$ 6.3 <sup>a</sup>	
		$T_A = 25^\circ\text{C}$ 3.3 <sup>a, b, c</sup>	
		$T_A = 70^\circ\text{C}$ 2.1 <sup>b, c</sup>	
Pulsed Drain Current	$I_{DM}$	29	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$ 7.2 <sup>a</sup>	
		$T_A = 25^\circ\text{C}$ 3.5 <sup>b, c</sup>	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$ 2.7	W
		$T_C = 70^\circ\text{C}$ 1.08	
		$T_A = 25^\circ\text{C}$ 0.5 <sup>b, c</sup>	
		$T_A = 70^\circ\text{C}$ 0.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	250	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	46	

Notes:

- Package limited
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- The DFN2X2 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is  $80^\circ\text{C/W}$ .

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		23		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 5.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0		2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V			± 5	μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	25			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8 A		19	23	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A		23	28	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 24 V, I <sub>D</sub> = 8 A		30		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		510		pF
Output Capacitance	C <sub>oss</sub>			77		
Reverse Transfer Capacitance	C <sub>rss</sub>			51		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8 A		9		nC
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A		7		
Gate-Source Charge	Q <sub>gs</sub>			1.8		
Gate-Drain Charge	Q <sub>gd</sub>			1.5		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		2.9		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 8 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		8		ns
Rise Time	t <sub>r</sub>			10		
Turn-Off Delay Time	t <sub>d(off)</sub>			25		
Fall Time	t <sub>f</sub>			7		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 5 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		12		
Rise Time	t <sub>r</sub>			17		
Turn-Off Delay Time	t <sub>d(off)</sub>			37		
Fall Time	t <sub>f</sub>			11		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			7.2	A
Pulse Diode Forward Current	I <sub>SM</sub>				29	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1 A, V <sub>GS</sub> = 0 V		0.7	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 8 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		23	50	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			9	18	nC
Reverse Recovery Fall Time	t <sub>a</sub>			8		ns
Reverse Recovery Rise Time	t <sub>b</sub>			10		

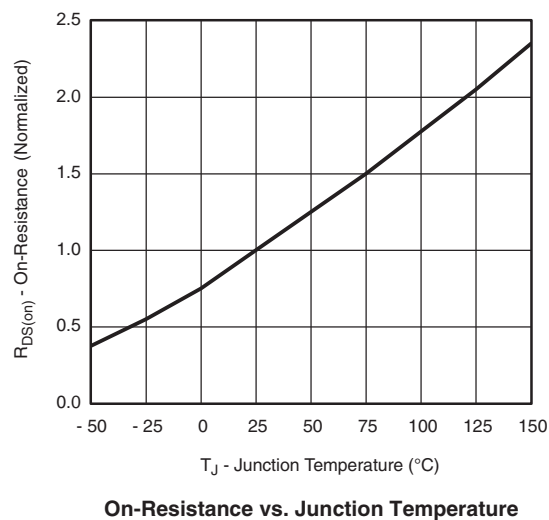
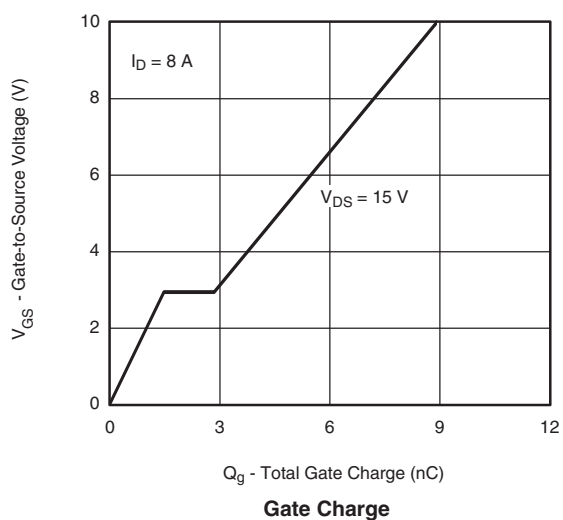
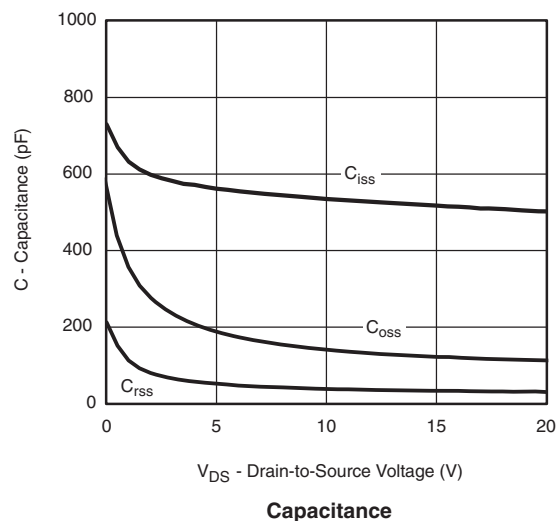
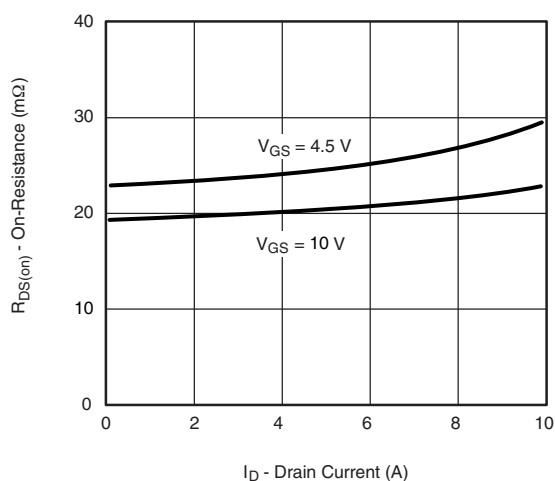
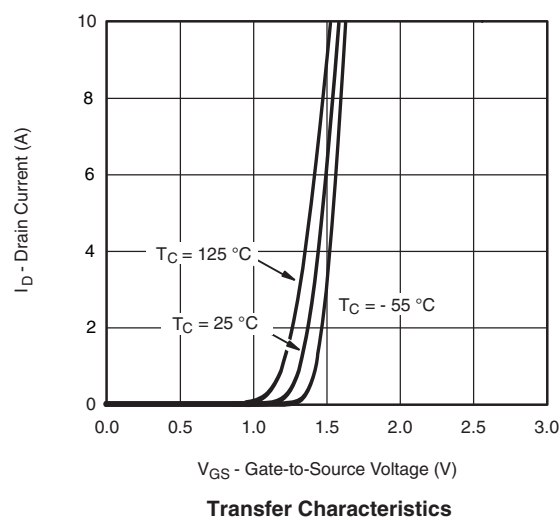
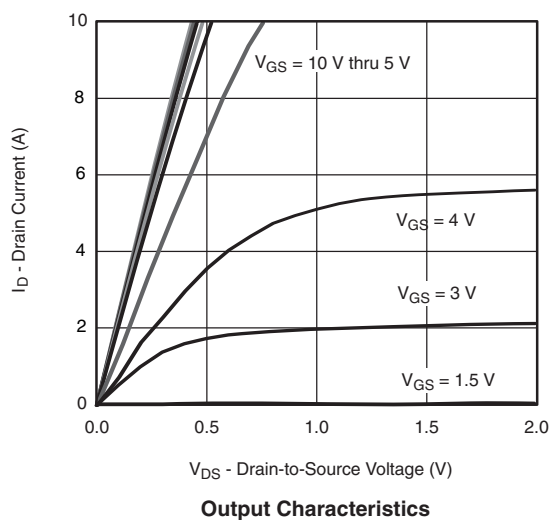
Notes:

 a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

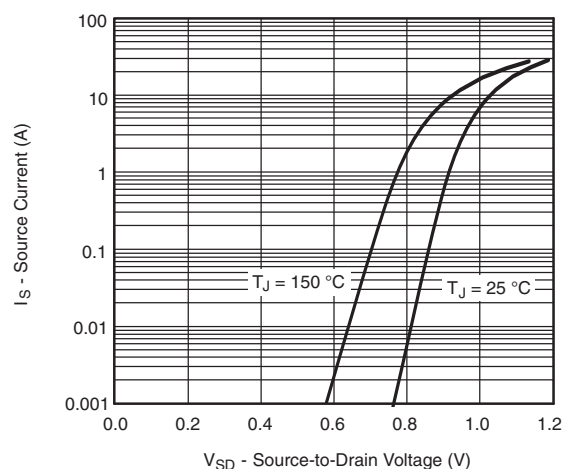
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

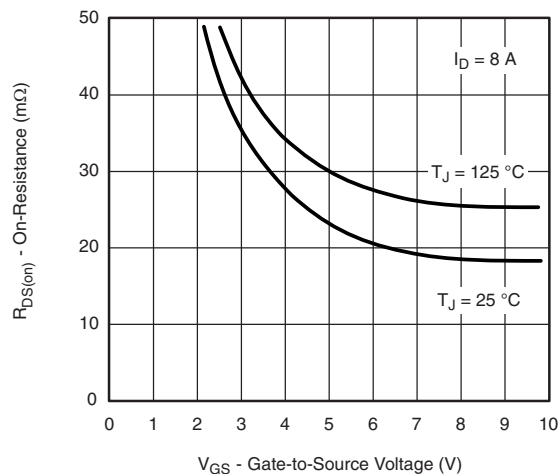
**TYPICAL CHARACTERISTIC** (25 °C, unless otherwise noted)



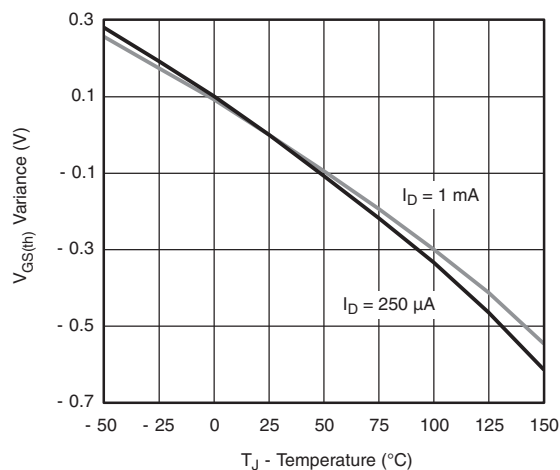
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



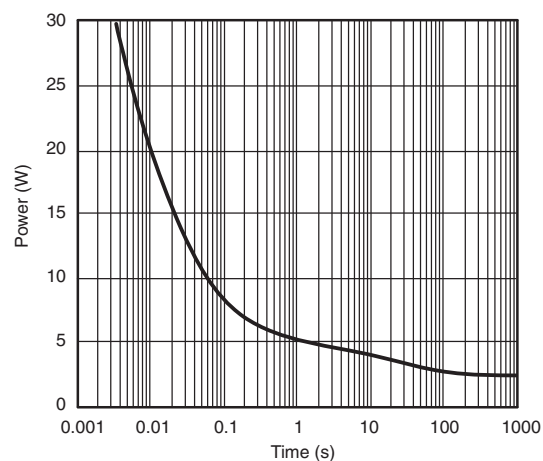
**Source-Drain Diode Forward Voltage**



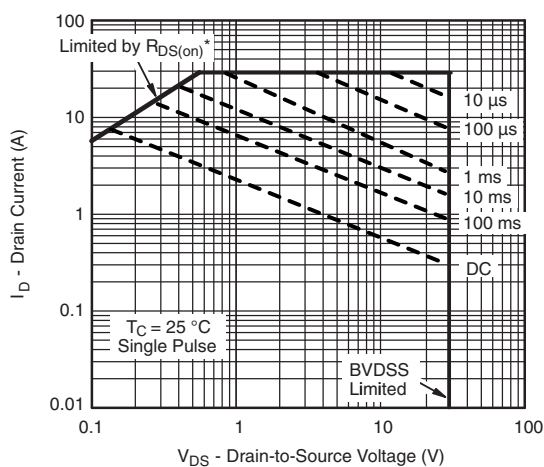
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



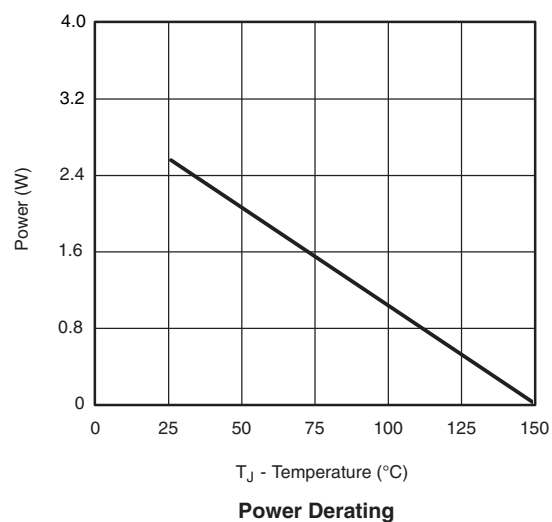
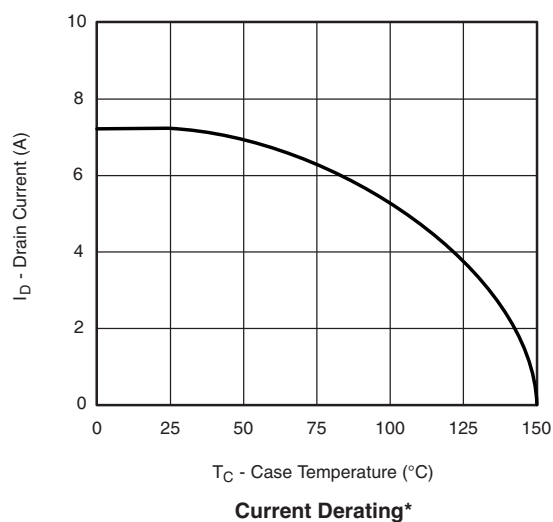
**Single Pulse Power (Junction-to-Ambient)**



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

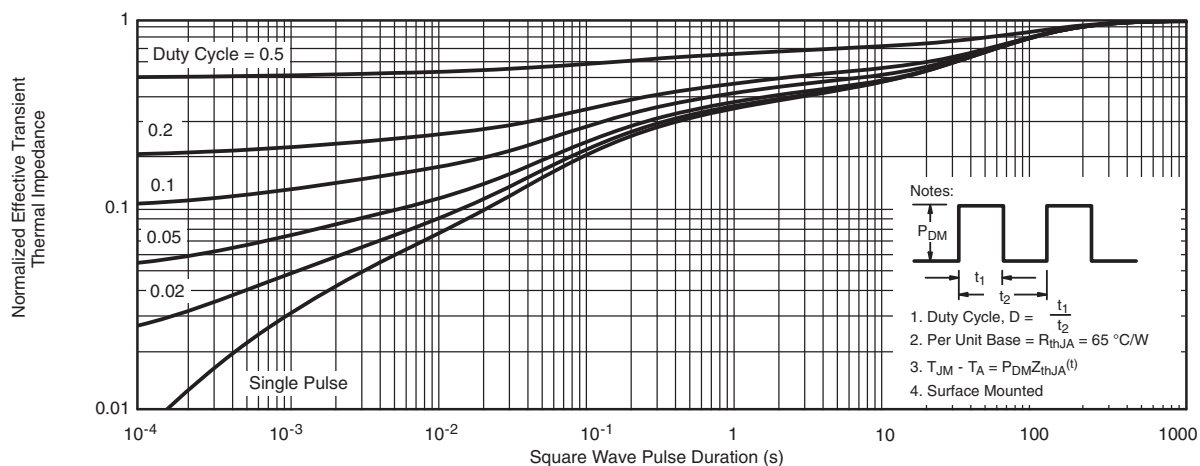
**Safe Operating Area, Junction-to-Case**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

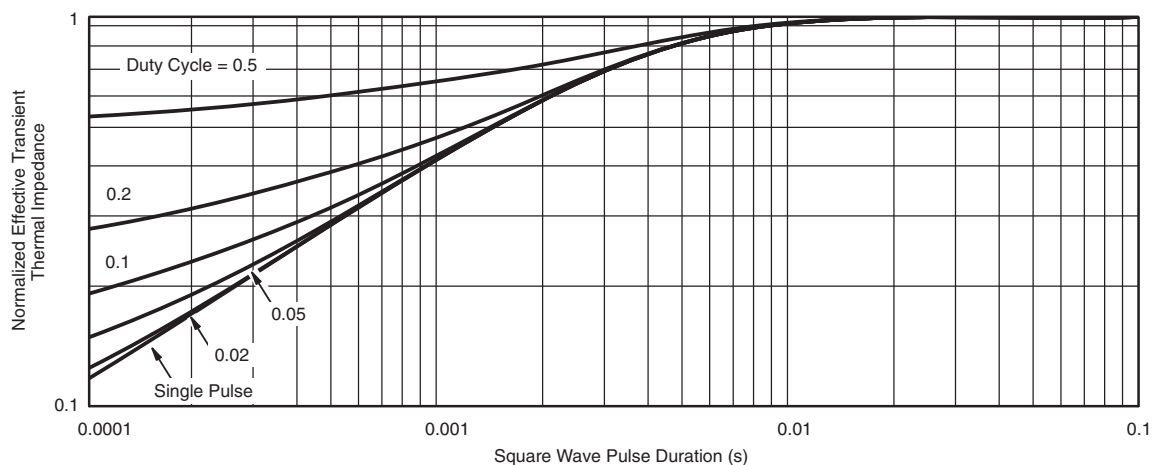


\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

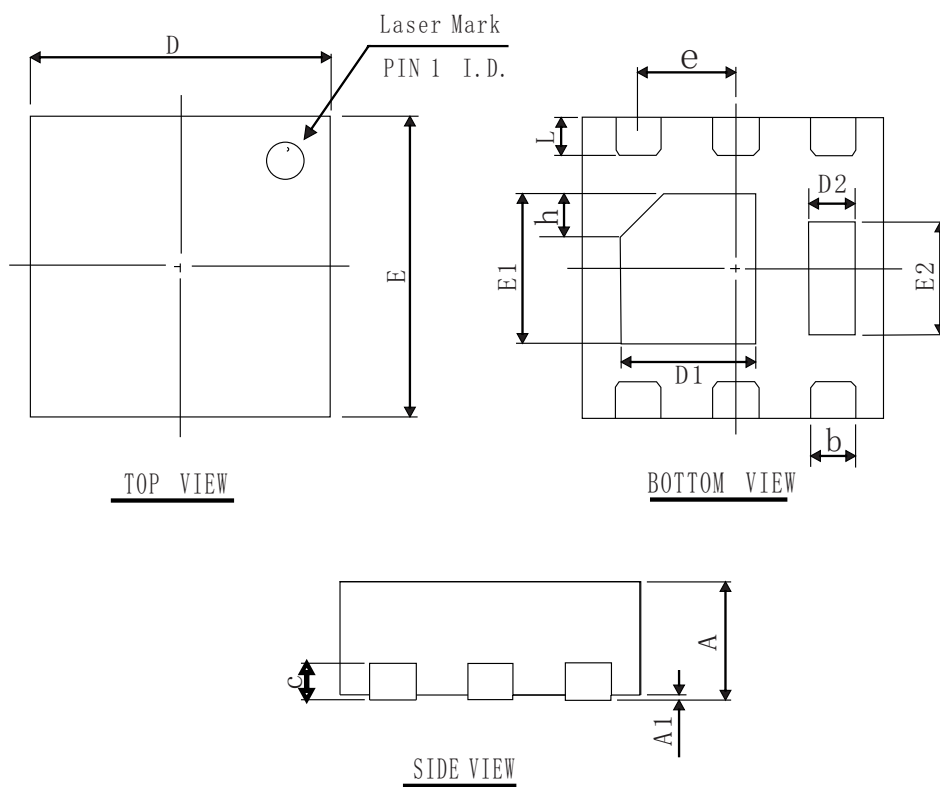


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

# DFN 2X2 PACKAGE OUTLINE



COMMON DIMENSIONS  
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	0.60	0.75	0.90
A1	0.00	0.02	0.10
b	0.15	0.25	0.40
D	1.80	2.00	2.25
E	1.80	2.00	2.25
D1	0.70	0.90	1.10
E1	0.75	1.00	1.20
D2	0.15	0.30	0.45
E2	0.45	0.75	0.95
L	0.15	0.25	0.40
h	0.15	0.25	0.40
c	0.203 REF		
e	0.65 BSC		

Other thickness dimensions are as follows

A	0.50	0.55	0.60
A	0.40	0.45	0.50

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