

N-Channel 100 V (D-S) Super Junction Power MOSFET

PRODUCT SUMMARY

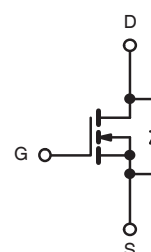
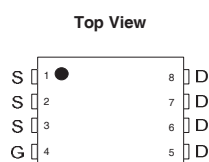
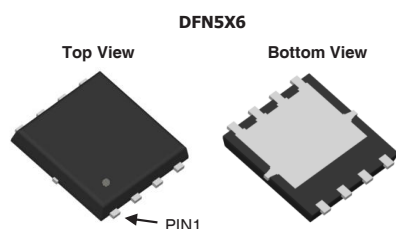
| V_{DS} (V) | $R_{DS(on)}$ (m Ω)(Typ.) | I_D (A) ^a | Q_g (Typ.) |
|--------------|----------------------------------|------------------------|--------------|
| 100 | 6 at $V_{GS} = 10$ V | 55 | 27 nC |
| | 10.5 at $V_{GS} = 4.5$ V | 40 | |

FEATURES

- TrenchFET II Power MOSFET
- 100 % Rg and UIS Tested

APPLICATIONS

- DC/DC Primary Side Switch
- Telecom/Server 48 V, Full/Half-Bridge DC/DC
- Industrial


RoHS
 COMPLIANT


N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|--|------------------------------------|----------------|----------------------|--------------------|
| Drain-Source Voltage | | V_{DS} | 100 | V |
| Gate-Source Voltage | | V_{GS} | ± 20 | |
| Continuous Drain Current ($T_J = 150\text{ }^{\circ}\text{C}$) | $T_C = 25\text{ }^{\circ}\text{C}$ | I_D | 55 | A |
| | $T_C = 70\text{ }^{\circ}\text{C}$ | | 38 | |
| | $T_A = 25\text{ }^{\circ}\text{C}$ | | 15.6 ^{b, c} | |
| | $T_A = 70\text{ }^{\circ}\text{C}$ | | 12.2 ^{b, c} | |
| Pulsed Drain Current ($t = 300\text{ }\mu\text{s}$) | | I_{DM} | 200 | |
| Continuous Source-Drain Diode Current | $T_C = 25\text{ }^{\circ}\text{C}$ | I_S | 55 | |
| | $T_A = 25\text{ }^{\circ}\text{C}$ | | 4.5 ^{b, c} | |
| Single Pulse Avalanche Current | $L = 0.1\text{ mH}$ | I_{AS} | 45 | |
| Single Pulse Avalanche Energy | | E_{AS} | 54 | mJ |
| Maximum Power Dissipation | $T_C = 25\text{ }^{\circ}\text{C}$ | P_D | 108 | W |
| | $T_C = 70\text{ }^{\circ}\text{C}$ | | 69 | |
| | $T_A = 25\text{ }^{\circ}\text{C}$ | | 5.5 ^{b, c} | |
| | $T_A = 70\text{ }^{\circ}\text{C}$ | | 3.5 ^{b, c} | |
| Operating Junction and Storage Temperature Range | | T_J, T_{stg} | - 55 to 150 | $^{\circ}\text{C}$ |
| Soldering Recommendations (Peak Temperature) ^{d, e} | | | 260 | |

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Typical | Maximum | Unit |
|---|------------|---------|---------|------|
| Maximum Junction-to-Ambient ^{b, f} | R_{thJA} | 20 | 25 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | 2.1 | 2.8 | |

Notes:

 a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

 c. $t = 10$ s.

d. The DFN5X6 is a leadless package. The end of the lead terminal is exposed copper

(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 70 °C/W.

| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|--------------------------------------|--|------|-------|-------|-------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} = 0, I _D = 250 μA | 100 | | | V |
| V _{DS} Temperature Coefficient | ΔV _{DS} /T _J | I _D = 250 μA | | 64 | | mV/°C |
| V _{GS(th)} Temperature Coefficient | ΔV _{GS(th)} /T _J | | | - 5.8 | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1.5 | | 3.5 | V |
| Gate-Source Leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 20 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 100 V, V _{GS} = 0 V | | | 1 | μA |
| | | V _{DS} = 64 V, V _{GS} = 0 V, T _J = 55 °C | | | 10 | |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} ≥ 5 V, V _{GS} = 10 V | 55 | | | A |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = 10 V, I _D = 15 A | | 6 | 7.5 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 10 A | | 10.5 | 15.9 | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 10 V, I _D = 15 A | | 65 | | S |
| Dynamic ^b | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz | | 1610 | | pF |
| Output Capacitance | C _{oss} | | | 359 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 40 | | |
| Total Gate Charge | Q _g | V _{DS} = 50 V, V _{GS} = 10 V, I _D = 10 A | | 27 | | nC |
| Gate-Source Charge | Q _{gs} | | | 4.3 | | |
| Gate-Drain Charge | Q _{gd} | | | 7.2 | | |
| Gate Resistance | R _g | f = 1 MHz | 0.2 | 1.05 | 2.1 | Ω |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 50 V, R _L = 5 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω | | 19 | | ns |
| Rise Time | t _r | | | 11 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 45 | | |
| Fall Time | t _f | | | 8 | | |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I _S | T _C = 25 °C | | | 55 | A |
| Pulse Diode Forward Current ^a | I _{SM} | | | | 200 | |
| Body Diode Voltage | V _{SD} | I _S = 1 A | | 0.7 | 1 | V |
| Body Diode Reverse Recovery Time | t _{rr} | I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C | | 56 | | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | | 38 | | nC |
| Reverse Recovery Fall Time | t _a | | | 22 | | ns |
| Reverse Recovery Rise Time | t _b | | | 15 | | |

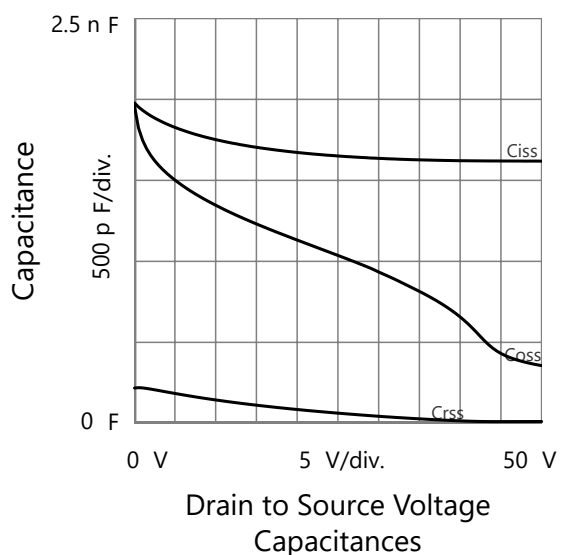
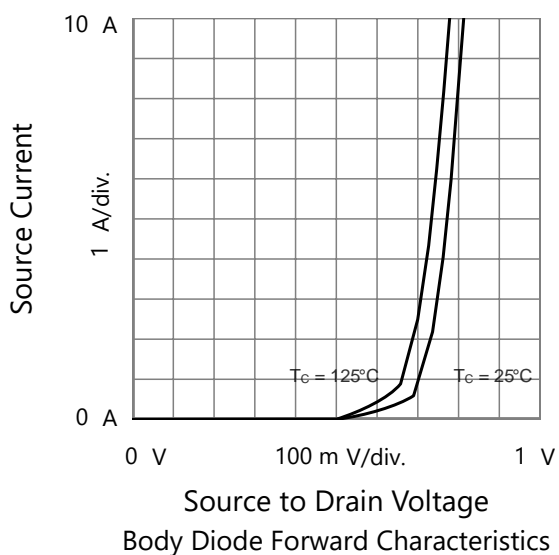
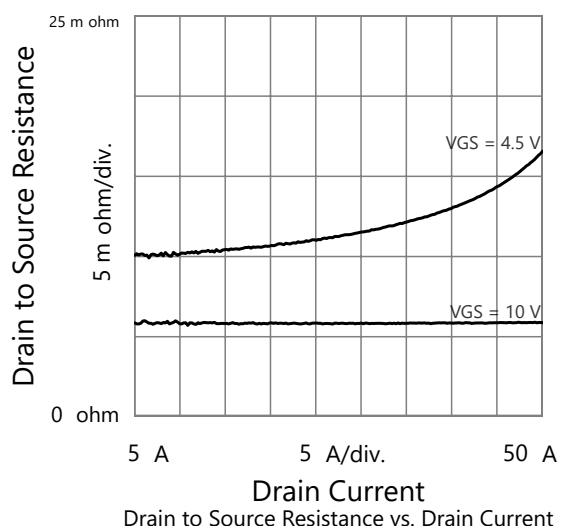
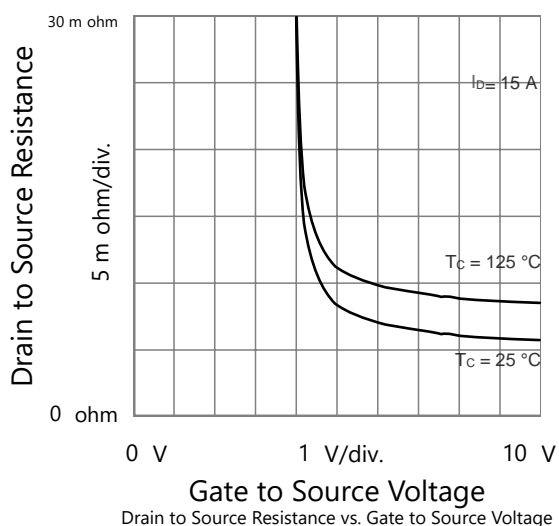
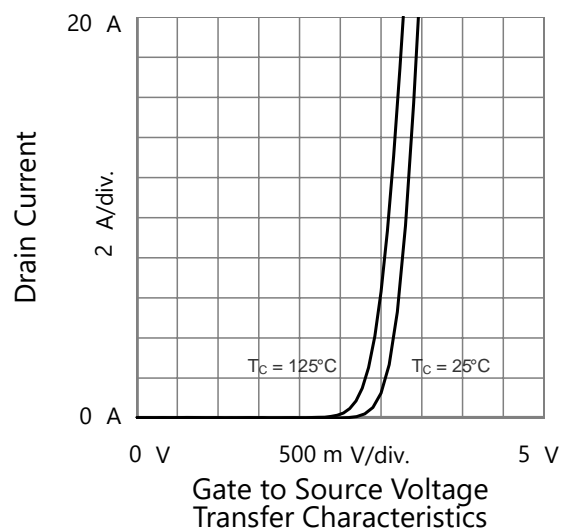
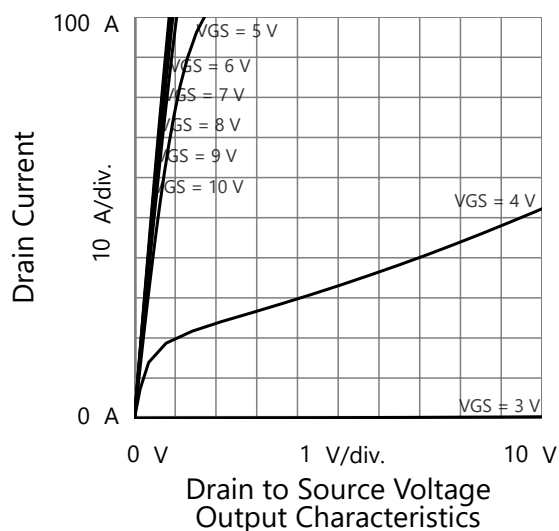
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

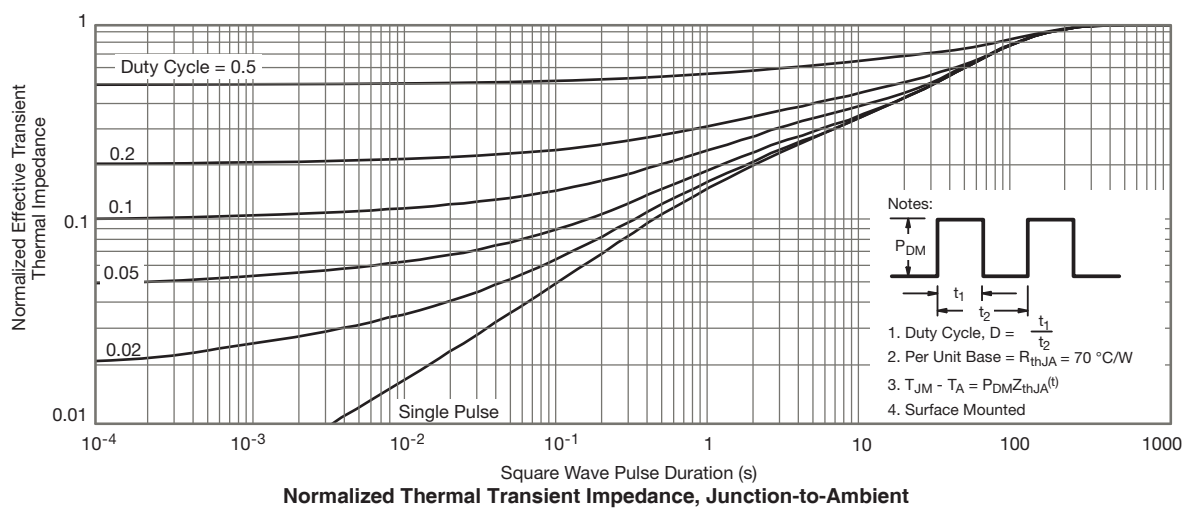
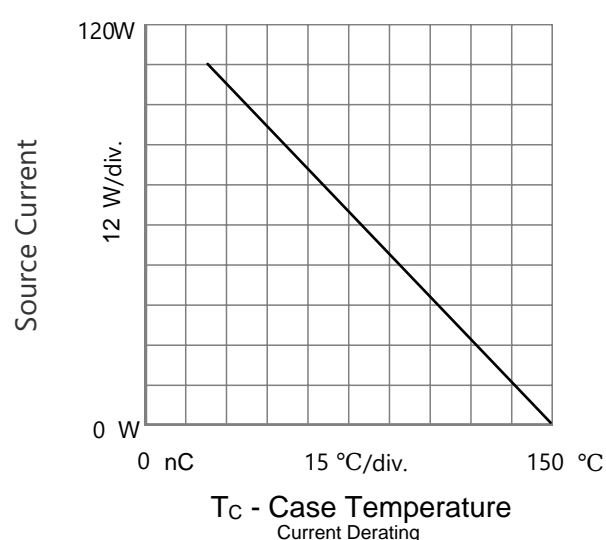
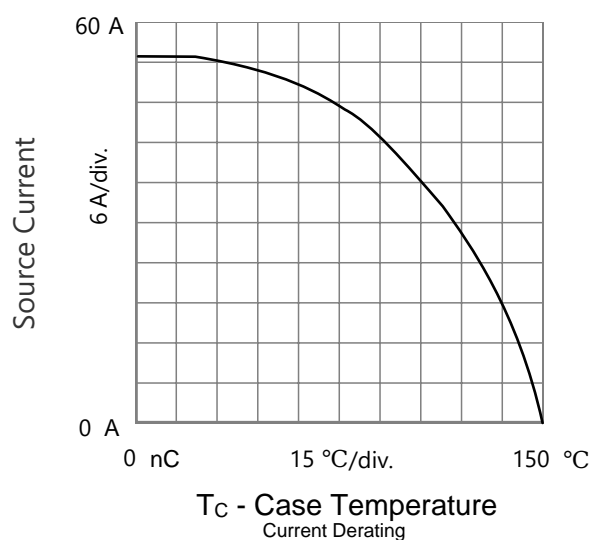
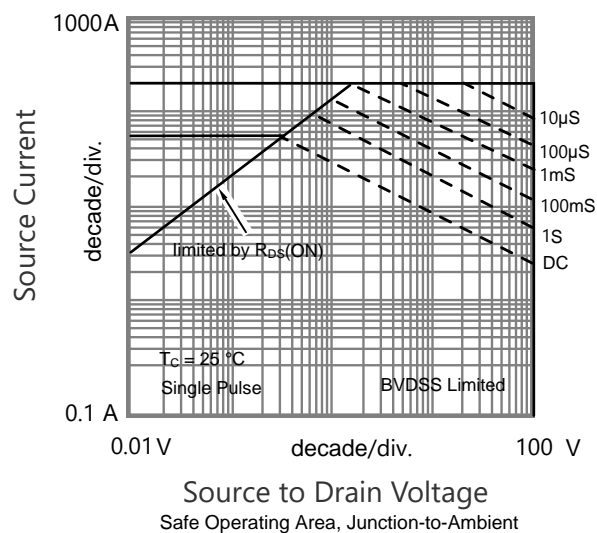
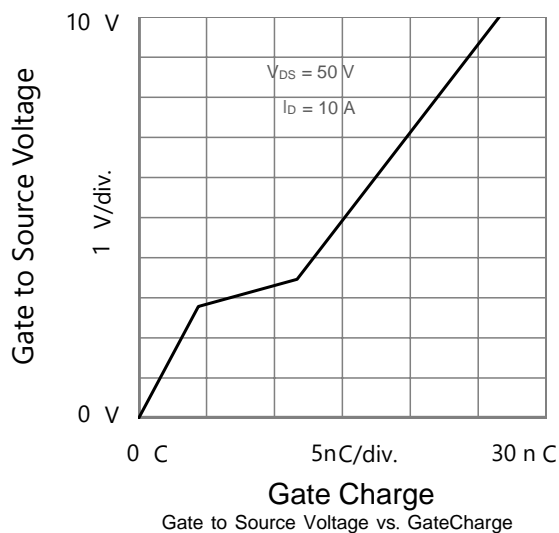
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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