N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a, e]	Q_g (Typ.)
20	0.0019 at V_{GS} = 4.5 V	147	61 nC
	0.0023 at V_{GS} = 2.5 V	110	

FEATURES

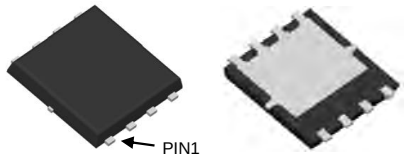
- TrenchFET® Power MOSFET
- 100 % R_g and UIS Tested

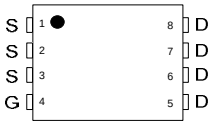
RoHS COMPLIANT

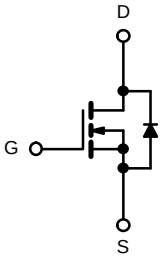
APPLICATIONS

- OR-ing
- Server

DFN5X6







N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	147[a, e]	A
	T_C = 70 °C		110[e]	
	T_A = 25 °C		52[b, c]	
	T_A = 70 °C		47.8[b, c]	
Pulsed Drain Current		I_{DM}	450	
Avalanche Current Pulse	L = 0.1 mH	I_{AS}	65	
Single Pulse Avalanche Energy		E_{AS}	120	mJ
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	87[a, e]	A
	T_A = 25 °C		3.02[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	247[a]	W
	T_C = 70 °C		169	
	T_A = 25 °C		3.72[b, c]	
	T_A = 70 °C		2.61[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, d]	t ≤ 10 s	R_{thJA}	12	19	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	1.1	1.8	

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under steady state conditions is 90 °C/W.
e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min .**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		35		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 7.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.8		2.5	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	90			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 32 A		0.0019	0.0021	Ω
		V_{GS} = 2.5 V, I_D = 29 A		0.0023	0.0025	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 32 A		100		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS}= 12.5 V, V_{GS} = 0 V, f = 1 MHz		4933		pF
Output Capacitance	C_{oss}			1991		
Reverse Transfer Capacitance	C_{rss}			983		
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 32 A		61		nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 29 A		80.3		
Gate-Source Charge	Q_{gs}			33		
Gate-Drain Charge	Q_{gd}			31		
Gate Resistance	R_g	f = 1 MHz		1.2		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 0.555 Ω $I_D \cong$ 27 A, V_{GEN} = 4.5 V, R_g = 1 Ω		19	30	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			75	111	
Fall Time	t_f			11	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 0.625 Ω $I_D \cong$ 24 A, V_{GEN} = 4.5 V, R_g = 1 Ω		56	85	
Rise Time	t_r			180	268	
Turn-Off Delay Time	$t_{d(off)}$			58	83	
Fall Time	t_f			14	21	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			147	A
Pulse Diode Forward Current[a]	I_{SM}				450	
Body Diode Voltage	V_{SD}	I_S = 22 A		0.7	1.0	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 20 A, di/dt = 100 A/µs, T_J = 25 °C		52	75	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70.2	102	nC
Reverse Recovery Fall Time	t_a			26		ns
Reverse Recovery Rise Time	t_b			24		

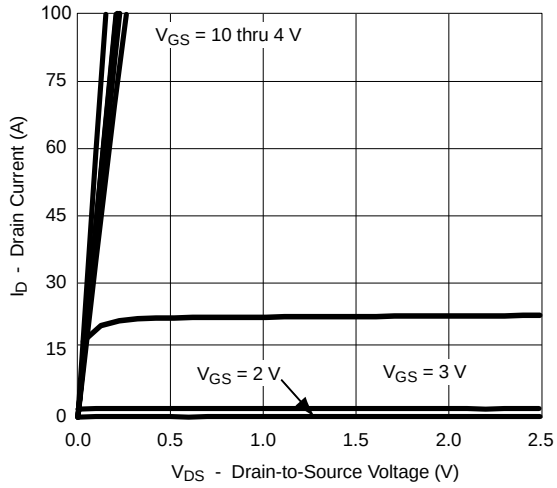
Notes:

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

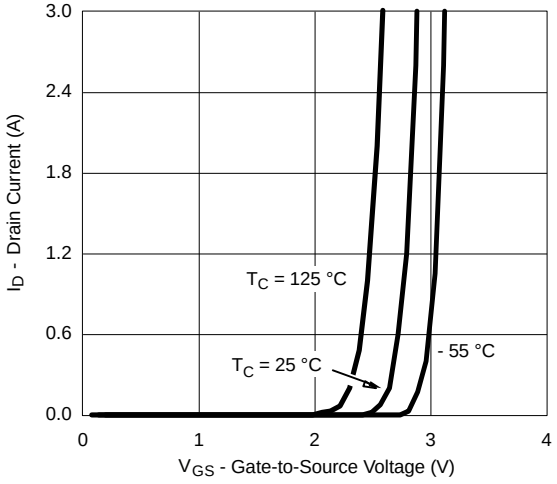
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

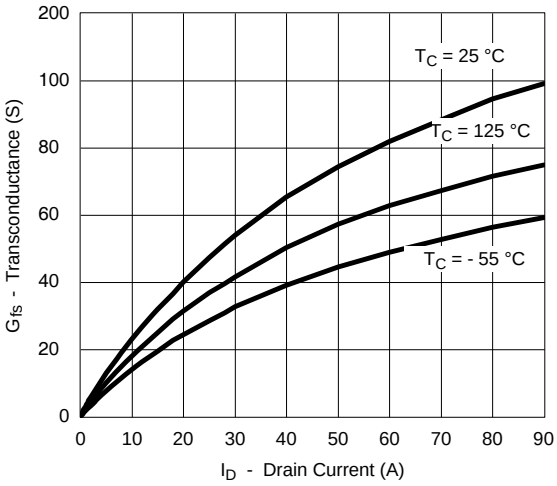
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



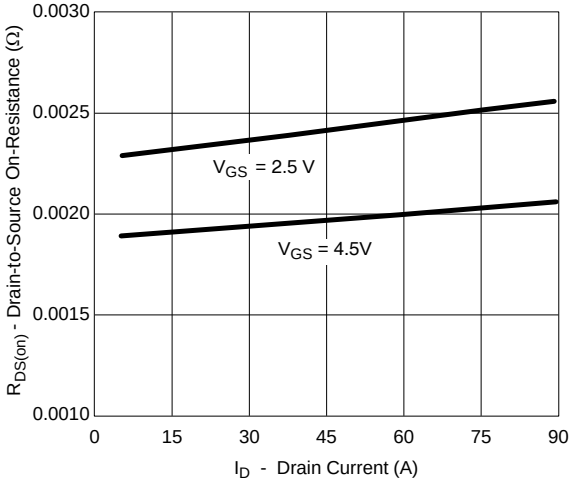
Output Characteristics



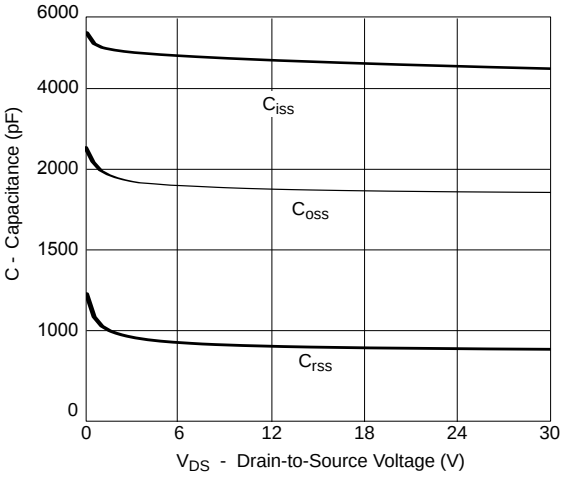
Transfer Characteristics



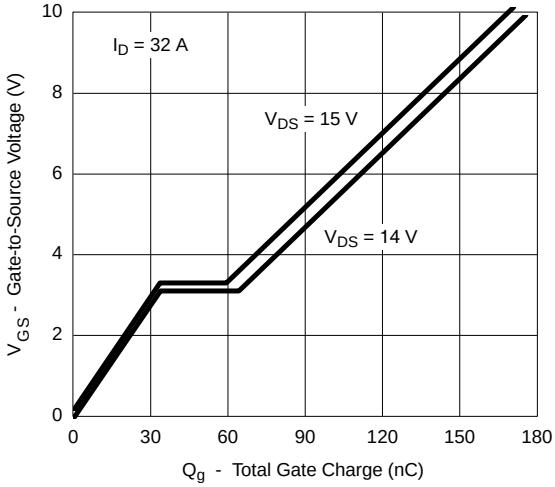
Transconductance



$R_{DS(on)}$ vs. Drain Current

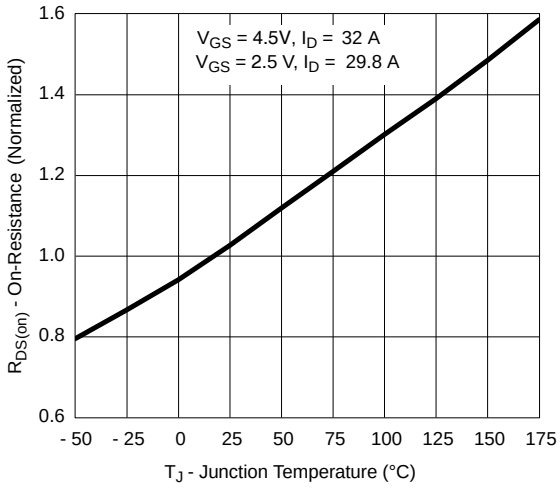


Capacitance

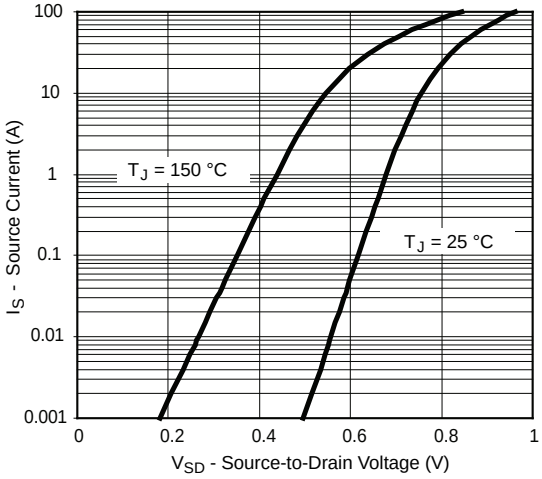


Gate Charge

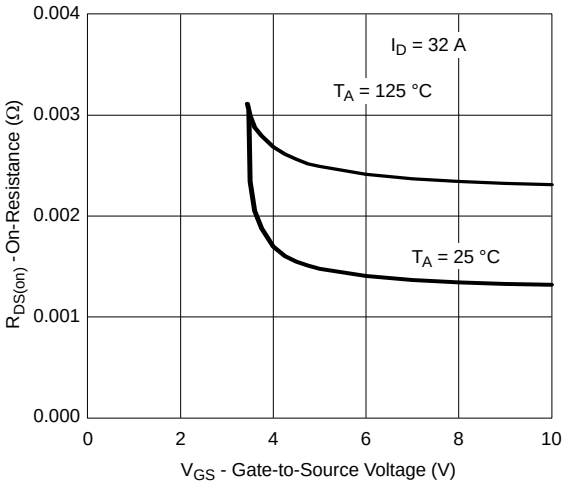
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



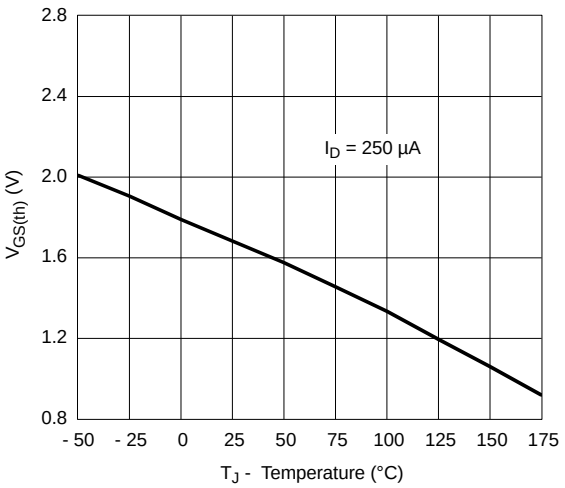
On-Resistance vs. Junction Temperature



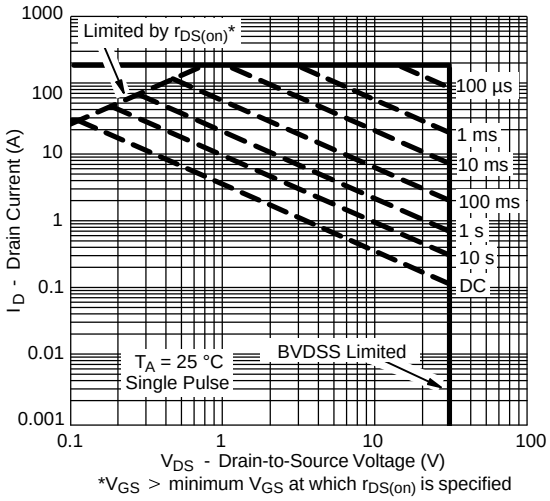
Forward Diode Voltage vs. Temperature



$R_{DS(on)}$ vs. V_{GS} vs. Temperature



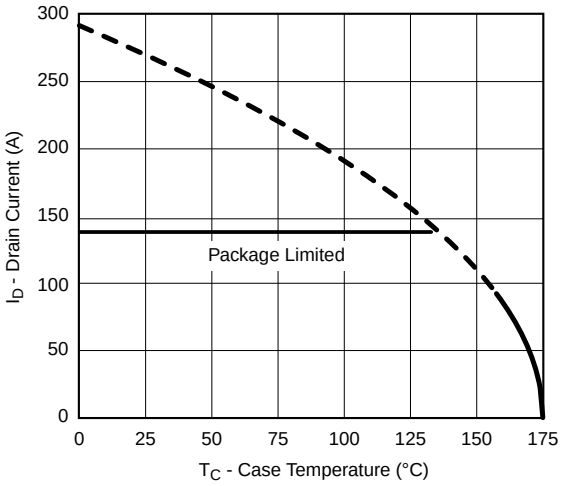
Threshold Voltage



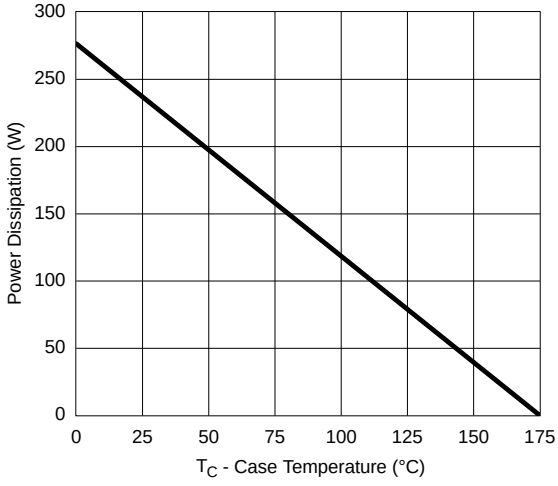
*V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

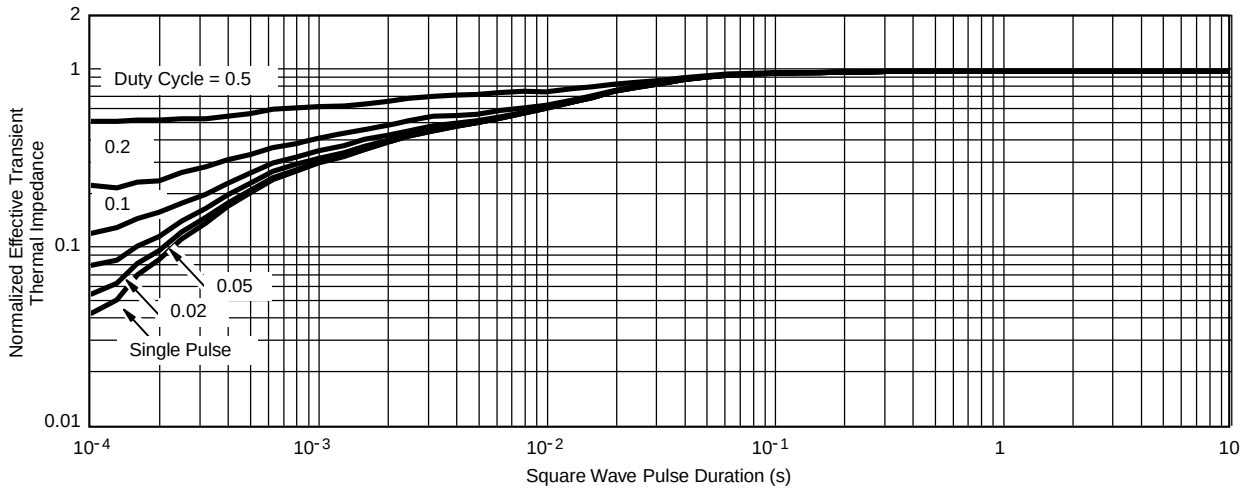


Current Derating*



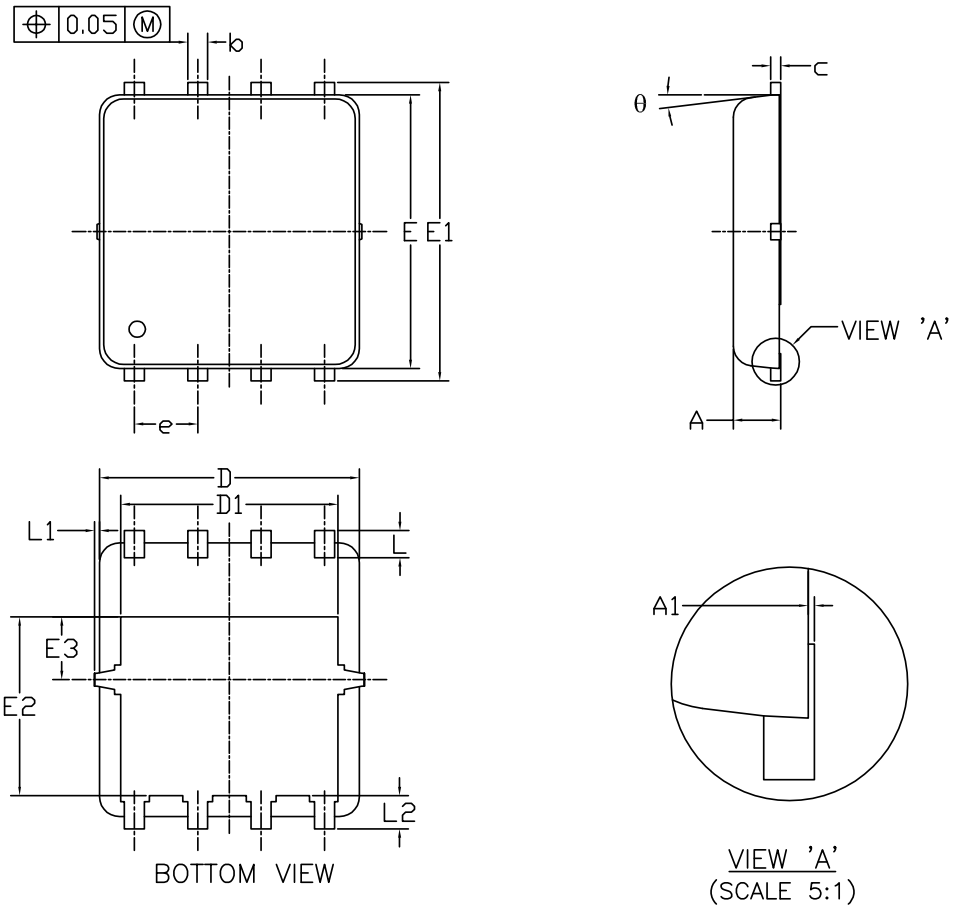
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

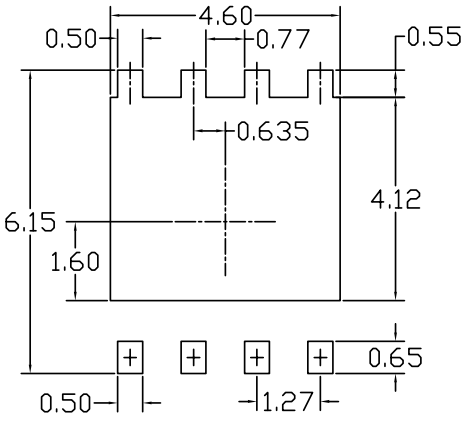


Normalized Thermal Transient Impedance, Junction-to-Case

DFN5x6_8L_EP1_P PACKAGE OUTLIN



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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