

N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (TYP.)
N-Channel	20	0.076 at V _{GS} = 4.5 V	2.7	0.55
		0.096 at V _{GS} = 2.7 V	2.5	
		0.128 at V _{GS} = 2.5 V	2.5	
P-Channel	-20	0.143 at V _{GS} = -4.5 V	-1.5	0.95
		0.182 at V _{GS} = -2.7 V	-1.5	
		0.230 at V _{GS} = -2.5 V	-1.3	

FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested

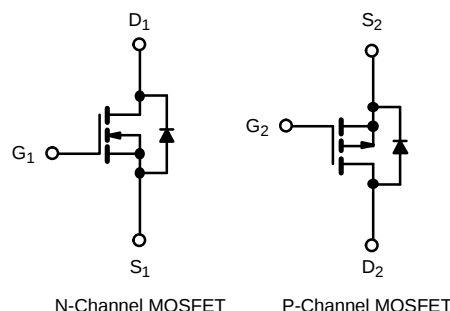
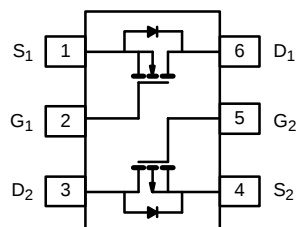
APPLICATIONS

- Load switch
- DC/DC converter



RoHS
COMPLIANT
HALOGEN
FREE

SOT-323-6



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-Source Voltage		V _{DS}	20	-20	V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	2.7	-1.5	A
	T _C = 70 °C		2.6	-1.4	
	T _A = 25 °C		2.7 ^{b, c}	-1.4 ^{b, c}	
	T _A = 70 °C		2.5 ^{b, c}	-1.4 ^{b, c}	
Source-Drain Current Diode Current	T _C = 25 °C	I _S	2.3	-1.3	
	T _A = 25 °C		2.2 ^{b, c}	-1.2 ^{b, c}	
Pulsed Drain Current (t = 300 μs)		I _{DM}	8	-5	
Maximum Power Dissipation	T _C = 25 °C	P _D	0.34	0.34	W
	T _C = 70 °C		0.22	0.22	
	T _A = 25 °C		0.29 ^{b, c}	0.29 ^{b, c}	
	T _A = 70 °C		0.18 ^{b, c}	0.18 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{std}	-55 to 150		°C

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	N-CHANNEL		P-CHANNEL		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	165	238	165	238	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	108	270	108	270	

Notes

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 186 °C/W (N-Channel) and 186 °C/W (P-Channel).

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP. ^a	MAX.	UNIT		
Static									
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	20	-	-	V		
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-20	-	-			
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch	-	24	-	mV/°C		
		I _D = -250 μA	P-Ch	-	-13	-			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch	-	-1.8	-			
		I _D = -250 μA	P-Ch	-	2.3	-			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.5	-	1.5	V		
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.3	-	-1.5			
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch	-	-	± 100	nA		
			P-Ch	-	-	± 100			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch	-	-	1	μA		
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch	-	-	-1			
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch	-	-	10			
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch	-	-	-10			
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 5 V	N-Ch	2	-	-	A		
		V _{DS} = -5 V, V _{GS} = -5 V	P-Ch	-1	-	-			
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 0.7 A	N-Ch	-	0.076	0.084	Ω		
		V _{GS} = -4.5 V, I _D = -0.4 A	P-Ch	-	0.143	0.157			
		V _{GS} = 2.7 V, I _D = 0.4 A	N-Ch	-	0.096	0.106			
		V _{GS} = -2.7 V, I _D = -0.2 A	P-Ch	-	0.182	0.201			
		V _{GS} = 2.5 V, I _D = 0.4 A	N-Ch	-	0.128	0.150			
		V _{GS} = -2.5V, I _D = -0.2 A	P-Ch	-	0.230	0.253			
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 0.7 A	N-Ch	-	1.5	-	S		
		V _{DS} = -15 V, I _D = -0.5 A	P-Ch	-	0.8	-			
Dynamic ^a									
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	-	221	-	pF		
Output Capacitance	C _{oss}		P-Ch	-	228	-			
			N-Ch	-	14	-			
Reverse Transfer Capacitance	C _{rss}		P-Ch	-	16	-			
		N-Ch	-	6	-				
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 0.7 A	N-Ch	-	1.2	1.8	nC		
			V _{DS} = -10 V, V _{GS} = -10 V, I _D = -0.5 A	P-Ch	-	1.9		3	
		N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V I _D = 0.5 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -0.4 A	N-Ch	-	0.55	1.1			
			P-Ch	-	0.95	1.5			
			Gate-Source Charge	Q _{gs}	N-Ch	-		0.15	-
					P-Ch	-		0.25	-
Gate-Drain Charge	Q _{gd}	N-Ch	-	0.15	-				
		P-Ch	-	0.25	-				
Gate Resistance	R _g	f = 1 MHz	N-Ch	1.5	7.2	14.4	Ω		
			P-Ch	2.1	10.3	20.6			

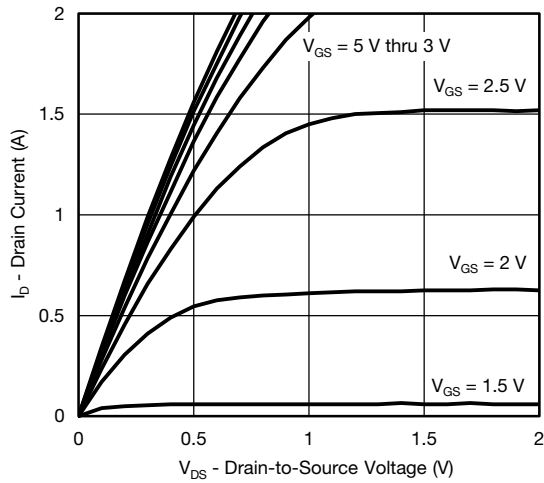
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP. ^a	MAX.	UNIT
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 20 Ω I _D ≡ 0.5 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch	-	2	4	ns
			P-Ch	-	2	4	
Rise Time	t _r		N-Ch	-	14	21	
			P-Ch	-	9	18	
Turn-Off Delay Time	t _{d(off)}	N-Ch	-	11	20		
		P-Ch	-	10	20		
Fall Time	t _f	N-Ch	-	7	14		
		P-Ch	-	7	14		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 20 Ω I _D ≡ 0.5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch	-	16	24	
			P-Ch	-	15	23	
Rise Time	t _r		N-Ch	-	22	33	
			P-Ch	-	15	23	
Turn-Off Delay Time	t _{d(off)}	N-Ch	-	22	33		
		P-Ch	-	12	20		
Fall Time	t _f	N-Ch	-	13	20		
		P-Ch	-	8	16		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch	-	-	2.7	A
			P-Ch	-	-	-1.5	
Pulse Diode Forward Current ^a	I _{SM}		N-Ch	-	-	8	
			P-Ch	-	-	-5	
Body Diode Voltage	V _{SD}	I _S = 0.5 A	N-Ch	-	0.8	1.2	V
		I _S = -0.4 A	P-Ch	-	-0.8	-1.2	
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 0.5 A, di/dt = 100 A/μs, T _J = 25 °C	N-Ch	-	8	15	ns
			P-Ch	-	12	20	
Body Diode Reverse Recovery Charge	Q _{rr}		N-Ch	-	1	2	nC
			P-Ch	-	5	10	
Reverse Recovery Fall Time	t _a	P-Channel I _F = -0.4 A, di/dt = -100 A/μs, T _J = 25 °C	N-Ch	-	4	-	ns
			P-Ch	-	9	-	
Reverse Recovery Rise Time	t _b		N-Ch	-	4	-	
			P-Ch	-	3	-	

Notes

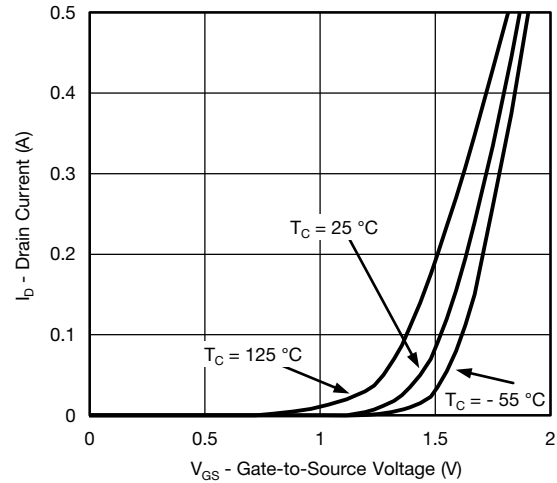
- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\text{ }\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

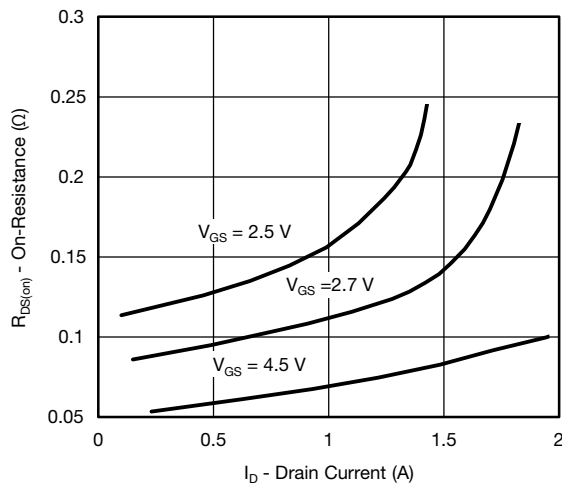
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



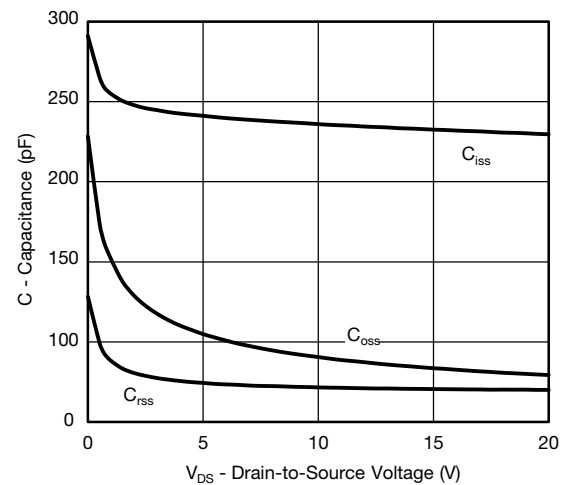
Output Characteristics



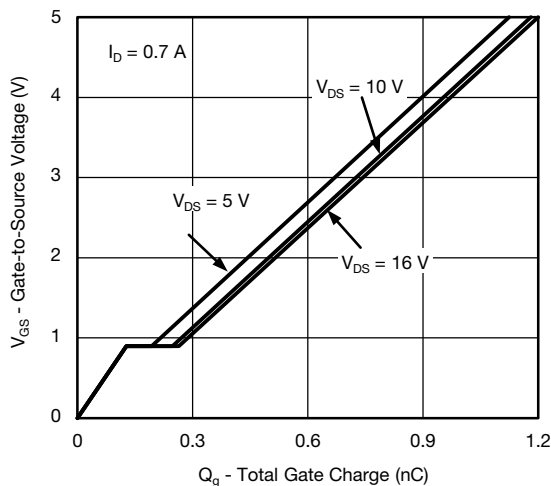
Transfer Characteristics



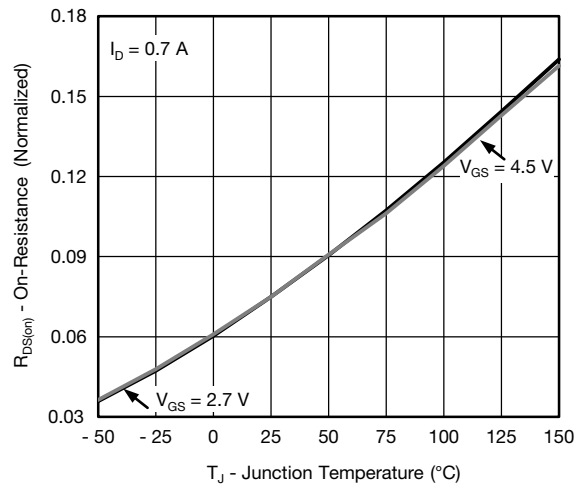
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

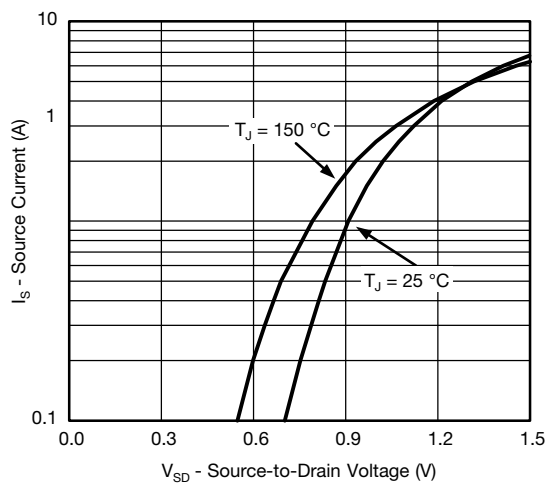


Gate Charge

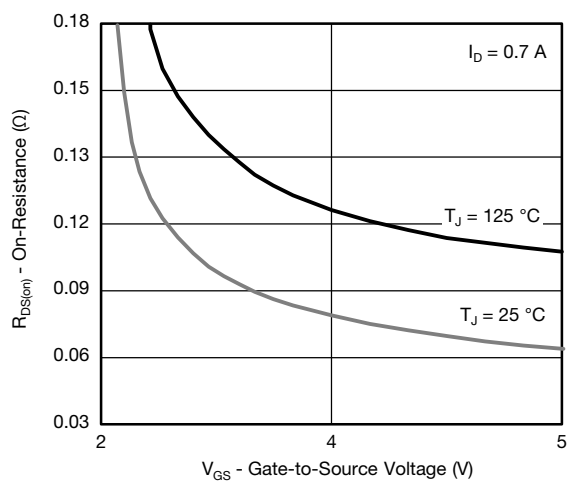


On-Resistance vs. Junction Temperature

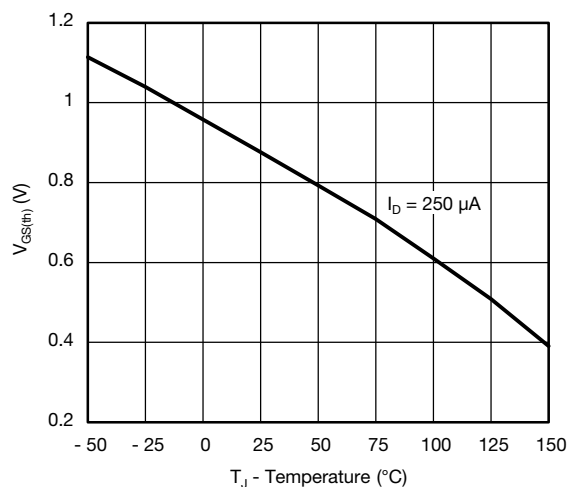
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



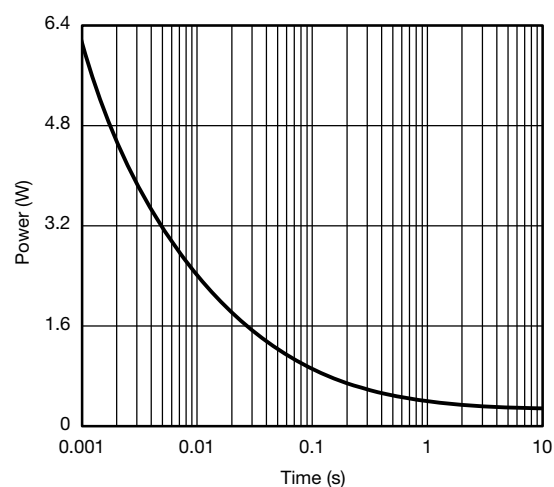
Source-Drain Diode Forward Voltage



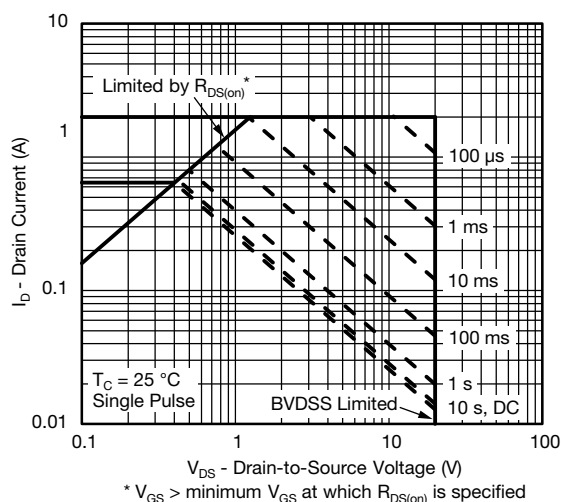
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

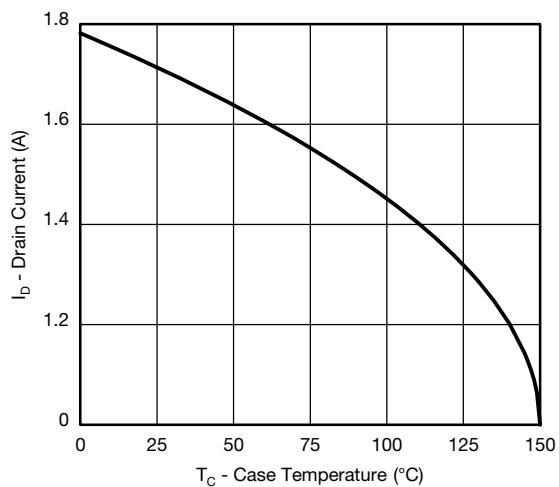


Single Pulse Power, Junction-to-Ambient

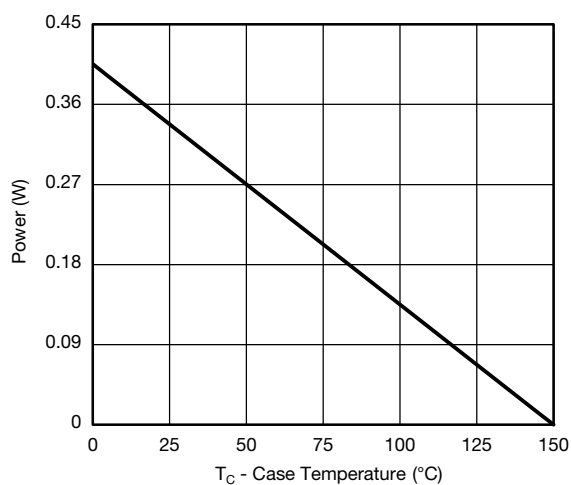


Safe Operating Area, Junction-to-Ambient

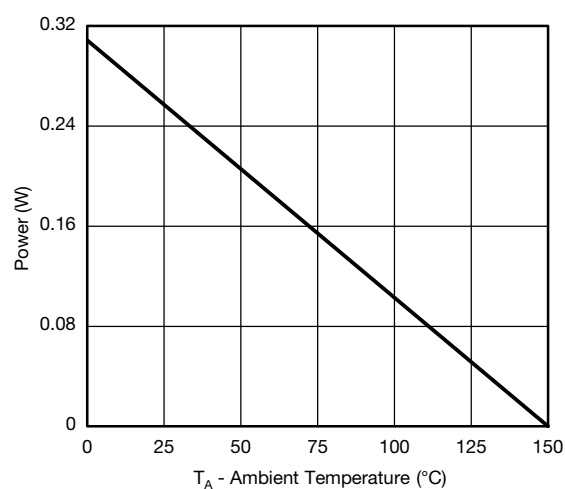
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



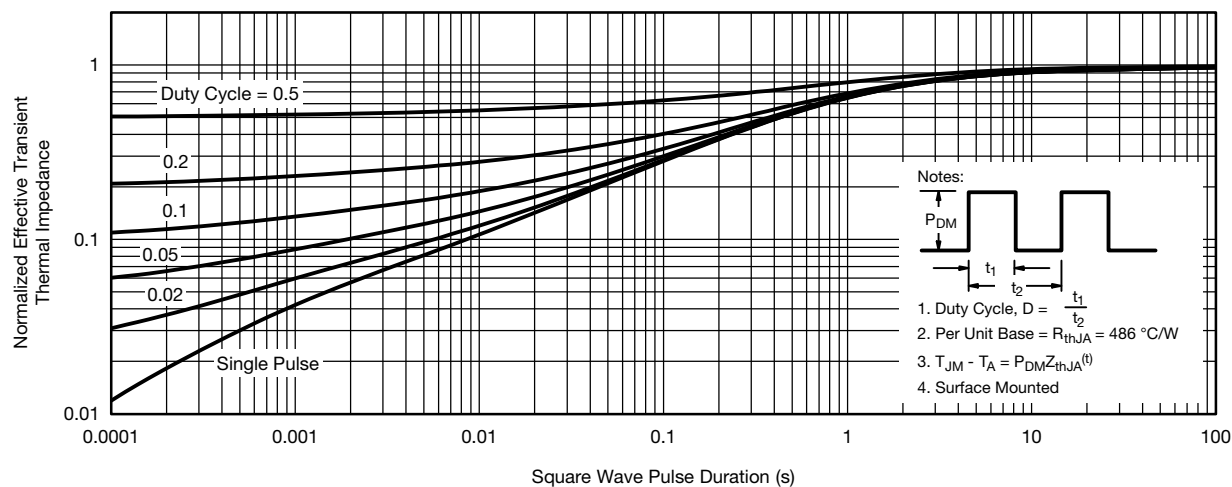
Power Derating, Junction-to-Foot



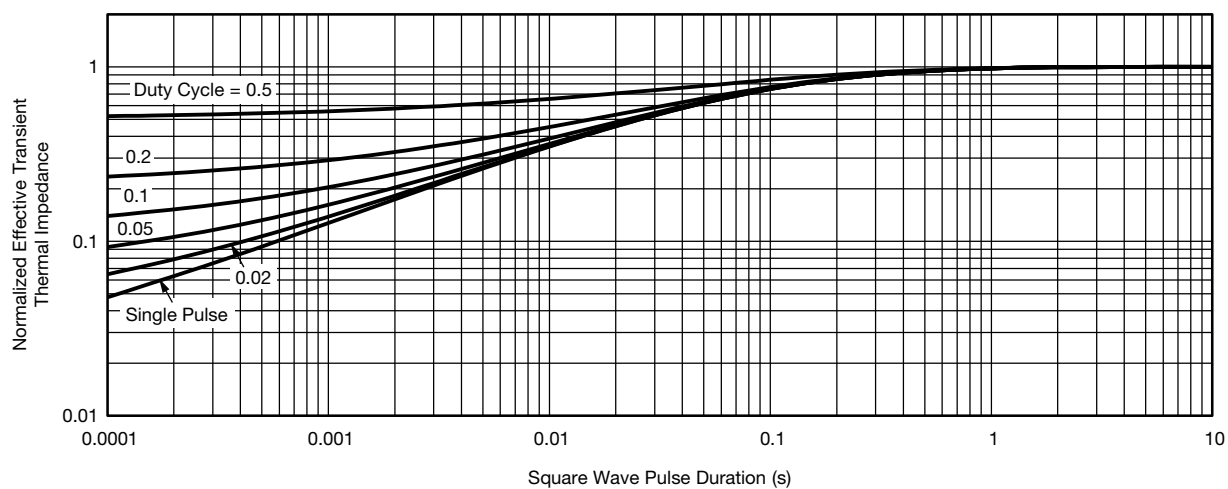
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

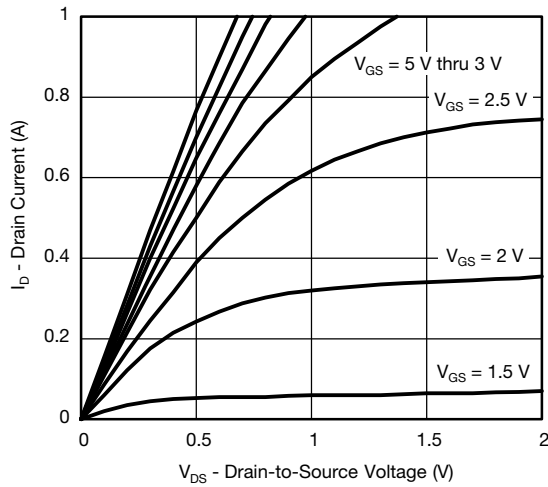


Normalized Thermal Transient Impedance, Junction-to-Ambient

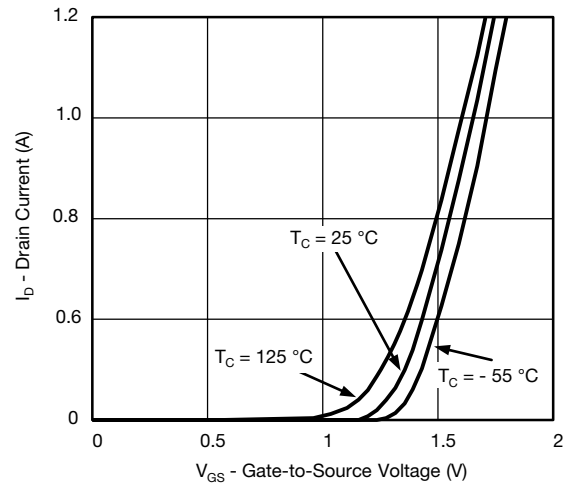


Normalized Thermal Transient Impedance, Junction-to-Foot

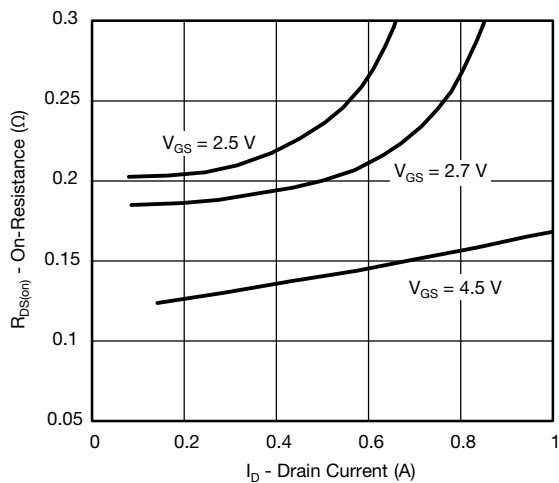
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



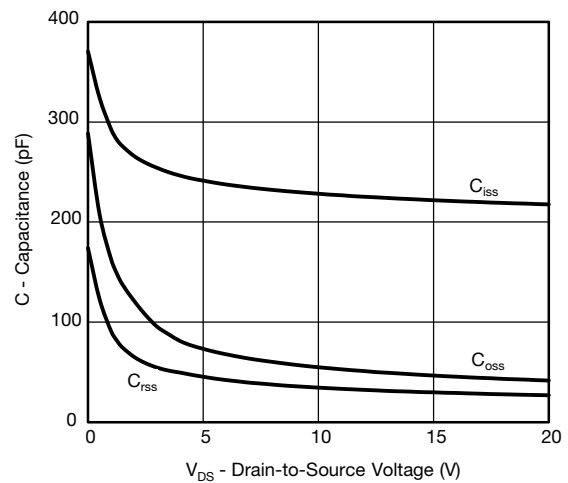
Output Characteristics



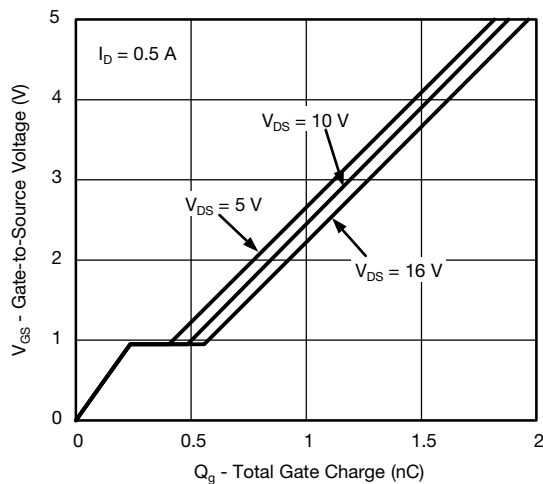
Transfer Characteristics



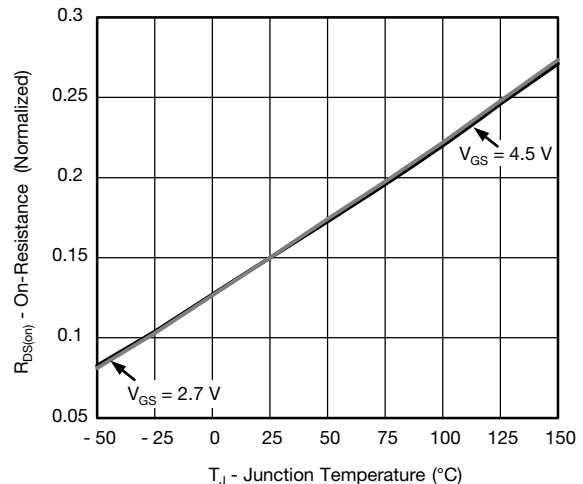
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

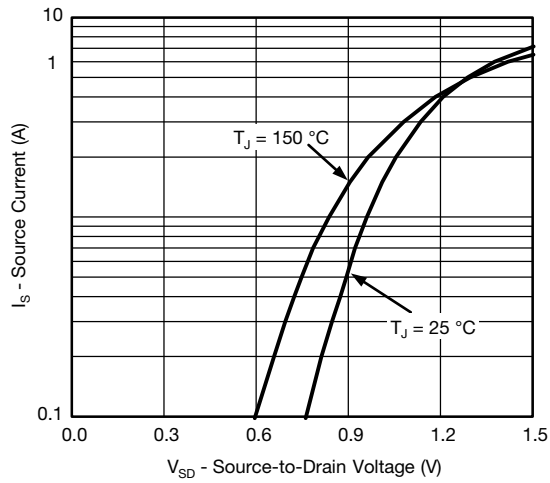


Gate Charge

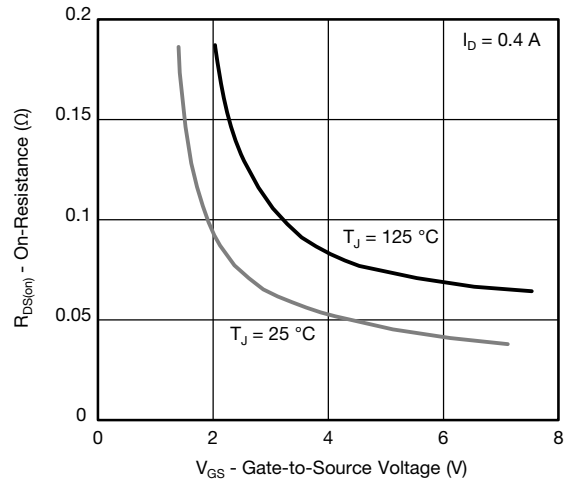


On-Resistance vs. Junction Temperature

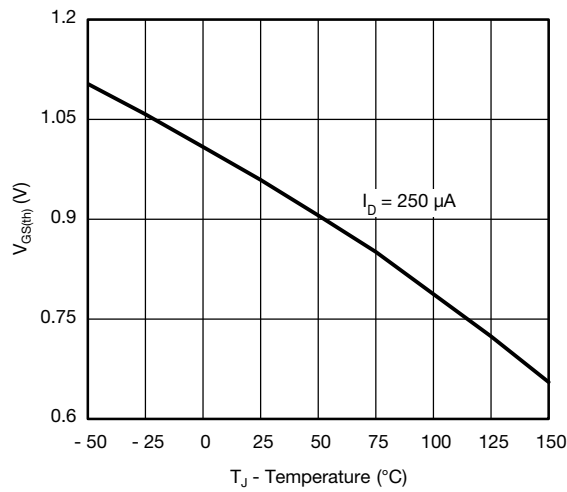
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



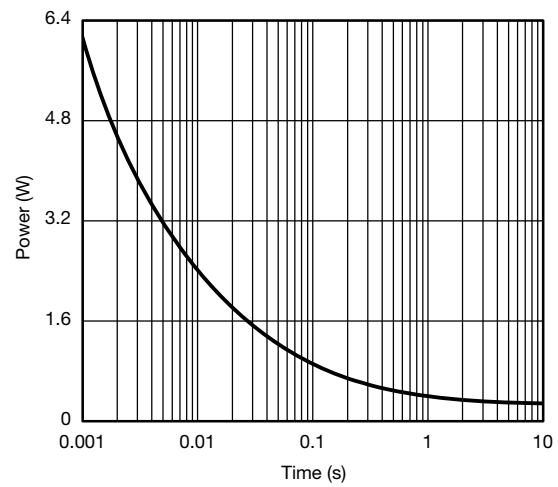
Source-Drain Diode Forward Voltage



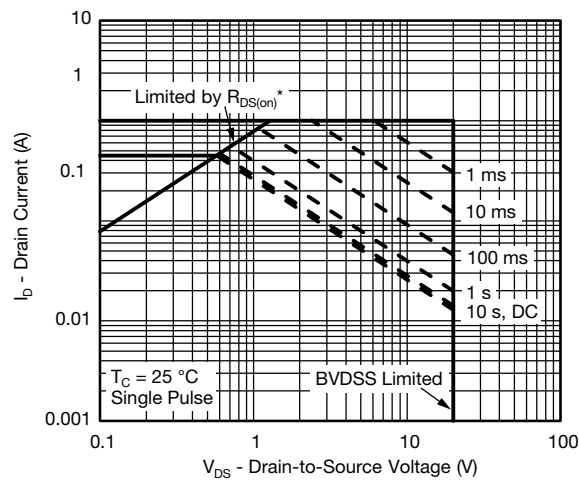
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

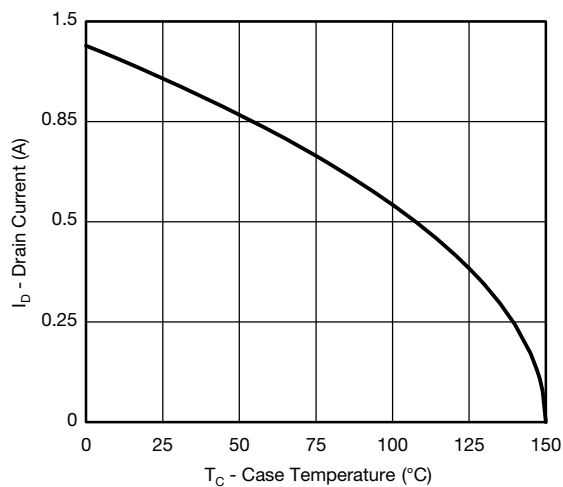


Single Pulse Power, Junction-to-Ambient

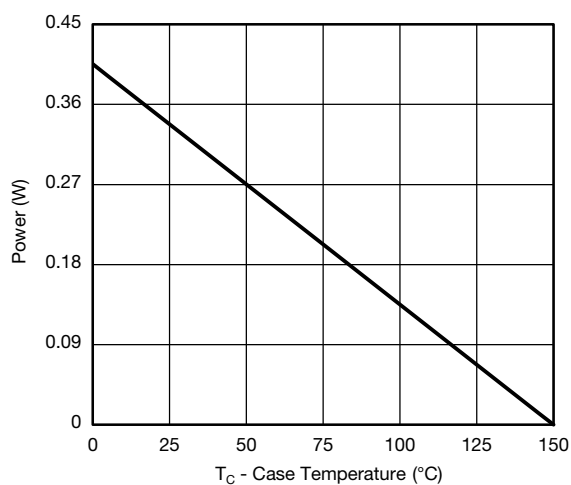


Safe Operating Area, Junction-to-Ambient

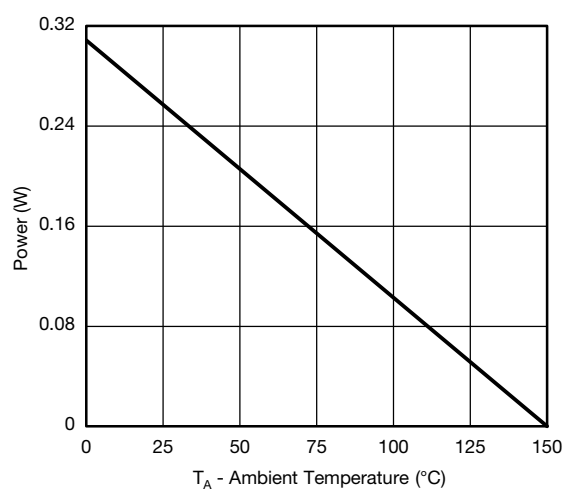
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



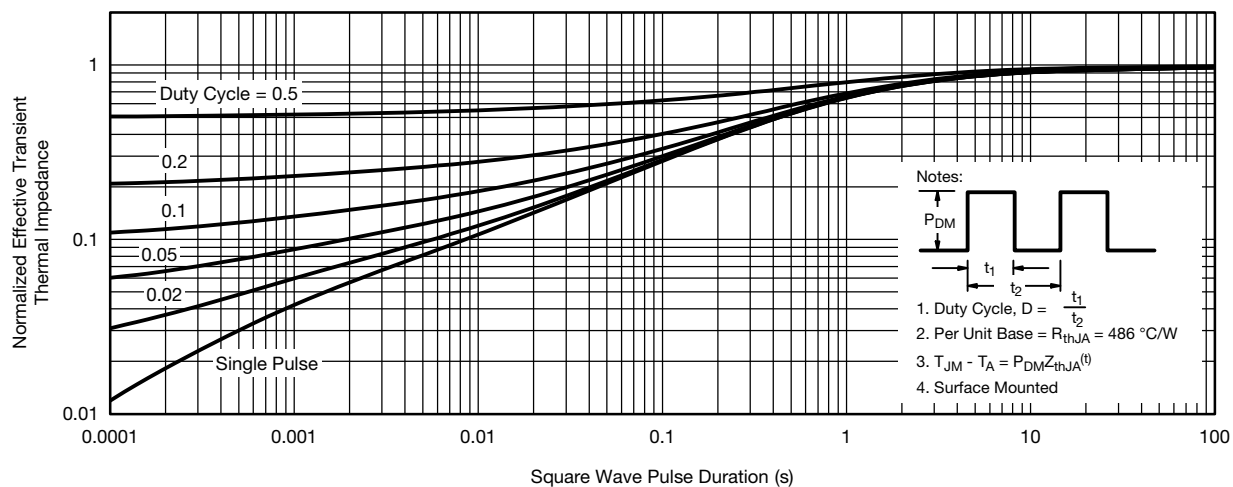
Power Derating, Junction-to-Foot



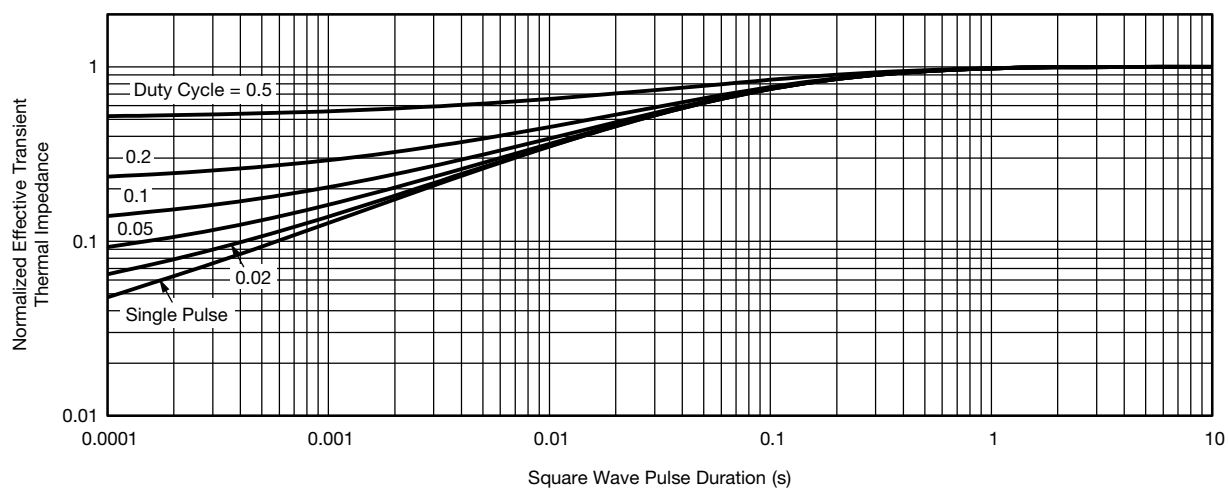
Power Derating, Junction-to-Ambient

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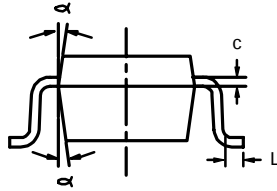
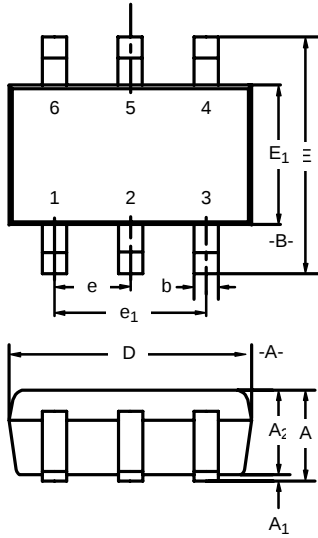
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

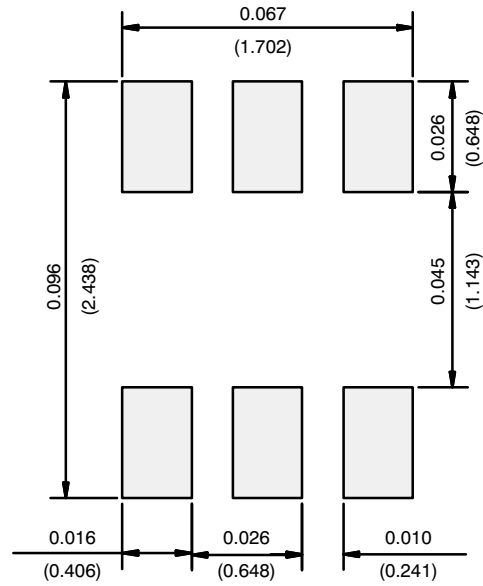


Normalized Thermal Transient Impedance, Junction-to-Foot



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	—	1.10	0.035	—	0.043
A ₁	—	—	0.10	—	—	0.004
A ₂	0.80	—	1.00	0.031	—	0.039
b	0.15	—	0.30	0.006	—	0.012
c	0.10	—	0.25	0.004	—	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

RECOMMENDED MINIMUM PADS FOR SOT323: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

Disclaimer

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Din-Tek Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Din-Tek documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Din-Tek Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Din-Tek documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.