# N-Channel 60-V (D-S) MOSFET

## PRODUCT SUMMARY

| $V_{DS}$ (V) | $R_{DS(on)}$ ($\Omega$) | $I_D$ (mA) |
|---|---|---|
| 60 | 2.5 at $V_{GS}$ = 10 V | 200 |

**SOT-523**



Top View
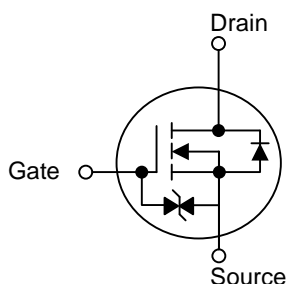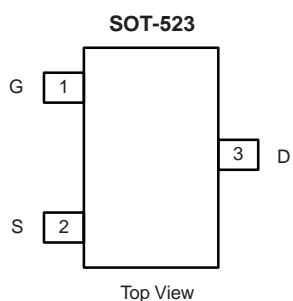


## FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Low On-Resistance: 2.5 $\Omega$
- Low Threshold: 2 V (typ.)
- Low Input Capacitance: 25 pF
- Fast Switching Speed: 25 ns
- Low Input and Output Leakage
- TrenchFET II Power MOSFET
- 1200V ESD Protection

## BENEFITS

- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

## APPLICATIONS

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

## ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted

| Parameter | | Symbol | Limit | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current ($T_J$ = 150 °C)[b] | $T_A$ = 25 °C | $I_D$ | 200 | mA |
| | $T_A$ = 100 °C | | 150 | |
| Pulsed Drain Current[a] | | $I_{DM}$ | 700 | |
| Power Dissipation[b] | $T_A$ = 25 °C | $P_D$ | 0.15 | W |
| | $T_A$ = 100 °C | | 0.07 | |
| Maximum Junction-to-Ambient[b] | | $R_{thJA}$ | 390 | °C/W |
| Operating Junction and Storage Temperature Range | | $T_J, T_{stg}$ | - 55 to 150 | °C |

Notes:
a. Pulse width limited by maximum junction temperature.
b. Surface Mounted on FR4 board.

## SPECIFICATIONS $T_A$ = 25 °C, unless otherwise noted

| Parameter | Symbol | Test Conditions | Min. | Typ.[a] | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 10 μA | 60 | | | V |
| Gate-Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | | 2.5 | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ± 10 | μA |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = ± 15 V | | | 1 | |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = ± 10 V | | | ± 150 | nA |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = ± 10 V, $T_J$ = 85 °C | | | ± 1000 | |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = ± 5 V | | | ± 100 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | | | 1 | μA |
| | | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V , $T_J$ = 125 °C | | | 500 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 7.5 V | 700 | | | mA |
| | | $V_{GS}$ = 4.5 V, $V_{DS}$ = 10 V | 300 | | | |
| Drain-Source On-Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 100 mA | | | 2.5 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 100 mA | | | 4 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 100 mA | 100 | | | mS |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = 100 mA, $V_{GS}$ = 0 V | | | 1.3 | V |
| **Dynamic[a]** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V $I_D \cong$ 100 mA | | 0.4 | 0.6 | nC |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V f = 1 MHz | | 30 | | pF |
| Output Capacitance | $C_{oss}$ | | | 6 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 2.5 | | |
| **Switching[a, b, c]** | | | | | | |
| Turn-On Time | $t_{d(on)}$ | $V_{DD}$ = 30 V, $R_L$ = 150 Ω $I_D \cong$ 100 mA, $V_{GEN}$ = 10 V, $R_G$ = 10 Ω | | | 25 | ns |
| Turn-Off Time | $t_{d(off)}$ | | | | 35 | |

Notes:
a. For DESIGN AID ONLY, not subject to production testing.
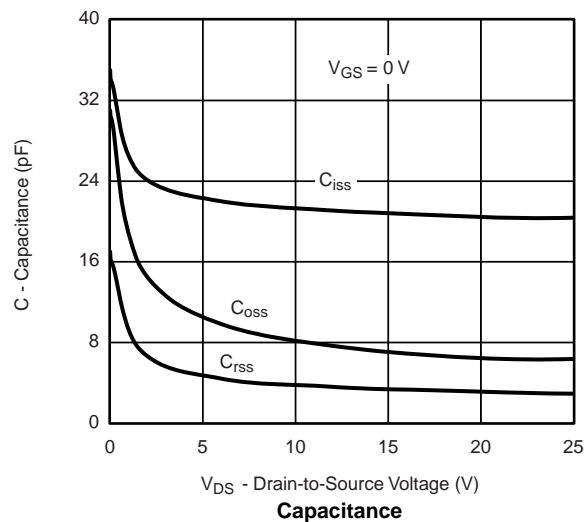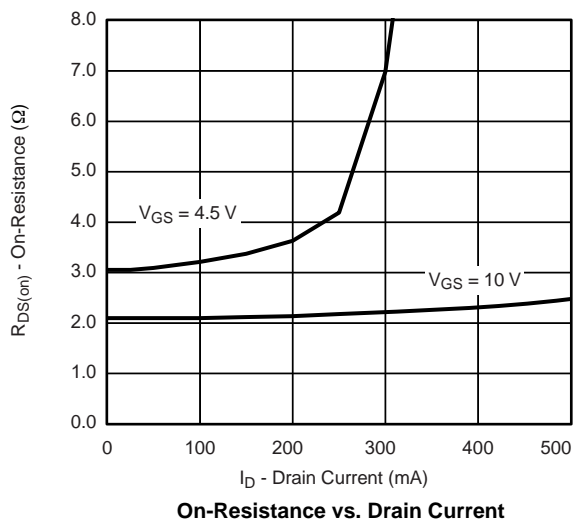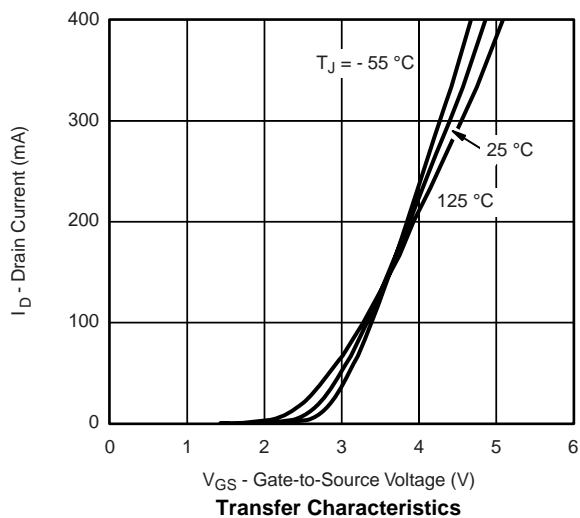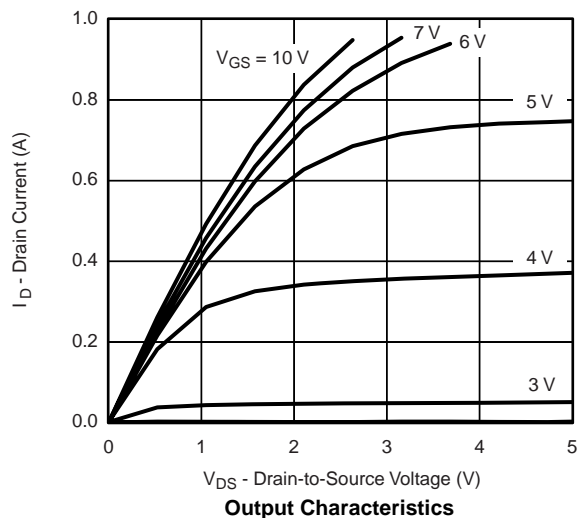b. Pulse test: PW ≤ 300 μs duty cycle ≤ 2 %.
c. Switching time is essentially independent of operating temperature.

**Din-Tek**
SEMICONDUCTOR

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

![Din-Tek SEMICONDUCTOR logo]

## TYPICAL CHARACTERISTICS  25 °C, unless otherwise noted



$V_{GS} = 0$ V

$T_J = 125$ °C

$T_J = 25$ °C

$T_J = -55$ °C

$I_S$ - Source Current (mA)

$V_{SD}$ - Source-to-Drain Voltage (V)

**Source-Drain Diode Forward Voltage**



$I_D = 200$ mA   $I_D = 500$ mA

$R_{DS(on)}$ - On-Resistance (Ω)

$V_{GS}$ - Gate-to-Source Voltage (V)
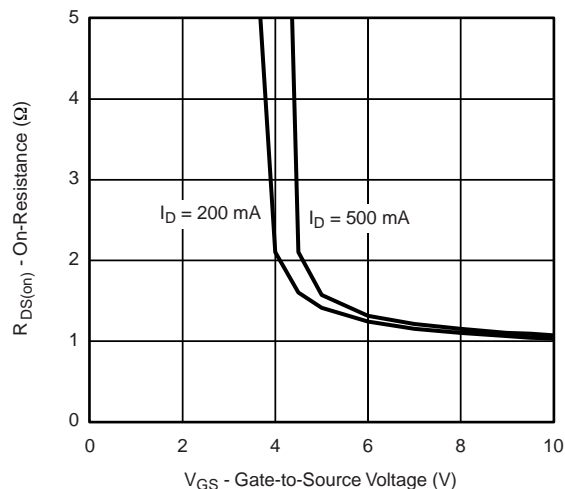
**On-Resistance vs. Gate-Source Voltage**



$I_D = 250$ µA

$V_{GS(th)}$ Variance (V)

$T_J$ - Junction Temperature (°C)
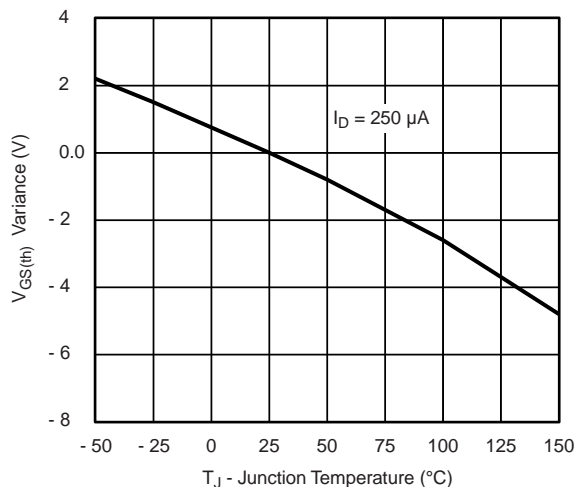
**Threshold Voltage Variance Over Temperature**



$T_A = 25$ °C

Power (W)

Time (s)
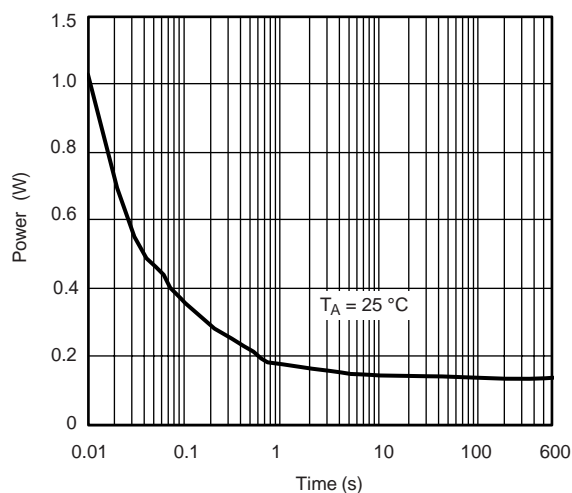
**Single Pulse Power, Junction-to-Ambient**



Duty Cycle = 0.5

0.2

0.1

0.05

0.02

Single Pulse

Normalized Effective Transient Thermal Impedance

Square Wave Pulse Duration (s)

Notes:

$P_{DM}$

$t_1$

$t_2$

1. Duty Cycle, D = $\dfrac{t_1}{t_2}$
2. Per Unit Base = $R_{thJA}$ = 350 °C/W
3. $T_{JM} - T_A = P_{DM}Z_{thJA}{}^{(t)}$
4. Surface Mounted

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

![Din-Tek SEMICONDUCTOR]
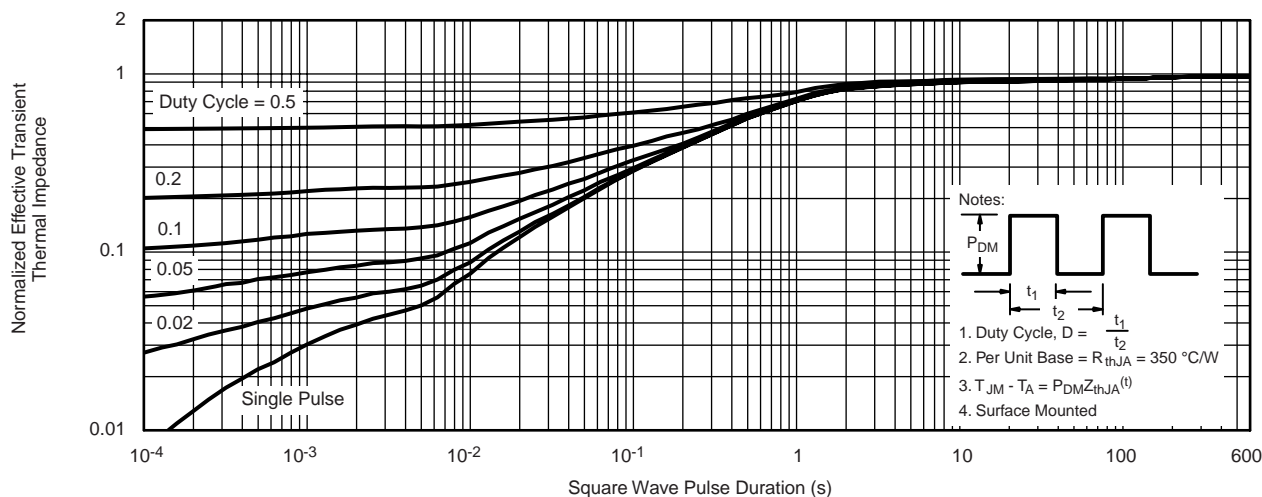
**THERMAL RATINGS** ($T_A$ = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot
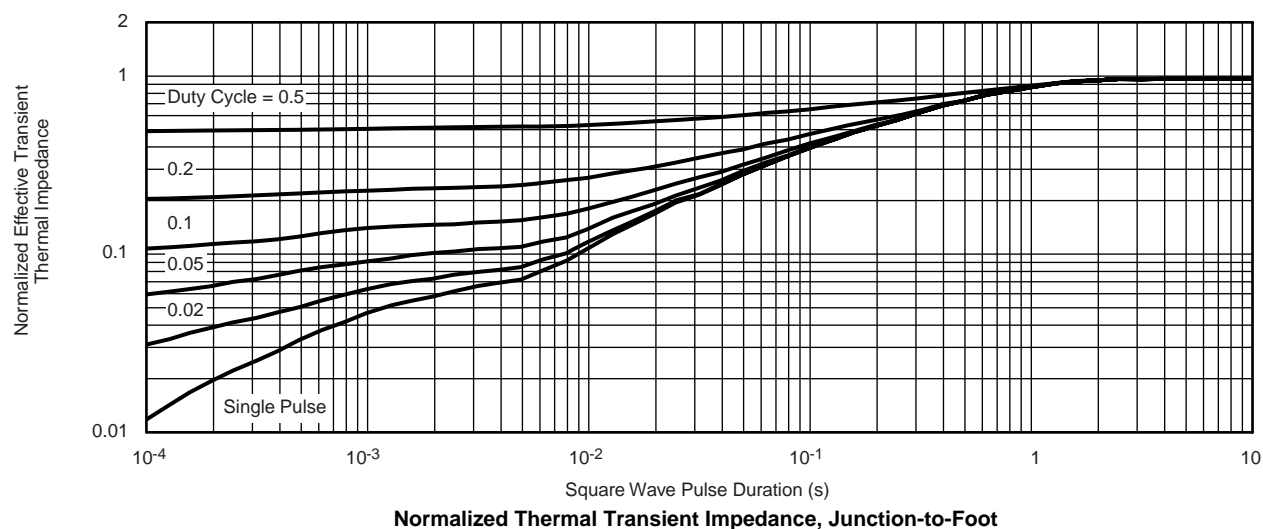
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 ℃)

  are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

# SOT-523: 3 Leads
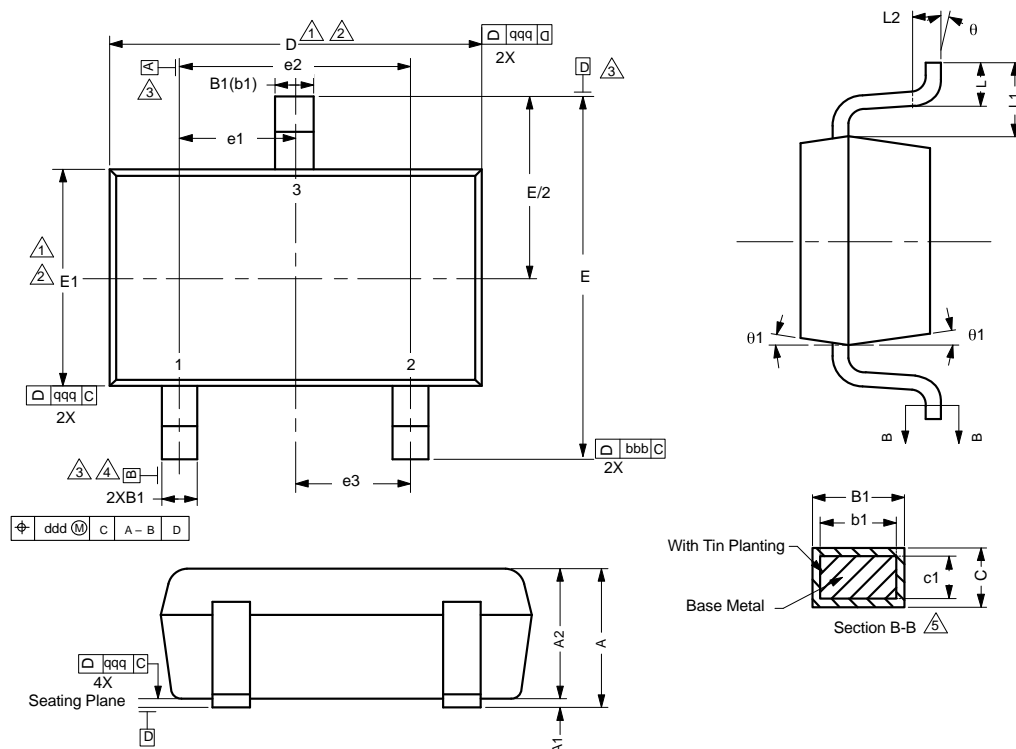


## Notes

Dimensions in millimeters will govern.

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.

2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interelead flash, but including any mismatch between the top and bottom of the plastic body.

3. Datums A, B and D to be determined 0.10 mm from the lead tip.

4. Terminal positions are shown for reference only.

5. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

| DIMENSIONS | TOLERANCES |
|---|---|
| aaa | 0.10 |
| bbb | 0.10 |
| ccc | 0.10 |
| ddd | 0.10 |

| DIM. | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | - | - | 0.80 | |
| $A_1$ | 0.00 | - | 0.10 | |
| $A_2$ | 0.65 | 0.70 | 0.80 | |
| $B_1$ | 0.19 | - | 0.24 | 5 |
| $b_1$ | 0.17 | - | 0.21 | |
| c | 0.13 | - | 0.15 | 5 |
| $c_1$ | 0.10 | - | 0.12 | 5 |
| D | 1.48 | 1.575 | 1.68 | 1, 2 |
| E | 1.50 | 1.60 | 1.70 | |
| $E_1$ | 0.66 | 0.76 | 0.86 | 1, 2 |
| $e_1$ | 0.50 BSC | | | |
| $e_2$ | 1.00 BSC | | | |
| $e_3$ | 0.50 BSC | | | |
| L | 0.15 | 0.205 | 0.30 | |
| $L_1$ | 0.40 ref. | | | |
| $L_2$ | 0.15 BSC | | | |
| θ | 0° | - | 8° | |
| $θ_1$ | 4° | - | 10° | |

**RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead**
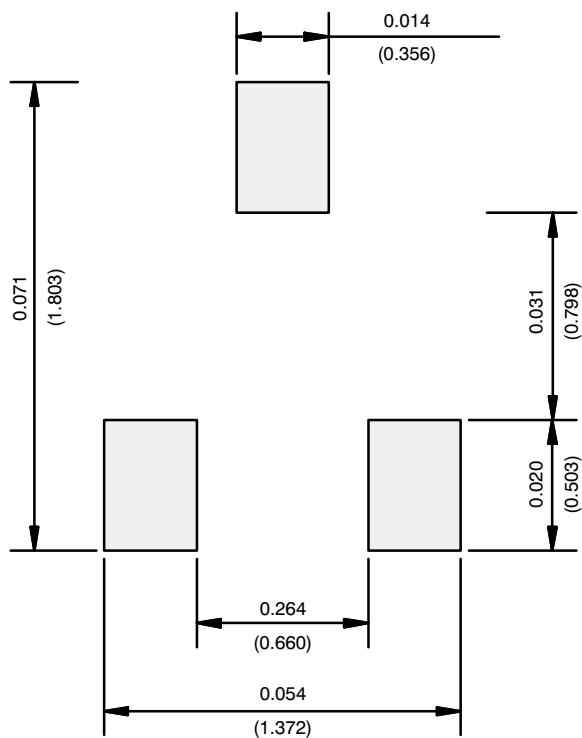


Recommended Minimum Pads
Dimensions in Inches/(mm)

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