Dual N-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) TYP.	I_D (A) [a]	Q_g (TYP.)
12	0.0021 at V_{GS} = 4.5V	26	31 nC
	0.0032 at V_{GS} = 2.5 V	22	

FEATURES

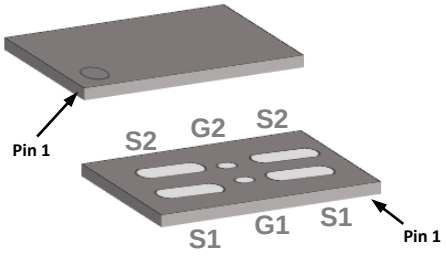
- DT-Trench Power MOSFET
- 100 % R_g and UIS tested
- ESD Protection Diode Embedded

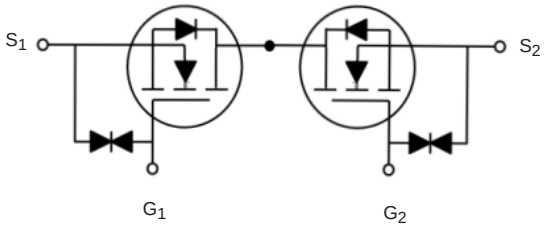
RoHS COMPLIANT

APPLICATIONS

- Battery Management
- POL Applications
- Battery Protection Applications

CSP-6 Dual Pin Configuration





N-Channel MOSFET N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	12	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	26	A
	T_C = 70 °C		19	
	T_A = 25 °C		9.0 [b, c]	
	T_A = 70 °C		5.4 [b, c]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	105	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	26	
	T_A = 25 °C		5.2 [b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	25	
Single Pulse Avalanche Energy		E_{AS}	8.9	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	16	W
	T_C = 70 °C		10.2	
	T_A = 25 °C		2.1 [b, c]	
	T_A = 70 °C		1.3 [b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient [b, f]	t ≤ 10 s	R_{thJA}	50	59.5	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	6	7.8	

Notes

a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. The CSP-6 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 70 °C/W.

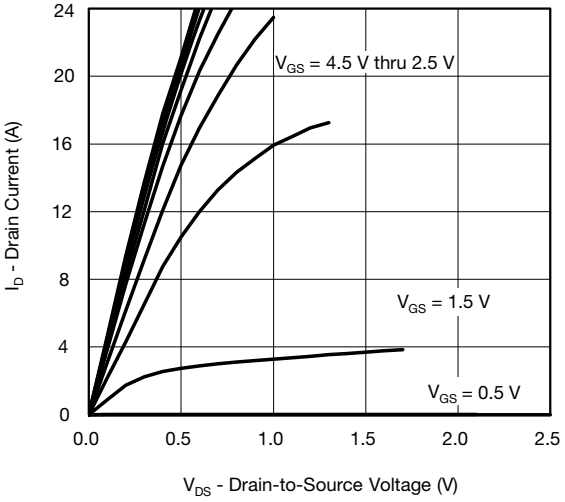
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	12	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	-	20	-	mV/° C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-4.6	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.4	-	1.4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V	-	-	± 10	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 12 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 10 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	26	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 6 A	-	0.0021	0.0028	Ω
		V_{GS} = 2.5 V, I_D = 6A	-	0.0032	0.0059	
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz	-	3050	-	pF
Output Capacitance	C_{oss}		-	1010	-	
Reverse Transfer Capacitance	C_{rss}		-	603	-	
Total Gate Charge	Q_g	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 6 A	-	39	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	9	-	
Gate Resistance	R_g	f = 1 MHz	-	1.60	-	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 6 V, R_L = 1.5 Ω I_D≅6 A, V_{GEN} = 4.5 V, R_g = 1Ω	-	29	-	ns
Rise Time	t_r		-	13	-	
Turn-Off Delay Time	$t_{d(off)}$		-	180	-	
Fall Time	t_f		-	68	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	-	-	26	A
Pulse Diode Forward Current [a]	I_{SM}		-	-	105	
Body Diode Voltage	V_{SD}	I_S = 3 A	-	0.70	1.2	V

Notes

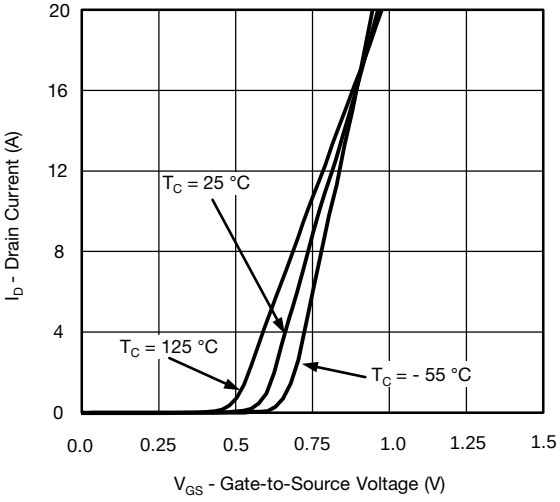
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. T_{CASE} = 25 °C. Expected voltage stress during 100 % UIS test. Production datalog is not available.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

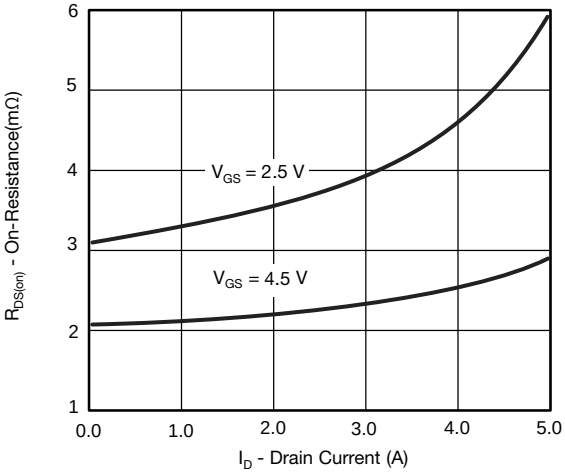
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



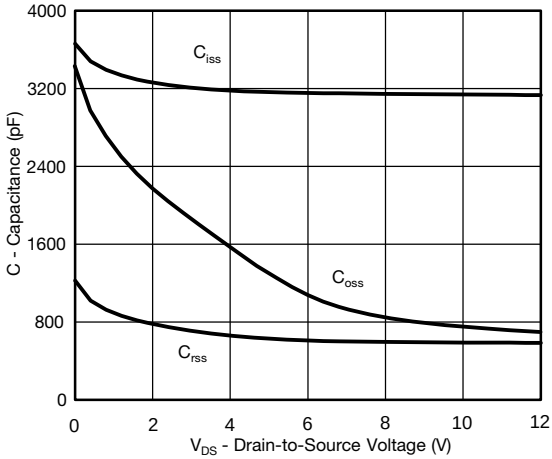
Output Characteristics



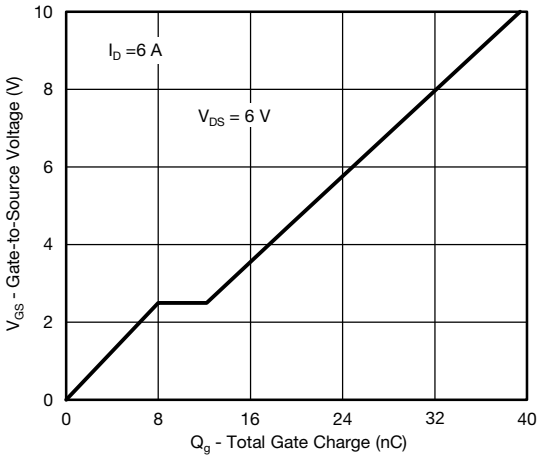
Transfer Characteristics



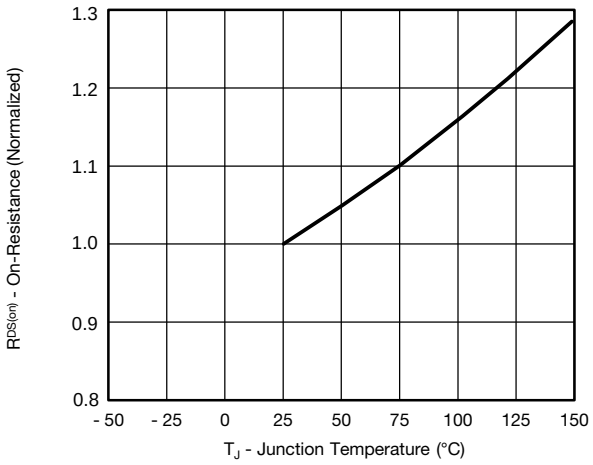
On-Resistance vs. Drain Current



Capacitance

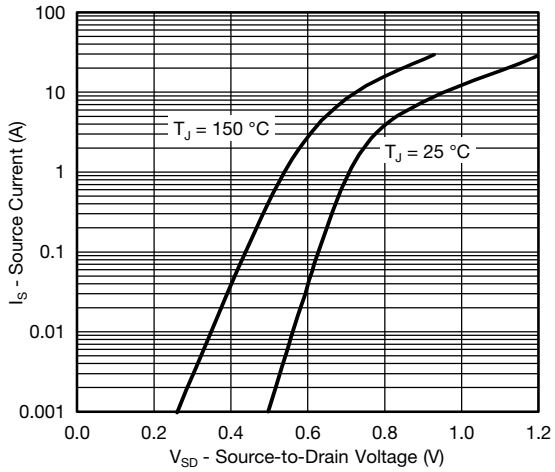


Gate Charge

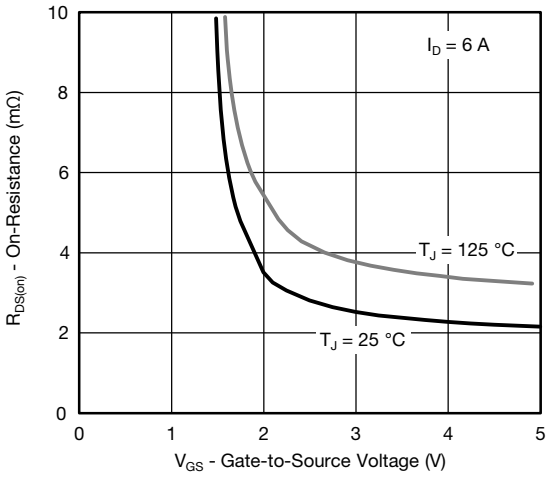


On-Resistance vs. Junction Temperature

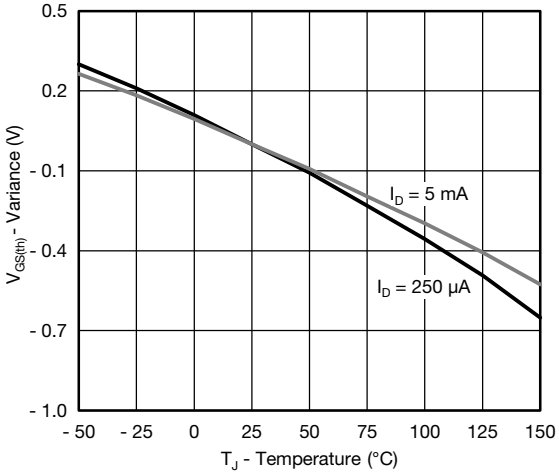
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



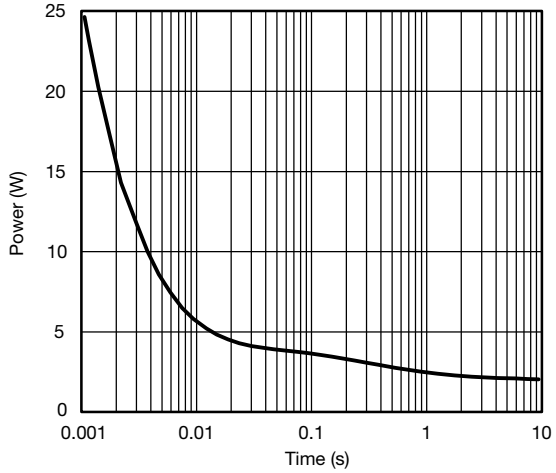
Source-Drain Diode Forward Voltage



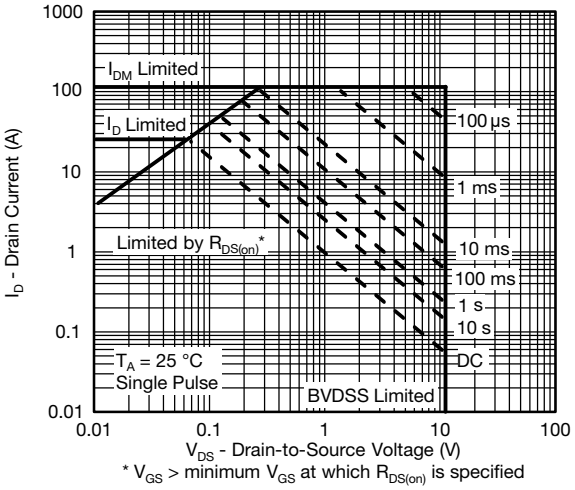
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

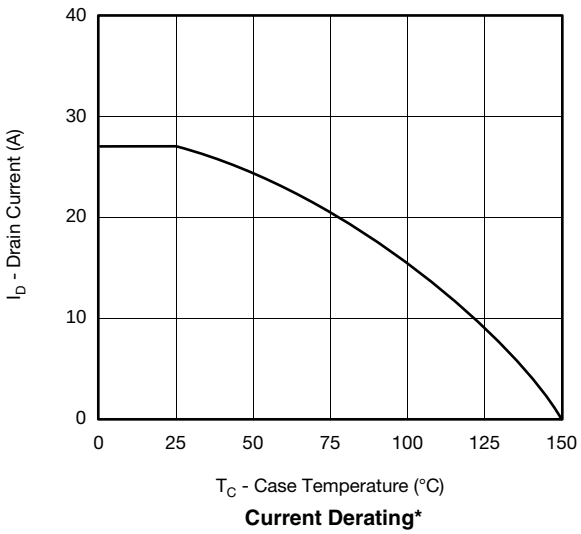


Single Pulse Power, Junction-to-Ambient

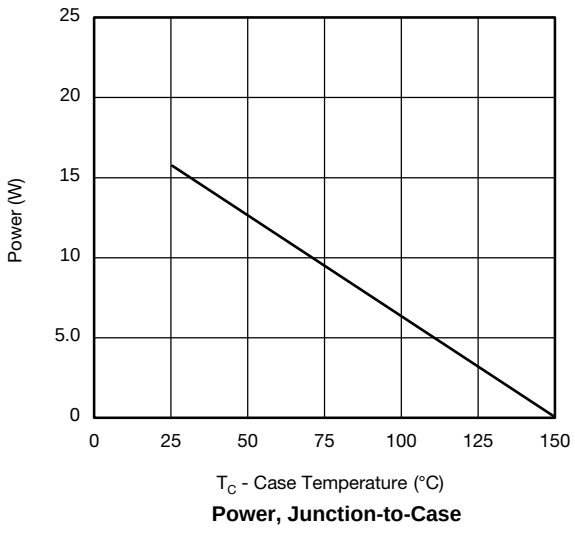


Safe Operating Area

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



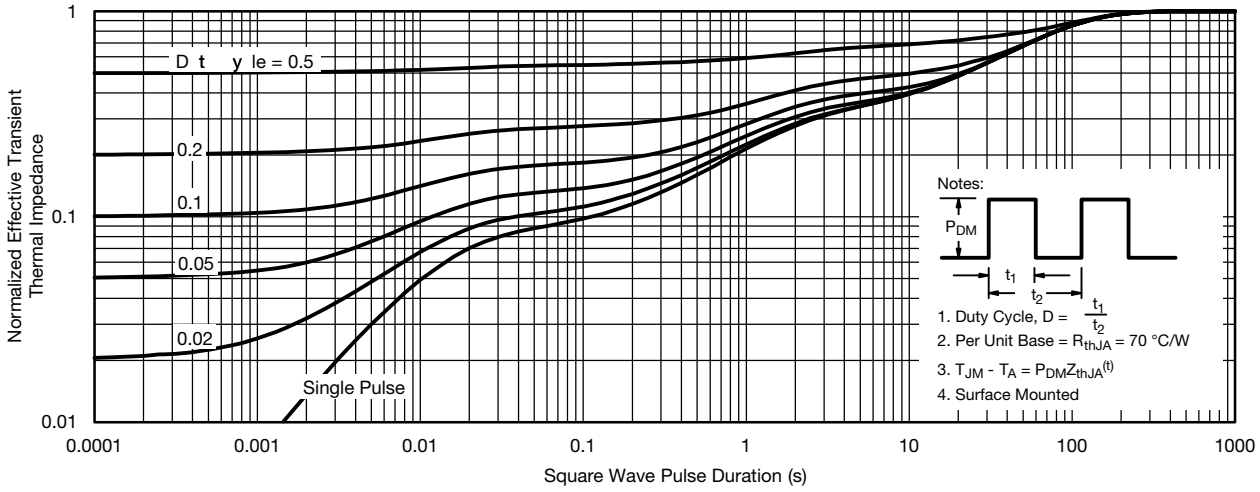
Current Derating*



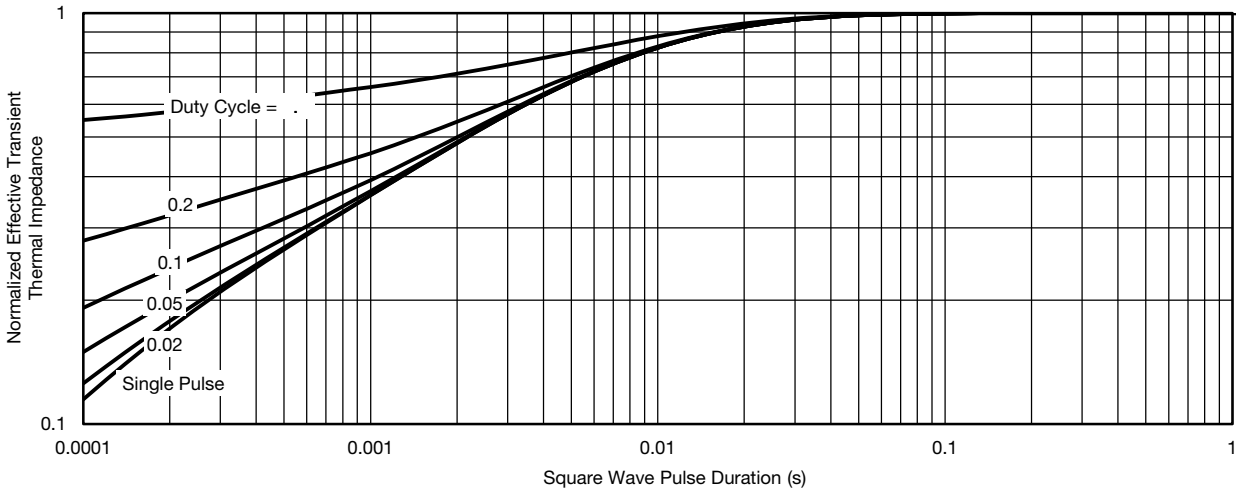
Power, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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