DU361/361B Datasheet

Audio Codec

Rev1.0

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Revision History

Date	Revision	Description
	V0.1	Initial
	V0.2	Added feature description, pin name changes and SNR updates.
	V0.3	Added flash pin assignment
2014-5-26	V0.4	Added the pin function table, and the store/reflow requirements
2014-7-11	V0.5	Renamed the pin 20
2015-3-24	V0.6	Renamed the pin 6,7,35,36,46,47
2015-6-12	V0.7	Added the description of DU361B
2015-10-29	V0.8	Added functional block diagram
2015-11-11	V1.0	Modified the name of some audio effect, added power consumption about the DU361

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1. Overview

The DU361/361B is a member of advanced audio CODEC powered with DSP, designed for portable devices such as boom-boxes, mobile phones, tablets, lap-tops and multimedia speakers etc.

A flexible input configuration for up to three stereo sources and one mono microphone interface is integrated. The inclusion of preamps for analog inputs and drivers for stereo outputs reduce external component requirements as no separate amplifiers are required. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the internal PLL.

Advanced on-chip digital signal processing includes a mixed signal Automatic Level Control (ALC) for the microphone or line inputs through the ADC as well as a Dynamic Range Compressor (DRC) for the DAC output.

The DU361/361B also integrates excellent sound effects. For low-frequency reproduction, MVBASS creates a perceived low bass effect which is usually very difficult to be realized from small speakers. The MV3D effect helps widen the stereo image of the sound. The embedded MVEQ also provides flexible adjustment to satisfy the various listening tastes of customers.

The ACPWorkbench software with rich Graphical User Interface (GUI) makes it easy for sound engineers to fine-tune the device and customize the presets for various audio products.

1.1 Features

- Embedded 20-bit stereo DAC and 16-bit stereo ADC
- DAC SNR 98dB (‘A’ weighted), THD+N -81dB at 48kHz, 3.3V
- ADC SNR 92dB (‘A’ weighted), THD+N -84dB at 48kHz, 3.3V
- I^2S digital audio input and output
- Audio Input
  - 3 x stereo analog inputs
  - 1 x mono microphone input
  - ALC/Noise Gating
- Audio Output

  - 1 x stereo analog output
  - DRC effect
- On-chip Headphone Driver
  - >40mW output power on 16Ω / 3.3V
  - THD –80dB at 20mW, SNR 90dB with 16Ω load
  - No DC blocking capacitors required (capless mode)
- Audio sample rates:
  - 8kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48kHz
- Audio effects
  - MV3D
  - MVBASS
  - MVEQ
- I^2C control interface
- UART code patch transfer interface (only for DU361B)

1.2 Functional block diagram

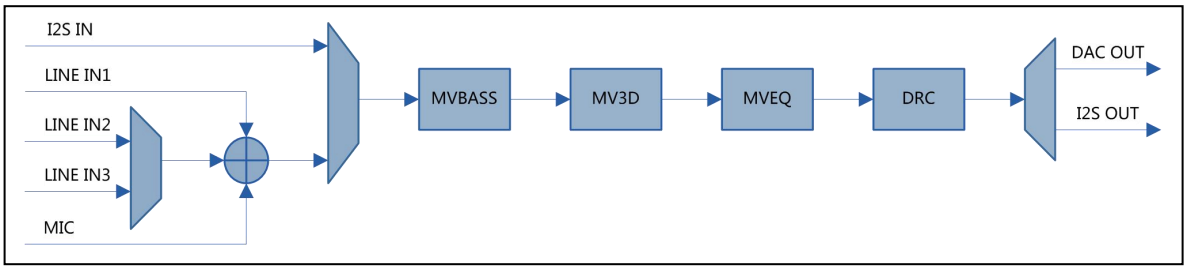


Figure 1 Functional block diagram (DU361)

1.3 The difference between DU361 and DU361B

As audio CODEC chips, both DU361 and DU361B need to used with host MCU such as AP80 series from MVSilicon or other MCUs. The main difference between DU361 and DU361B are the code storage and system BOM cost. Compared to DU361, DU361B obtains codes via UART from host MCU instead of from an external SPI flash, which is the case for DU361. If host MCU provides clock of 32.768kHz to DU361/361B, the external crystal for DU361/361B can be saved as well, which leads to further reduction in system cost.

2. Pin Description

DU361/361B is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
PWR	Power
GND	Ground

2.1 Pin Description

Table 1 Pin Description

Pin name	Pin #	Type	Description
			Audio CODEC interface pins
DAC_R	6	AO	Audio right channel output
DAC_L	7	AO	Audio left channel output
IN1R	9	AI	Line-in channel-1 right input
IN1L	10	AI	Line-in channel-1 left input
IN2R	3	AI	Line-in channel-2 right input
IN2L	2	AI	Line-in channel-2 left input
IN3R	1	AI	Line-in channel-3 right input
IN3L	48	AI	Line-in channel-3 left input
DACVMID	5	AI	Internal voltage reference
MICIN	11	AI	MIC input
MICBIAS	12	AO	MIC voltage reference
			Control pins
SCLK	31	I	I^2C signal
SDAT	30	I/O	I^2C signal
			I^2S IO pins
MCLK	32	I/O	I^2S MCLK
LRCLK_0	33	I/O	I^2S channel-0 sync
BCLK_0	34	I/O	I^2S channel-0 data clock
DOUT_0	35	I/O	I^2S channel-0 DO
DIN_0	36	I/O	I^2S channel-0 DI
LRCLK_1	44	I/O	I^2S channel-1 sync
BCLK_1	45	I/O	I^2S channel-1 data clock
DOUT_1	46	I/O	I^2S channel-1 DO
DIN_1	47	I/O	I^2S channel-1 DI
			GPIO/MCU IO pins

GPIO_A[13:18] (only for DU361B)	21:26	I/O	GPIO PORT, bank A
GPIO_A[21:19]	29:27	I/O	GPIO PORT, bank A
GPIO_B[9:8]	38:37	I/O	GPIO PORT, bank B
GPIO_B[23:20]	43:40	I/O	GPIO PORT, bank B
			CLK pins
XIN	14	I	32.768KHz Crystal oscillator input for PLL
XOUT	13	O	32.768KHz Crystal oscillator output for PLL
			Power/Ground pins
DVSS	39	GND	Ground for digital
LDOIN	16	PWR	LDO power in
LDO33O	15	PWR	LDO 3.3V out
LDO12O	18	PWR	LDO 1.2V out
DCOVDD	19	PWR	Power for PLL
DACVDD	8	PWR	Power for DAC
DACAVSS	4	GND	Ground for DAC
			Flash pins (only for DU361)
FLASH_HOLD	21	I/O	External SPI-flash pins
FLASH_SCK	22	O	External SPI-flash pins
FLASH_SI	23	I/O	External SPI-flash pins
FLASH_WP	24	I/O	External SPI-flash pins
FLASH_SO	25	I/O	External SPI-flash pins
FLASH_CS	26	O	External SPI-flash pins
			MISC pins
POWER_KEY	17	I	Power Key

Notes.

1. All GPIOs can be used as external interrupt pins.
2. Either I^2S channel-0 or I^2S channel-1 can be activated, but not both at the same time.

3. Package

3.1 Package Diagram

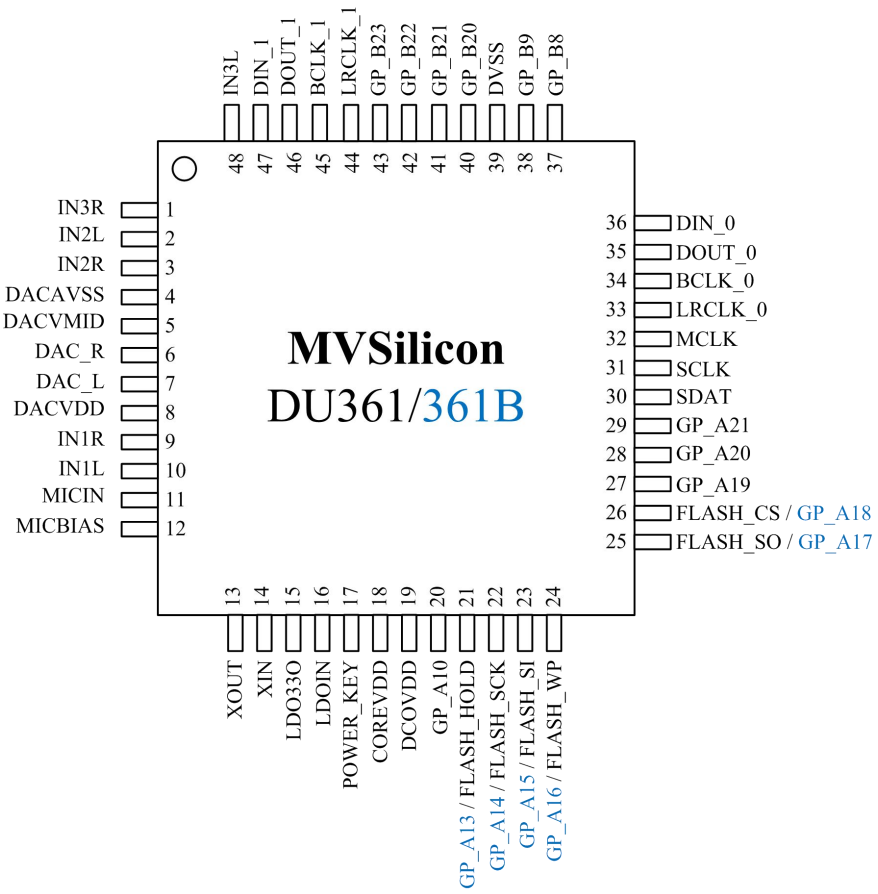


Figure 2 Package Diagram (LQFP48-7x7mm / TOP View)

3.2 Package Dimension Parameter

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50BSC	
L	0.35	0.50	0.65
L1		1.00BSC	
θ	0	—	8°

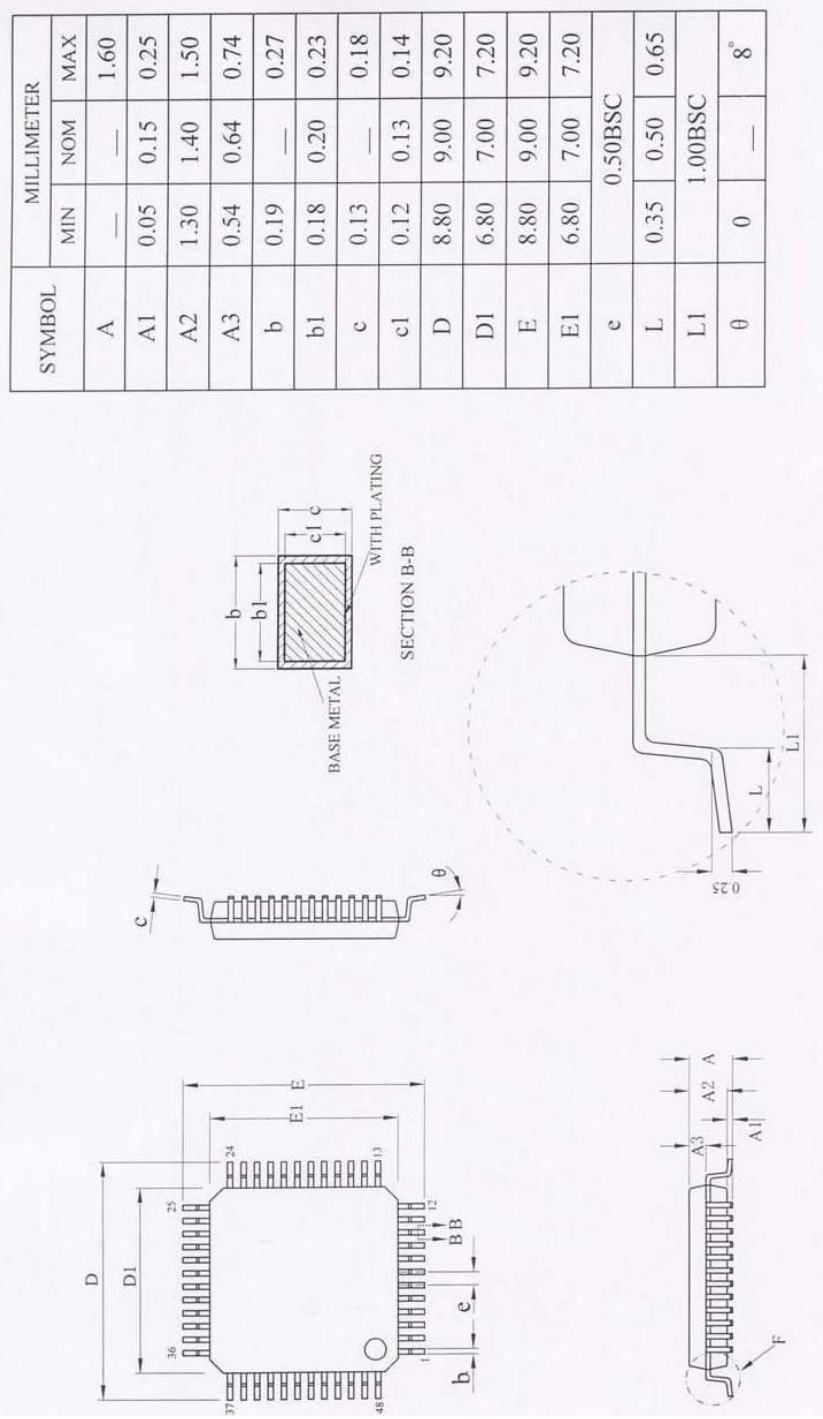


Figure 3 LQFP48-7x7mm Package Dimension Parameter

4. Electrical Specification

4.1 Absolute Maximum Ratings (Note 1)

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature	TEMP_STG	-65 to 150	C

4.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	LDOIN	3.0		5.5	V
IO Input Voltage	VIN	0		3.6	V
Operating_Free Air Temperature	TEMP_OPR	-40		85	C

4.3 Electrical Characteristics

Table 4 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		1.6		3.6	V
VIL	Input Low Voltage		-0.3		1.4	V
VOH	Output high voltage	@IOH=2mA	3.0			V
VOL	Output low voltage	@IOL=2mA			0.3	V
IL	Input leakage current		-10		10	uA

4.4 Power Consumption

Table 5 Power Consumption

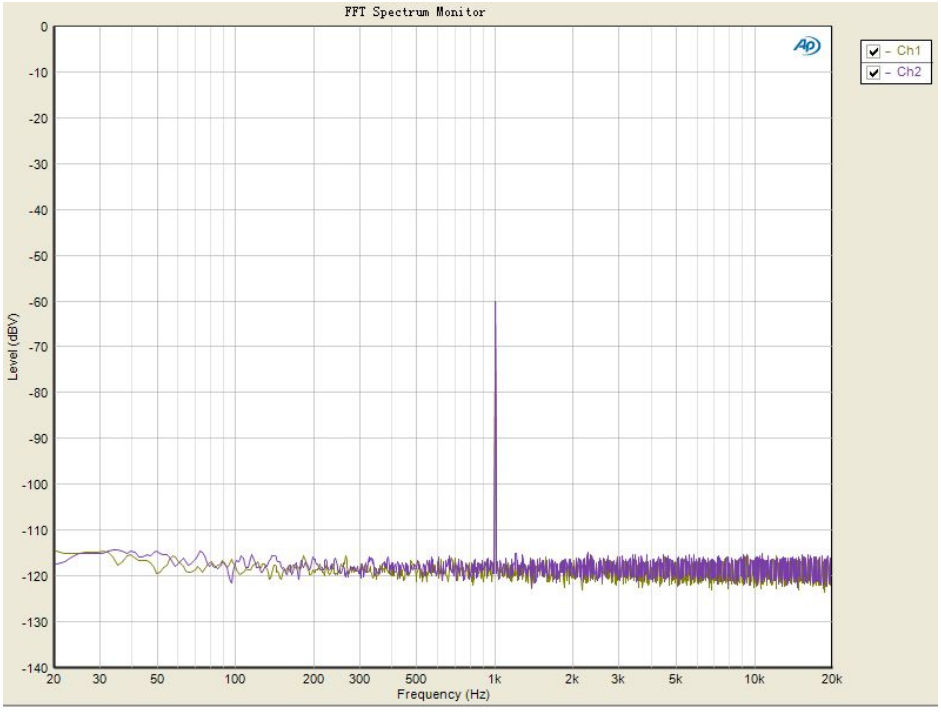
Symbol	Condition	Min	Typ	Max	Unit
IDLE	No path selected and no audio effects		27		mA
I2S-in -> I2S-out	No audio effects		27.7		mA
I2S-in -> DAC-out	No audio effects		31		mA
DRC	Two bands		4		mA
MVBASS			5		mA
MVEQ	Hardware module		0.01		mA
I2S-in -> DAC-out with MVBASS, MVEQ, DRC			40		mA

Note, The test platform is DU361 included GD25Q16B SPI-FLASH.

4.5 Audio Performance

Table 6 Audio DAC Performance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		93.6/93.6		dB
	With A-Weighted Filter		95/95		dB
Signal-to-Noise Ratio	No Filter		95.5/95.6		dB
	With A-Weighted Filter		98/98		dB
THD+N	Peak THD+N (@0dBFS)		-81/-81		dB
	0dBFS		-75/-75		dB
Frequency Response			0.06		dBV
Output Swing			0.993		Vrms
Inter-channel Gain Mismatch			0.003		dB
Volume Control Step			TBD		dB
Volume Control Range			TBD		dB
Group Delay			80		us
Inter-channel Phase Deviation			0.01		degree
Crosstalk			-99/-98		dB

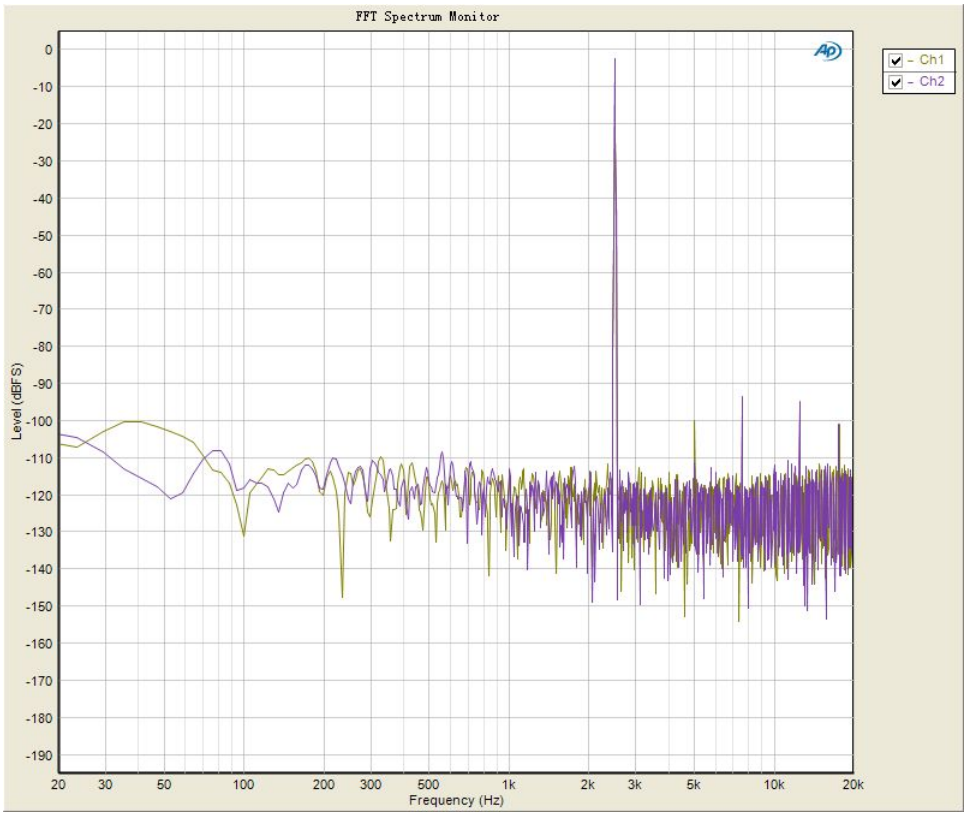


The measured output audio spectrum when the output is at -60 dBV

Table 7 Line-in 1 Channel Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

Dynamic Range	No Filter		88/88		dB
	With A-Weighted Filter		92/92		dB
Signal-to-Noise Ratio	No Filter		88/88		dB
	With A-Weighted Filter		92/92		dB
THD+N	Peak THD+N (@-2.4dBFS)		-84/-84		dB
Volume Control Step			TBD		dB
Volume Control Range			TBD		dB
Group Delay			26		fs
Power Consumption			7.6		mW
Power Supply Rejection Ratio	1kHz, 300mVrms		55		dB



The measured audio spectrum when the analog input is at -2.6 dBV

Table 8 Line-in 2&3 Channel Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		86		dB
	With A-Weighted Filter		89		dB
Signal-to-Noise Ratio	No Filter		85		dB
	With A-Weighted Filter		88		dB
THD+N	Peak THD+N (@-12dBFS)		-75		dB
Group Delay			26		fs
Power Consumption			7.6		mW
Power Supply Rejection Ratio	1kHz, 300mVrms		55		dB

Table 9 MIC Channel Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		87.5		dB
	With A-Weighted Filter		90		dB
Signal-to-Noise Ratio	No Filter		85.5		dB
	With A-Weighted Filter		88.5		dB
THD+N	Peak THD+N (@-2dBFS)		-82		dB
Group Delay			26		fs
Crosstalk			TBD		dB
Power Consumption			7.6		mW
Power Supply Rejection Ratio	1kHz, 300mVrms		55		dB

Note:

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

5. Store and Reflow

DU361/361B is a moisture sensitive component. The moisture sensitivity classification is **Class 3**.

It's important that the parts are handled under precaution and a proper manner.

The handling, baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC/JEDC S-STD-033A.

The Technologies recommends utilizing the standard precautions listed below.

1. Calculated shelf life in Sealed Bag: 12 months at <40℃ and <90% relative humidity(RH)
2. Peak Package Body Temperature: 250℃
3. After bag is opened, devices that will be subjected to reflow solder of other high temperature process must be:
   a. Mounted within 168 hours of factory condition ≤30℃ / 60% RH
   b. Stored at <10% RH if not used
4. Devices require baking, before mounting if:
   a. Humidity indicator card is >10% when read at 23±5℃ immediately after moisture barrier bag is opened
   b. Items 3a or 3b is not met
5. If baking is required, please refer to J-STD-033 standard for low temperature (40℃) baking requirement in Tape/Reel form.

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